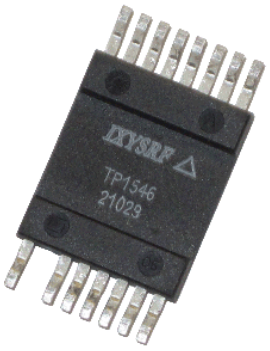
Description

The IXRFDSM607X2 is a dual CMOS high-speed, high-current gate driver specifically designed to drive MOSFETs in Class D and E HF RF applications as well as other applications requiring ultrafast rise and fall times or short minimum pulse widths. The IXRFDSM607X2 can source and sink 7 A of peak current per driver, 15 A when combined, while producing voltage rise and fall times of less than 5 ns and minimum pulse widths of 8 ns. The inputs of the driver are compatible with TTL or CMOS and are fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction or current shoot-through is virtually eliminated. The features and wide safety margin in operating voltage and power make the IXRFDSM607X2 unmatched in performance and value.

The surface mount IXRFDSM607X2 is packaged in a low-inductance surface mount package incorporating advanced layout techniques to minimize stray lead inductances for optimum switching performance. The input and output pins can be separated or combined for dual or single driver operation. However, both sides are ground referenced together and cannot be operated ground isolated from each other.



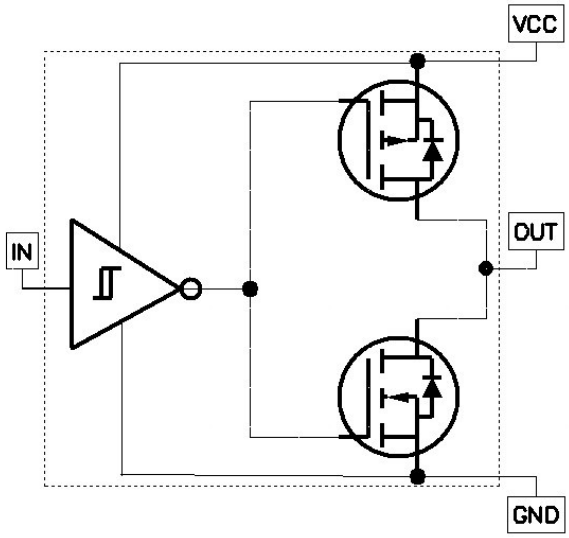
Features

- High Peak Output Current
- Low Output Impedance
- Low Quiescent Supply Current
- Low Propagation Delay
- High Capacitive Load Drive Capability
- Wide Operating Voltage Range
- Single or Dual Driver Operation Capable

Applications

- RF MOSFET Driver
- Class D and E RF Generators
- Multi-MHz Switch Mode Supplies
- Pulse Transformer Driver
- Pulse Laser Diode Driver
- Pulse Generator

Fig. 1- Block Diagram and Truth Table



IN	OUT
0	0
1	1

Absolute Maximum Ratings

Parameter	Value
Supply Voltage V_{CC}	30V
Input Voltage Level V_{IN}	-5V to V_{CC} + 0.3V
All Other Pins	-0.3V to V_{CC} +0.3V
Power Dissipation $T_{A\ (AMBIENT)} \leq 25°C$ $T_{C\ (CASE)} \leq 25°C$	2W 100W **Note: 1**
Storage Temperature	-40°C to 150°C
Soldering Lead Temperature (10 seconds maximum)	300°C

Parameter	Value
Maximum Junction Temperature	150°C
Operating Temperature Range	-40°C to 85° C
Thermal Impedance (Junction to Case) $R_{\Theta JC}$	0.25° C/W
Moisture Sensitivity Level (MSL)	1

Note: Operating the device outside of the "Absolute Maximum Ratings" may cause permanent damage. Typical values indicate conditions for which the device is intended to be functional but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum conditions for extended periods may impact device reliability.

Note: 1- Limited by high frequency performance, not package dissipation.

Electrical Characteristics

Unless otherwise noted, T_A = 25° C, 8V < V_{CC} < 30V.
All voltage measurements with respect to GND. IXRFDSM607X2 configured as described in *Test Conditions with combined outputs*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	8V ≤ V_{CC} ≤ 18V	3.5			V
V_{IL}	Low input voltage	8V ≤ V_{CC} ≤ 18V			0.8	V
V_{HYS}	Input hysteresis			0.25		V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V≤ V_{IN} ≤V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	High output resistance	V_{CC} = 15V I_{OUT} = 100mA		0.42		Ω
R_{OL}	Low output resistance	V_{CC} = 15V I_{OUT} = 100mA		0.22		Ω
I_{PEAK}	Peak output current	V_{CC} = 15V		15		A
I_{DC}	Continuous output current	Limited by package power dissipation		2.5		A
t_R	Rise time	V_{CC}=15V C_L=1nF C_L=2nF		4 5		ns ns
t_F	Fall time	V_{CC} =15V C_L=1nF C_L=2nF		4 5.5		ns ns
t_{ONDLY}	ON propagation delay	V_{CC} =15V C_L=2nF		25		ns
t_{OFFDLY}	OFF propagation delay	V_{CC} =15V C_L=2nF		22		ns
PW_{min}	Minimum pulse width	FWHM V_{CC} =15V C_L=1nF		8		ns
V_{CC}	Power supply voltage	Recommended	8	15	18	V
I_{CC}	Power supply current	V_{CC} = 15V, V_{IN} = 0V V_{CC} = 15V, V_{IN} = 3.5V V_{CC} = 15V, V_{IN} = V_{CC}		0.4 3.8 0.4	1 5 1	mA mA mA

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling.

All specifications are subject to change at any time without notice.

*Outputs combined

Fig. 2

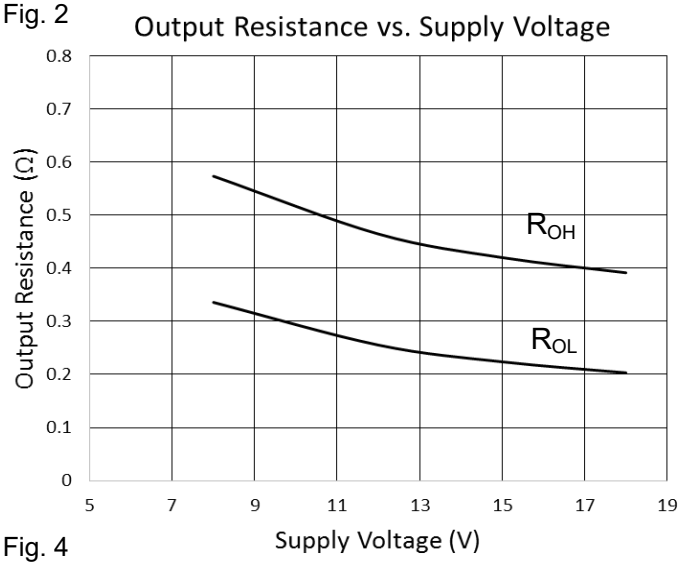


Fig. 3

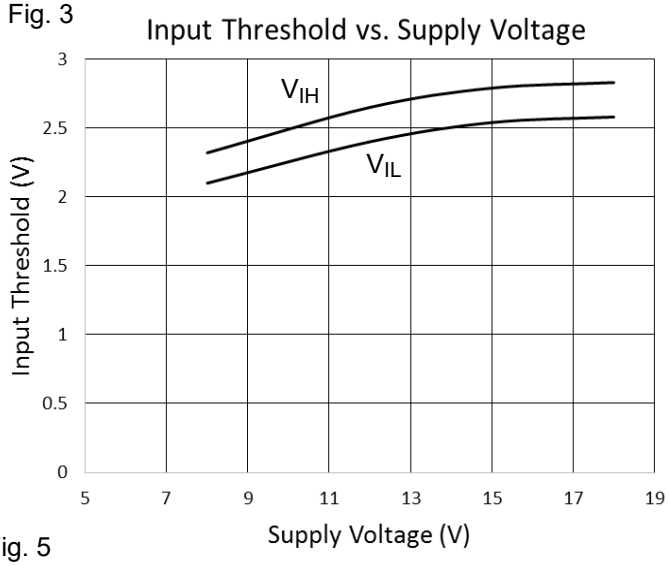


Fig. 4

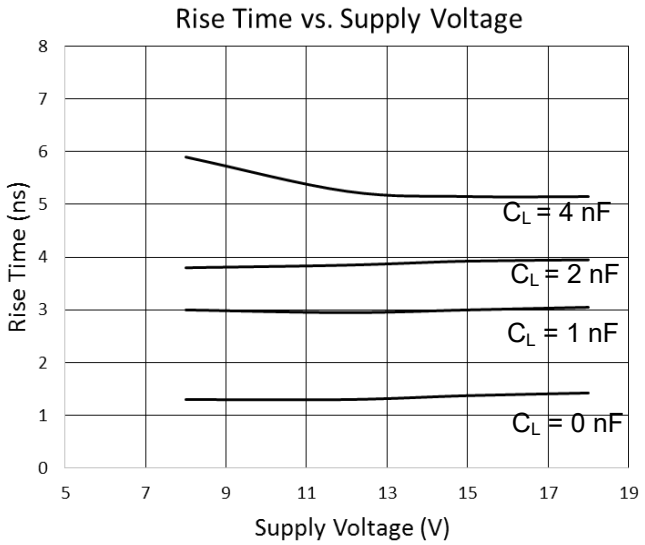


Fig. 5

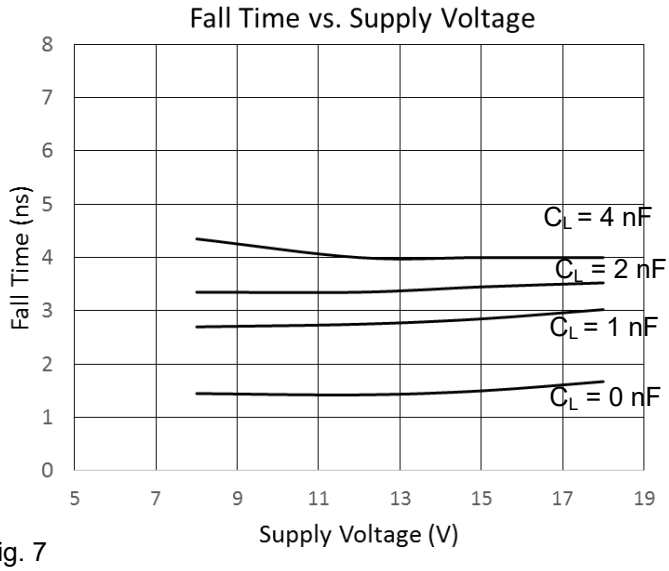


Fig. 6

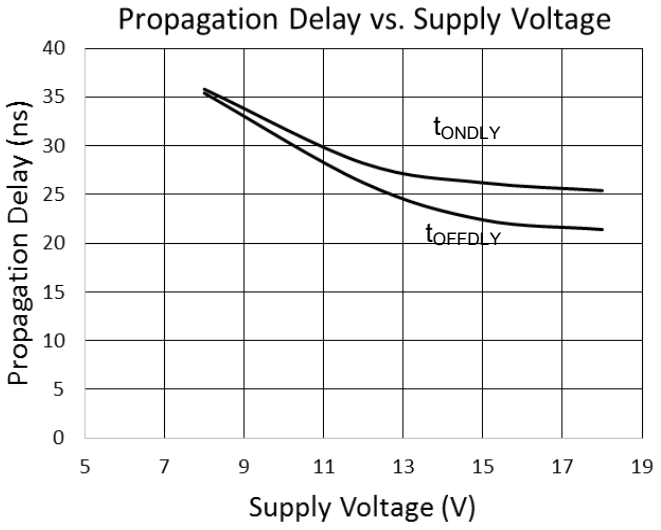
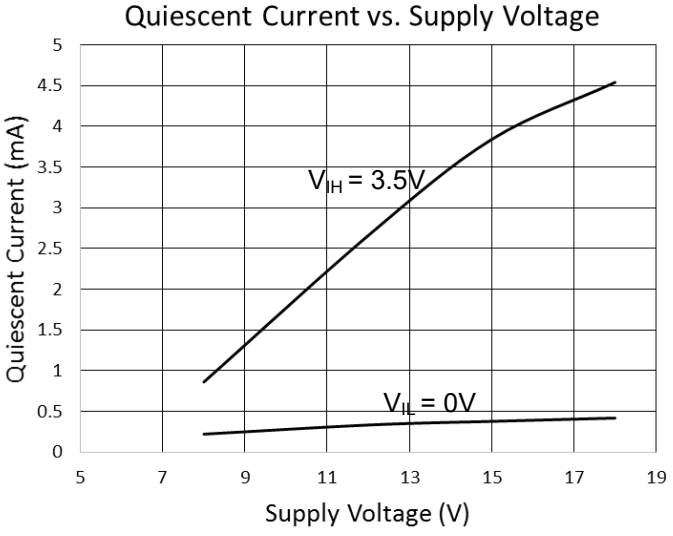


Fig. 7



*Outputs combined

Fig. 8

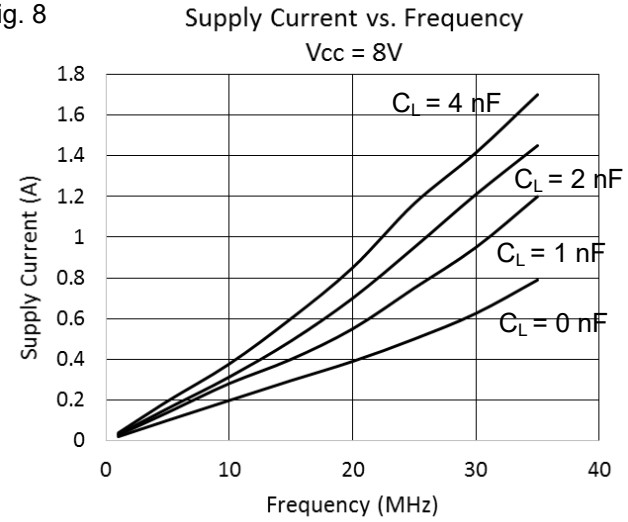


Fig. 9

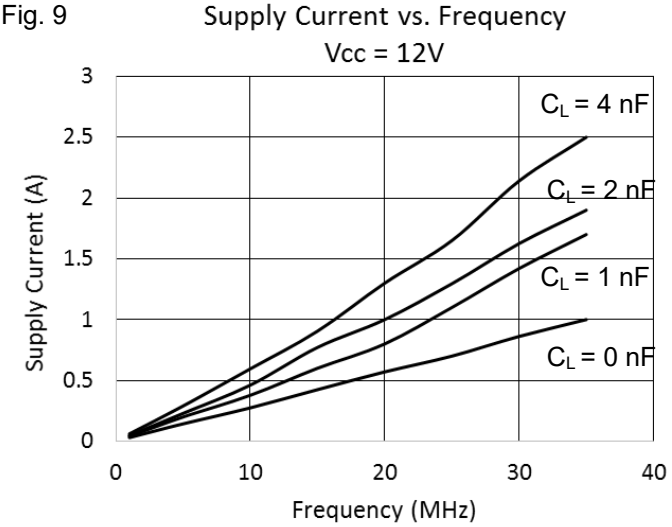


Fig. 10

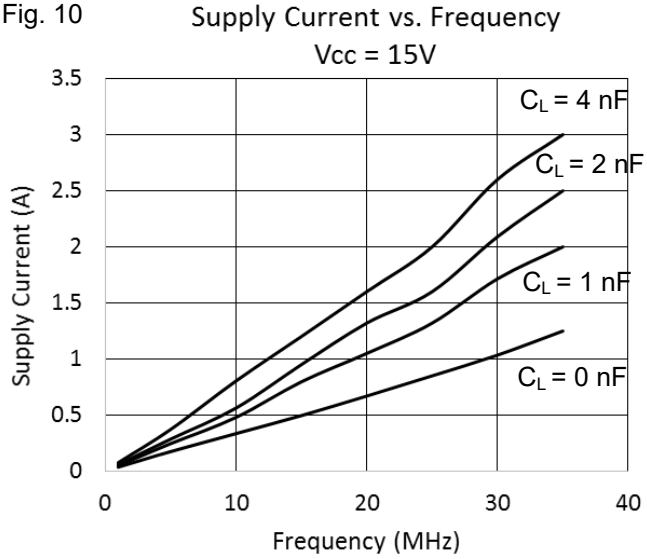


Fig. 11

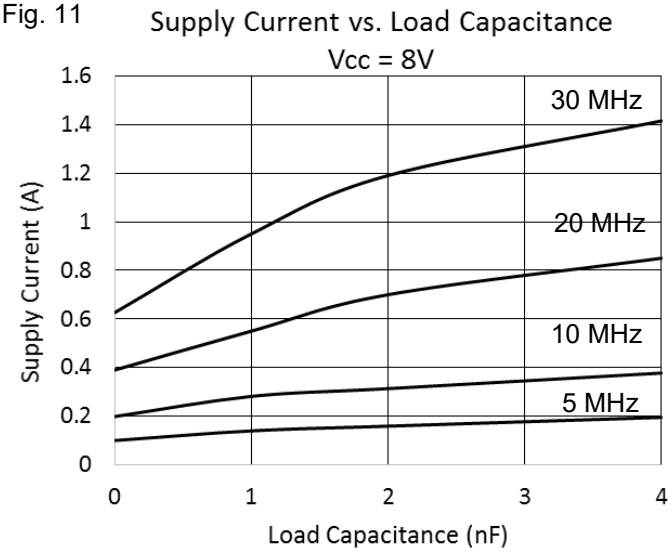


Fig. 12

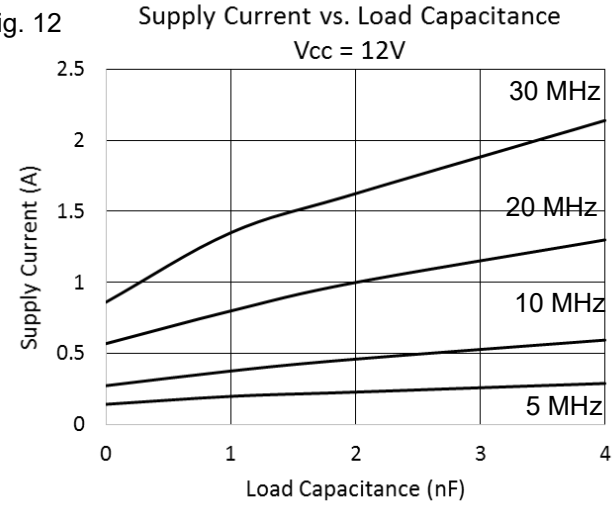
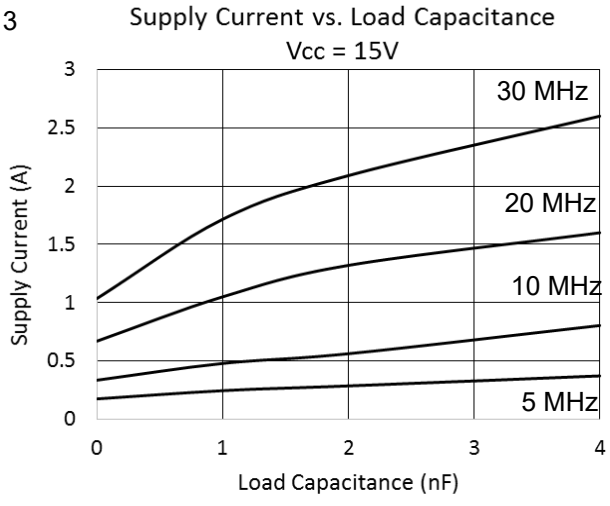


Fig. 13



*Outputs combined

Fig. 14 Peak Source Current vs. Supply Voltage

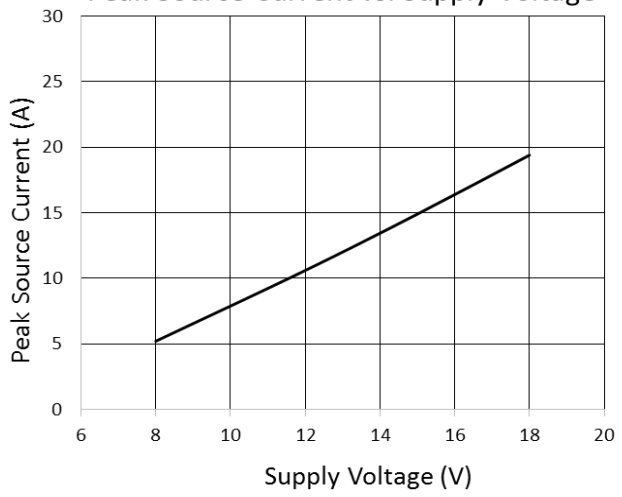


Fig. 15 Peak Sink Current vs. Supply Voltage

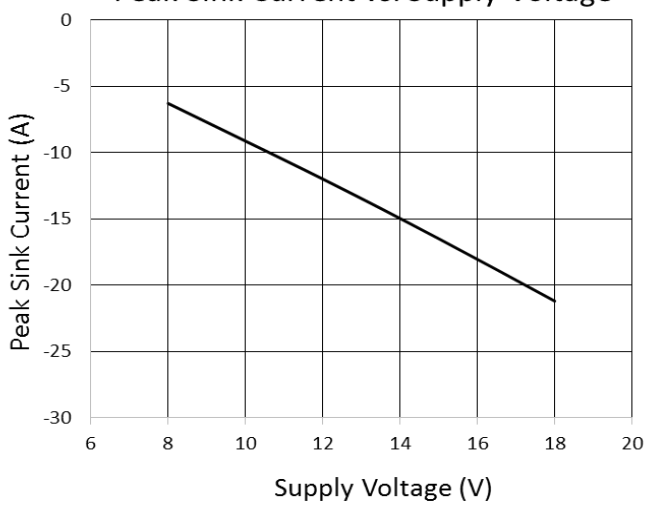


Fig. 16 Peak Source Current vs. Temperature
Vcc = 15V

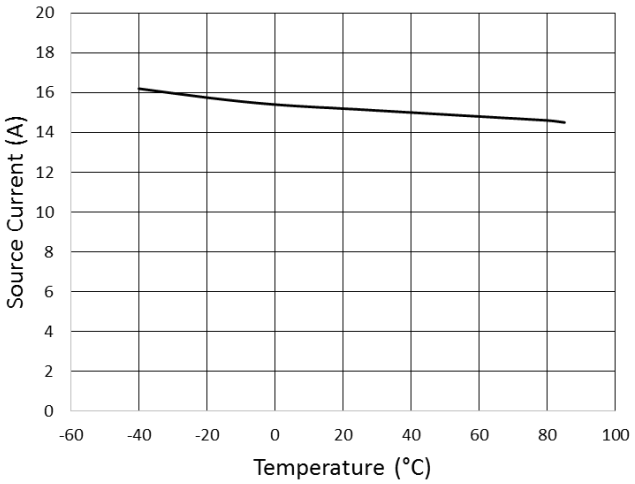


Fig. 17 Peak Sink Current vs. Temperature
Vcc = 15V

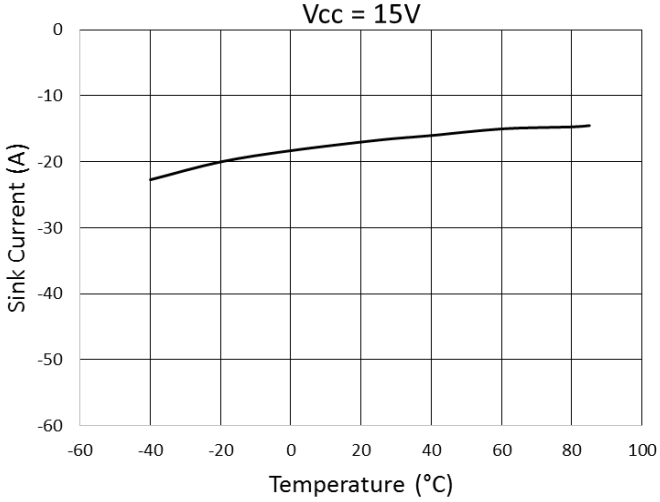


Fig. 18 Rise Time Normalized vs. Temperature
Vcc = 15V

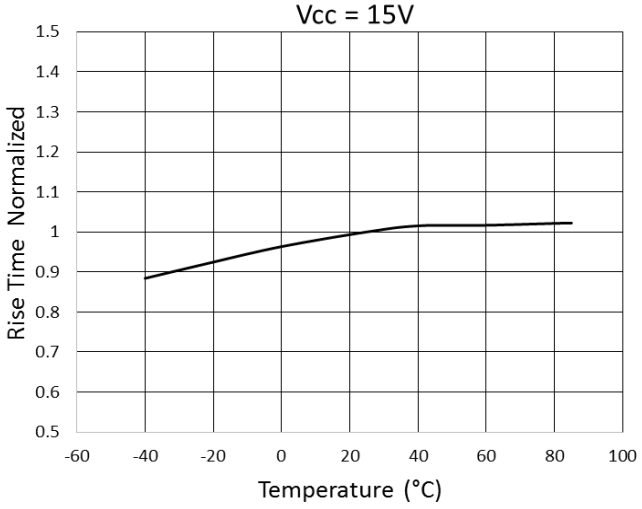


Fig. 19 Fall Time Normalized vs. Temperature
Vcc = 15V

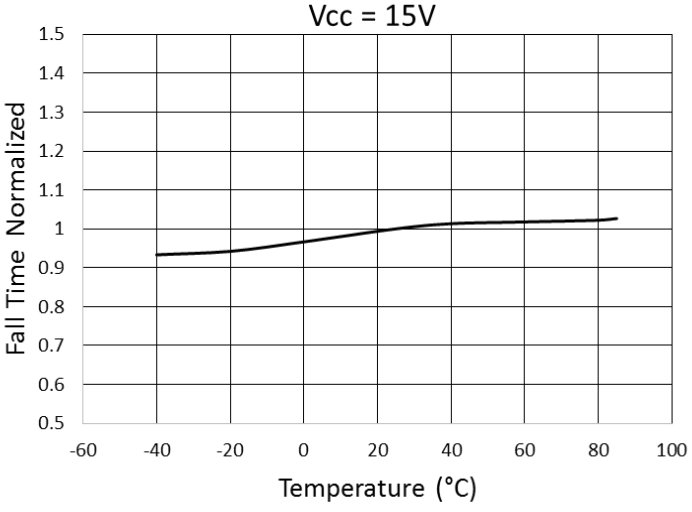


Fig. 20 Pin Description

Symbol	Function	Pin Number	Description
V_{CC}	Supply Voltage	1, 3, 6, 7, 8	Positive power supply voltage input.
IN	Input	4, 5	Input signal-TTL or CMOS compatible.
OUT	Output	11, 12, 13, 14	Device Output. For application purposes, connect directly to the Gate of a MOSFET
GND	Power Ground	9, 10, 15, 16	Device ground leads, should be connected to a low noise analog ground plane for optimum performance.

Fig. 21 Test Circuit Diagram– Combined input and output pins for single driver operation

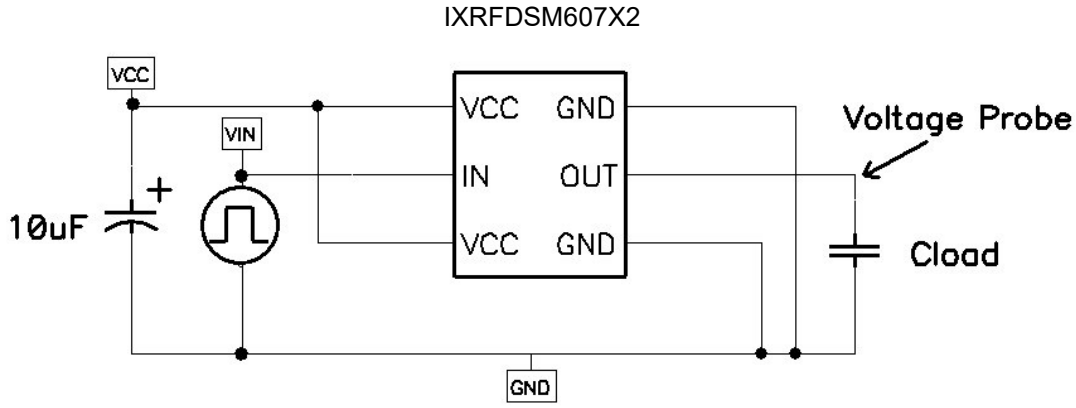


Fig. 22 Timing Diagram

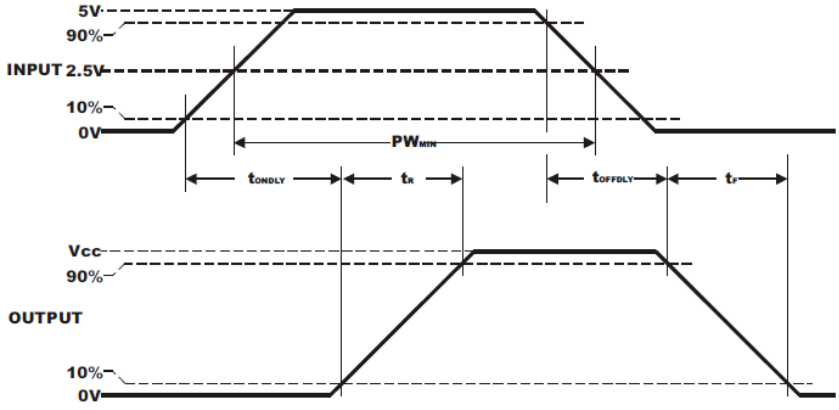
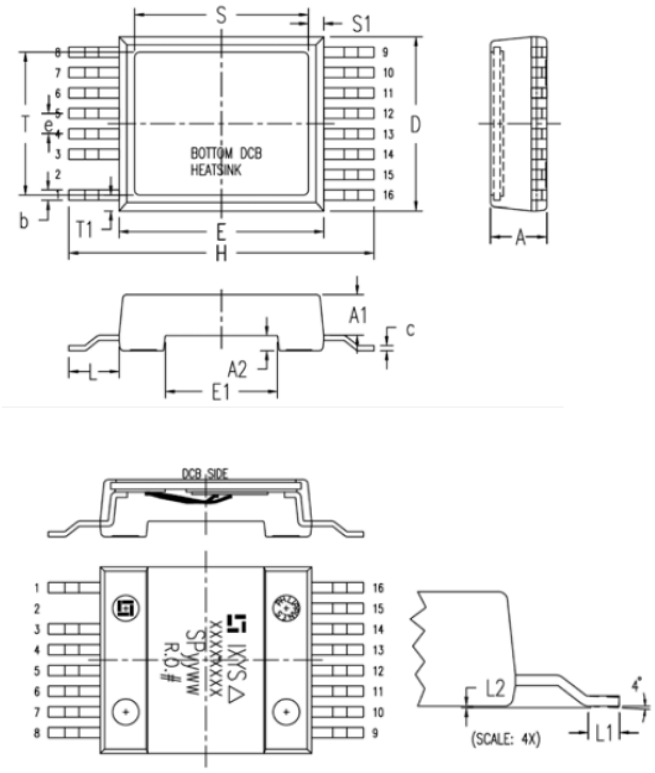


Fig. 23 Package Diagram

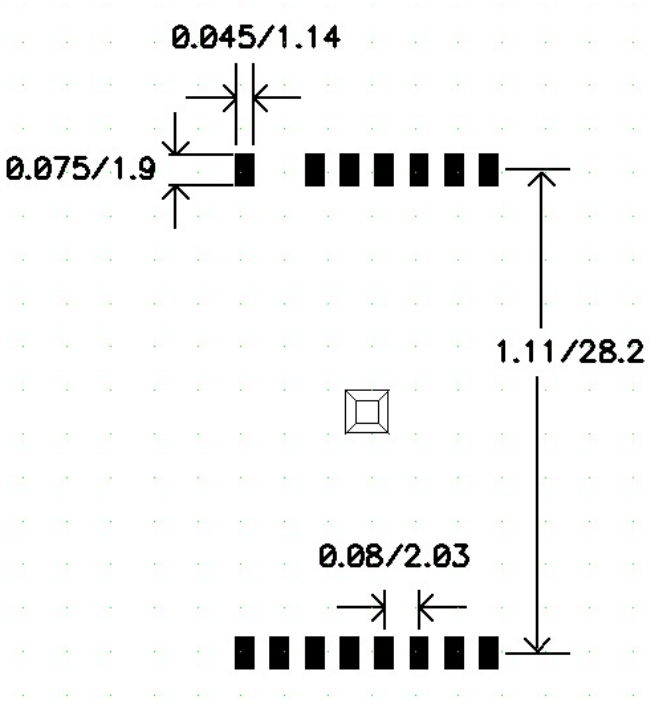


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.661	.677	16.80	17.20
E	.780	.795	19.80	20.20
E1	.425	.441	10.80	11.20
e	.079 BSC		2.00 BSC	
H	1.161	1.185	29.50	30.10
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.661	.677	16.80	17.20
S1	.051	.067	1.30	1.70
T	.543	.559	13.80	14.20
T1	.051	.067	1.30	1.70

Note:
1. ALL LEADS ARE PURE MATTE TIN PLATED.
2. Cu SURFACE OF BOTTOM DCB IS PRE-Ni PLATED UNLESS OTHERWISE STATED
3. Cu SURFACE OF BOTTOM DCB IS ELECTRICALLY ISOLATED 2,500V AC FROM ALL OTHER LEADS.
4. PIN 2 N/A, missing, used for device orientation

Fig. 24 Footprint and PCB layout

For optimum results, multiple pins of the same type should be grouped together on the PCB as shown below. This assures wide traces to the attached driver and load, minimizing parasitic inductance. For best operation, the ground lead groups are ideally incorporated into a large contiguous ground plane on the same side of mounting on the circuit board. In other words, instead of routing ground traces to the device during layout, the footprint is set over a large ground plane with drain and gate traces routed out of the ground plane. This is done during layout by first establishing a polygon that covers the entire PCB, representing the ground plane, that is 'poured' around needed traces by the layout software.



inch/mm

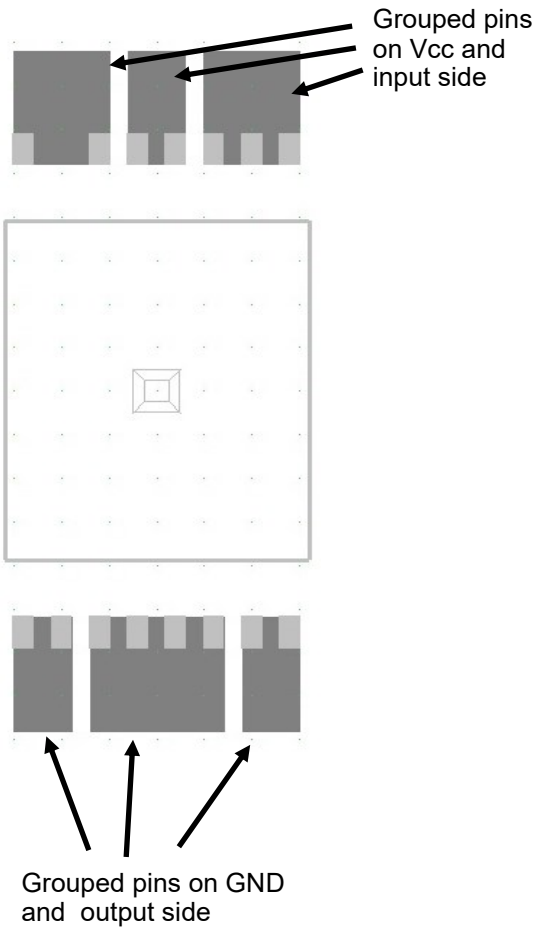
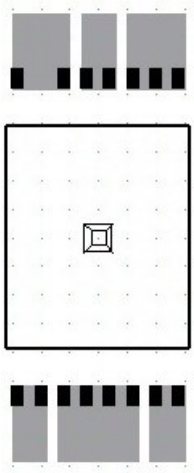


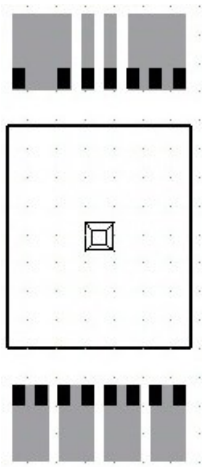
Fig. 25 Footprint Configuration

The IXRFDSM607X2 has the ability to operate as a dual or single driver depending on how the PCB footprint is configured. The footprints below show the combined inputs and outputs pins to form a single 15 A driver and uncombined inputs and outputs to provide a dual 7.5 A driver configuration. While the dual configuration can operate independently, side-to-side, they are not ground isolated from each other and cannot be used ground referenced on one side and floating on the other as would be the requirement in a half-bridge topology.

Combined input and output footprint



Dual input and output footprint



Applications Information

Introduction
Circuits capable of very high switching speeds and high frequency operation require close attention to several important issues. Key elements include circuit loop inductance, Vcc bypassing, and grounding.

Circuit Loop Inductance
The Vcc to Ground current path defines the loop that generates the inductive term. This loop must be kept as short as possible. The output lead must be no further than 0.375 inches (9.5 mm) from the gate of the MOSFET. Furthermore, the output ground leads must provide a balanced symmetric coplanar ground return for optimum operation.

Vcc Bypassing
In order to turn a MOSFET on properly, the IXRFDSM607X2 must be able to draw up to 15 A of current from the Vcc power supply in 2 ns to 6 ns (depending upon the input capacitance of the MOSFET being driven). Good performance requires very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value much larger than the load capacitance. Usually, this is achieved by placing two or three different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected for low inductance, low resistance, and high pulse current service.) Care should be taken to keep the lengths of the leads between these bypass capacitors and the IXRFDSM607X2 to an absolute minimum.

The bypassing should be comprised of several values of MLC (Multi-Layer Ceramic) capacitors symmetrically placed on either side of the IC. Recommended values are 0.01uF and 0.47uF for bypass and at least two 4.7uF tantalums for bulk storage.

Grounding
In order for the design to turn the load off properly, the IXRFDSM607X2 must be able to drain 15 A of current into an adequate grounding system. There are two paths for returning current that need to be considered: Path one is between the IXRFDSM607X2 and its load, and path two is between the IXRFDSM607X2 and its power supply. Both of these paths should be as low in resistance and inductance as possible, and thus as short as practical.

Output Lead Inductance
Of equal importance to supply bypassing and grounding are issues related to the output lead inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible, and treated as coplanar transmission lines. In configurations where the optimum configuration of circuit layout and bypassing cannot be used, a series resistance of a few ohms in the gate lead may be necessary to dampen ringing.

Heat Sinking
For high power operation, the bottom side metallized substrate should be placed in compression against an appropriate heat sink. The substrate is metalized for improved heat dissipation, and is not electrically connected to the device or to ground. See the technical note “DE-Series MOSFET and IC Mounting Instructions” on the IXYS Colorado website at www.ixyscolorado.com for detailed mounting instructions.

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