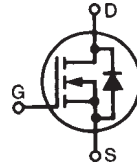


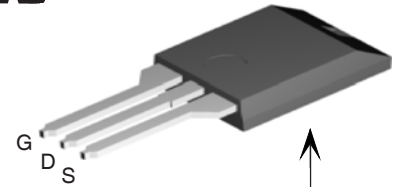
Trench Gate Power MOSFET (Electrically Isolated Back Surface)

N-Channel Enhancement Mode
Avalanche Rated



$$\begin{aligned} V_{DSS} &= 250V \\ I_{D25} &= 40A \\ R_{DS(on)} &\leq 31m\Omega \end{aligned}$$

ISOPLUS220 (IXTC)
E153432



Isolated back surface

G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	250	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	250	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	40	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	230	A
I_{AS}	$T_C = 25^\circ\text{C}$	5	A
E_{AS}	$T_C = 25^\circ\text{C}$	2	J
P_D	$T_C = 25^\circ\text{C}$	147	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6mm (0.062 in.) from case for 10s	300	$^\circ\text{C}$
T_{SOLD}	Plastic body for 10 seconds	260	$^\circ\text{C}$
V_{ISOL}	50/60Hz, $t = 1$ minute, $I_{ISOL} < 1\text{mA}$, RMS	2500	V
F_C	Mounting force	11..65 / 2.5..14.6	N/lb.
Weight		2	g

Features

- Silicon chip on Direct-Copper-Bond substrate
- Isolated mounting surface
- 2500V electrical isolation
- Low drain to tab capacitance ($< 30\text{pF}$)

Advantages

- Easy assembly
- Space savings
- High power density

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Uninterruptible power supplies
- High speed power switching applications

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu\text{A}$	250		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1\text{mA}$	3		5 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			5 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 48A$, Note 1		27	31 m Ω

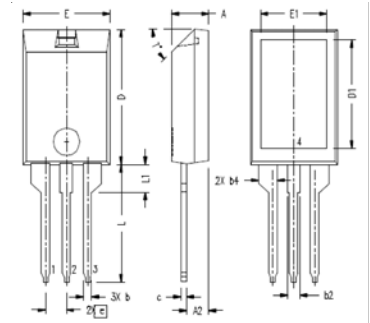
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 48\text{A}$, Note 1	50	82	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		6100	pF
C_{oss}			625	pF
C_{rss}			75	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 15\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 48\text{A}$ $R_G = 2.5\Omega$ (External)		20	ns
t_r			22	ns
$t_{d(off)}$			59	ns
t_f			28	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 V_{DSS}$, $I_D = 48\text{A}$		114	nC
Q_{gs}			33	nC
Q_{gd}			34	nC
R_{thJC}			0.85	$^\circ\text{C/W}$
R_{thCS}		0.21		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			96 A
I_{SM}	Repetitive, pulse width limited by T_{JM}			300 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 48\text{A}$, $-di/dt = 250\text{A}/\mu\text{s}$ $V_R = 100\text{V}$, $V_{GS} = 0\text{V}$		158	ns
I_{RM}			23	A
Q_{RM}			1.8	μC

Notes: 1. Pulse test: $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

ISOPLUS220 (IXTC) Outline



1. Gate 2. Drain
3. Source

Note: Bottom heatsink (Pin 4) is electrically isolated from Pins 1, 2 and 3.

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100	BASIC	2.55	BASIC
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T*			42.5*	47.5*

PRELIMINARY TECHNICAL INFORMATION

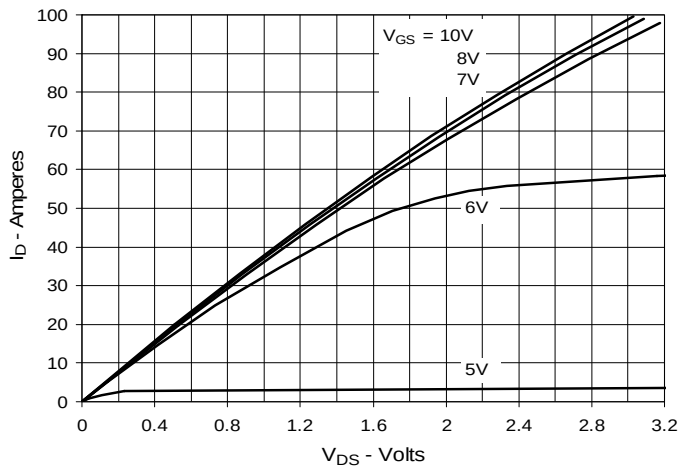
The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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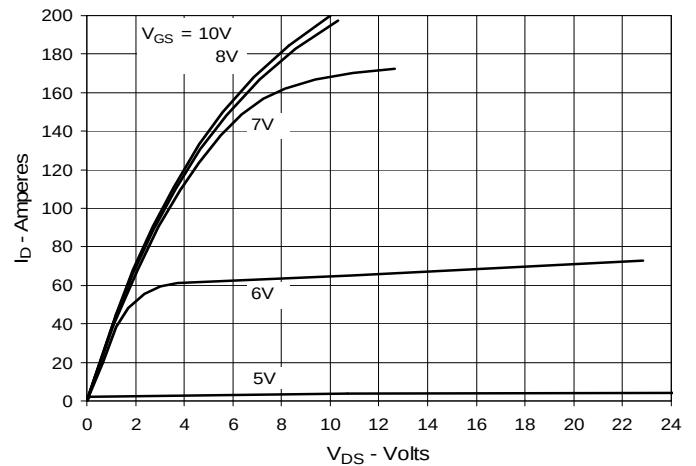
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338 B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

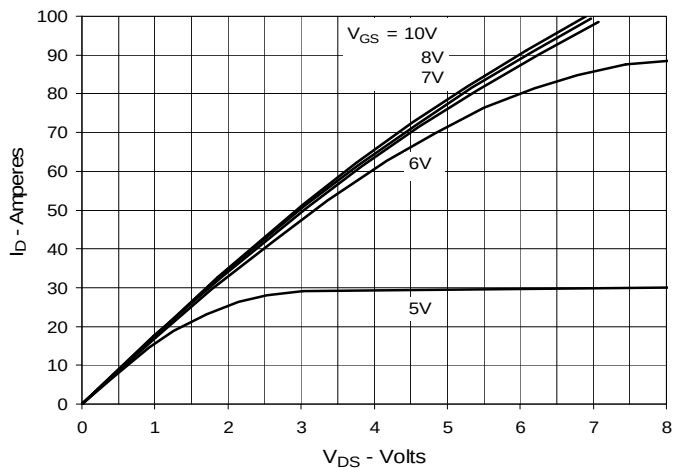
**Fig. 1. Output Characteristics
@ 25°C**



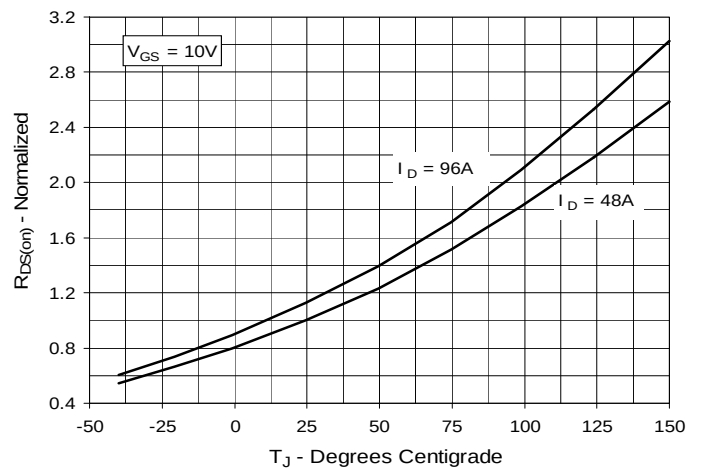
**Fig. 2. Extended Output Characteristics
@ 25°C**



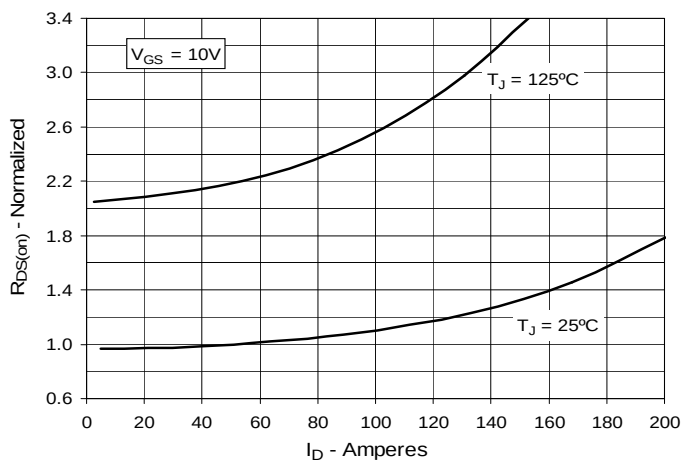
**Fig. 3. Output Characteristics
@ 125°C**



**Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 48\text{A}$ Value
vs. Junction Temperature**



**Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 48\text{A}$ Value
vs. Drain Current**



**Fig. 6. Maximum Drain Current vs.
Case Temperature**

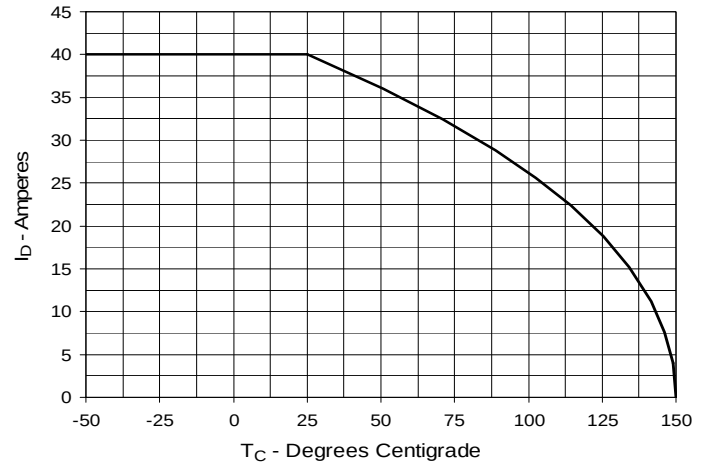


Fig. 7. Input Admittance

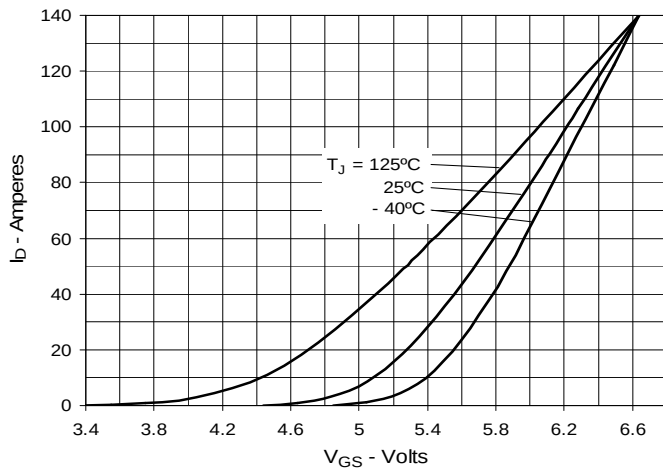


Fig. 8. Transconductance

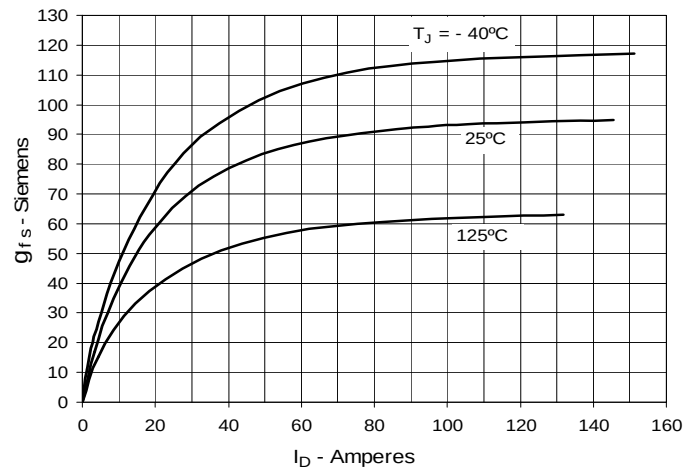


Fig. 9. Forward Voltage Drop of Intrinsic Diode

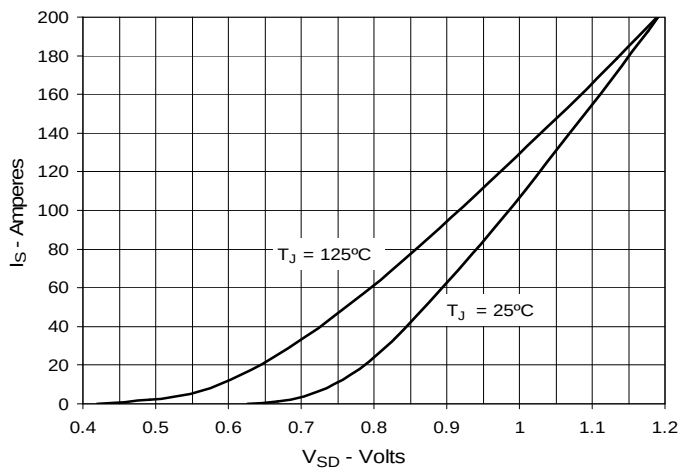


Fig. 10. Gate Charge

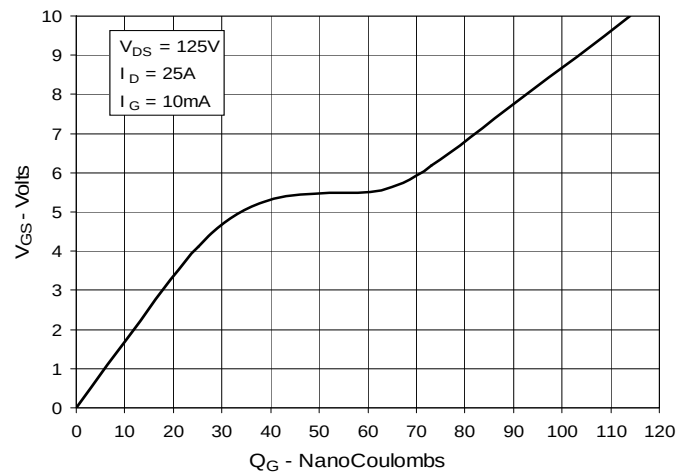


Fig. 11. Capacitance

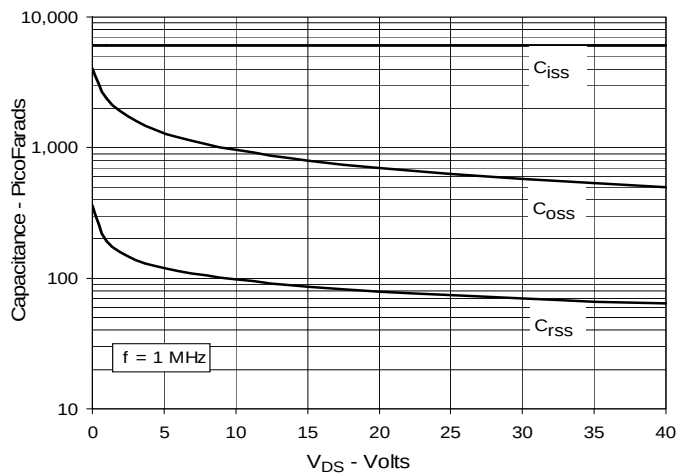
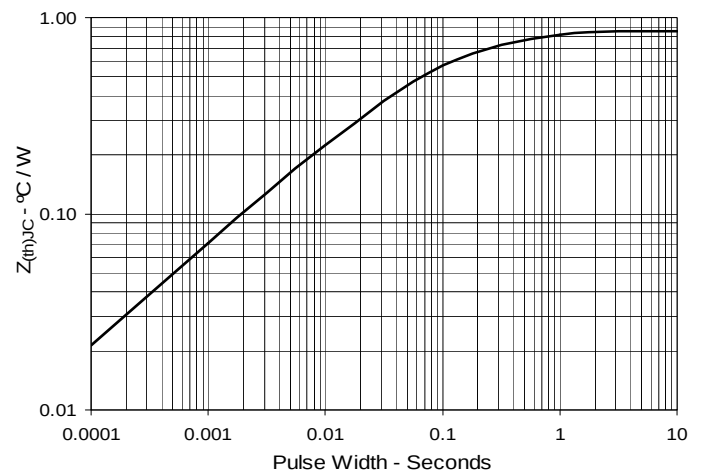
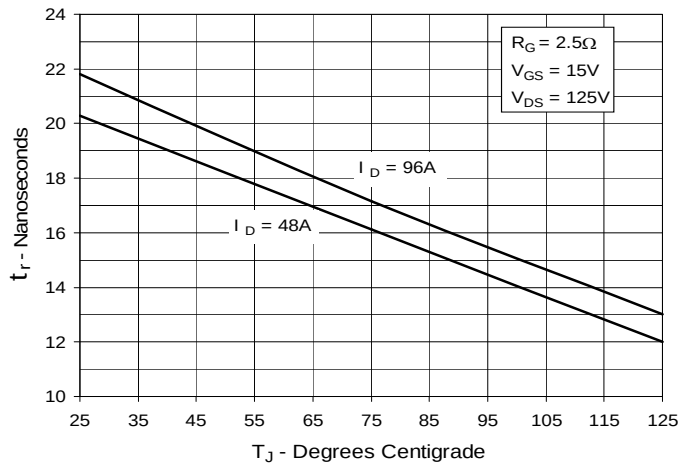


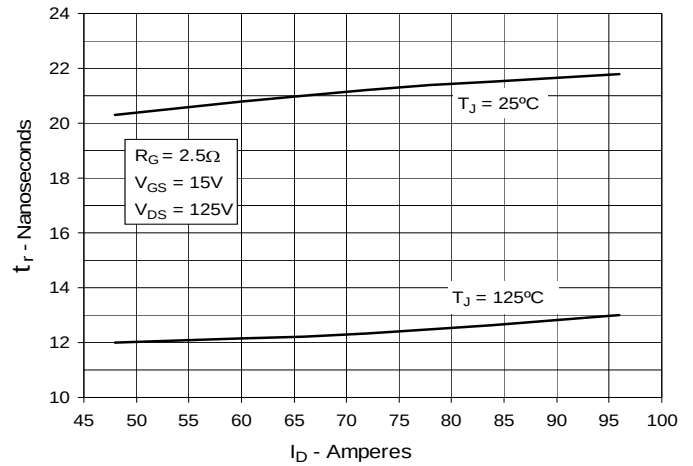
Fig. 12. Maximum Transient Thermal Impedance



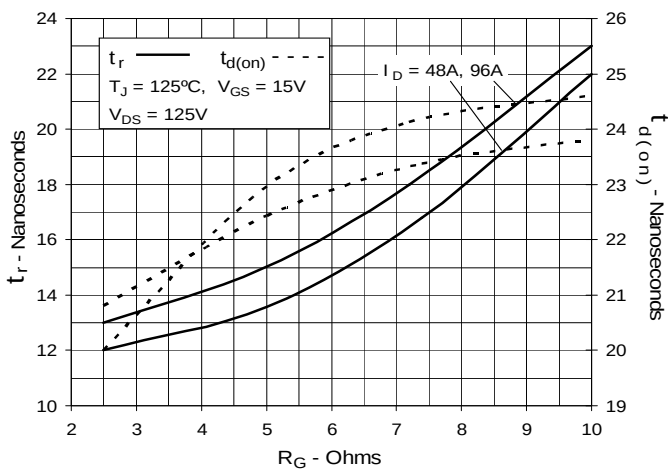
**Fig. 13. Resistive Turn-on
Rise Time vs. Junction Temperature**



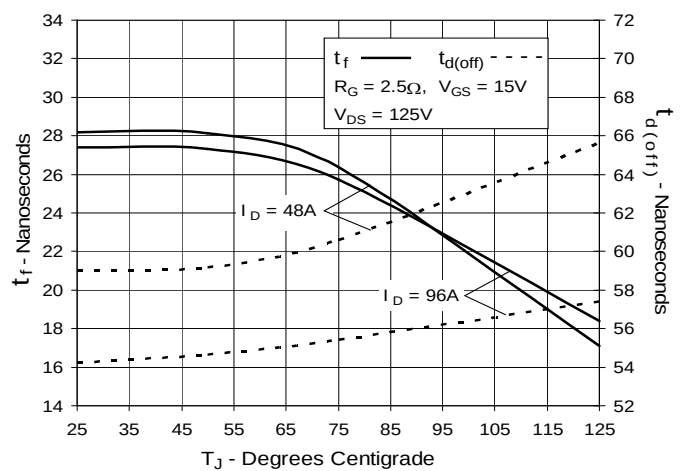
**Fig. 14. Resistive Turn-on
Rise Time vs. Drain Current**



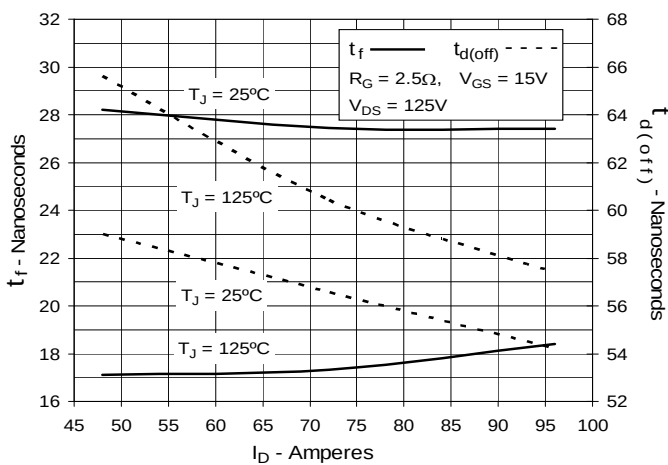
**Fig. 15. Resistive Turn-on
Switching Times vs. Gate Resistance**



**Fig. 16. Resistive Turn-off
Switching Times vs. Junction Temperature**



**Fig. 17. Resistive Turn-off
Switching Times vs. Drain Current**



**Fig. 18. Resistive Turn-off
Switching Times vs. Gate Resistance**

