IZ0065

40 Channel Segment / Common Driver For Dot Matrix LCD

The IZ0065 is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 20 × 2 bit bi-directional shift register, 20 × 2 bit data latch and 20 × 2 bit driver. This LSI can be used a common or segment driver.

FEATURES

- Display driving bias: static -1/5
- Power supply voltage: +5V ± 10%, +3V ± 10%
- Supply voltage for display: 0 ~ -5V(V_{EE})
- Interface

driver(cascade connection)	controller
Other IZ0065	IZ0066 KS0066 HD44780 SED1278

- CMOS Process
- Bare chip available

FUNCTIONS

- Dot matrix LCD driver with 40-channel output.
- Selectable function to use common/segment drivers simultaneously.
- Input / Output signal

- output: 20 × 2 channel waveform for LCD driving

- input: - Serial display data and control pulse from the controller LSI.

- Bias voltage (V_1-V_6)

ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3 ~ 7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD} - 13.5 ~ V_{DD} + 0.3	V
Input Voltage 1	V_{IN1}	- 0.3 ~ V_{DD} + 0.3	V
Input Voltage 2 (V_1-V_6)	V_{IN2}	V_{DD} + 0.3 ~ V_{EE} - 0.3	V
Operating Temperature	T_{OPR}	-30 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +125	°C

Voltage greater than above may damage to then circuit.
V_{EE}: connect protection resistor (220Ω ± 5%)

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD}=2.7~5.5V, V_{DD} - V_{EE} =3~13V, V_{SS}=0V, Ta=-30 ~ +85^{O}C)

Characteristic	Symbol	Test Condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	f_{CL2}=400KHz	-	1	mA	-
Supply Current *	I_{EE}	f_{CL1}=1KHz	-	10	μA	
Input High Voltage	V_{IH}	-	0.7V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2,
Input Low Voltage	V_{IL}		0	0.3V_{DD}		DR1, DR2,
Input Leakage Current	I_{LKG}	V_{IN} =0-V_{DD}	-5	5	μA	SHL1, SHL2, M, FCS
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	V_{DD}-0.4	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	I_{OL} = +0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON}=0.1mA for one of SC1-SC40	-	1.1		V(V_1-V_6), SC(SC_1-SC_{40})
	V_{D2}	I_{ON}=0.5mA for each SC1-SC40	-	1.5		
Leakage Current	I_V	$V_{IH=}$ V_{DD}~ V_{EE} (Output SC1-SC40:floating)	-10	10	μA	V_1-V_6

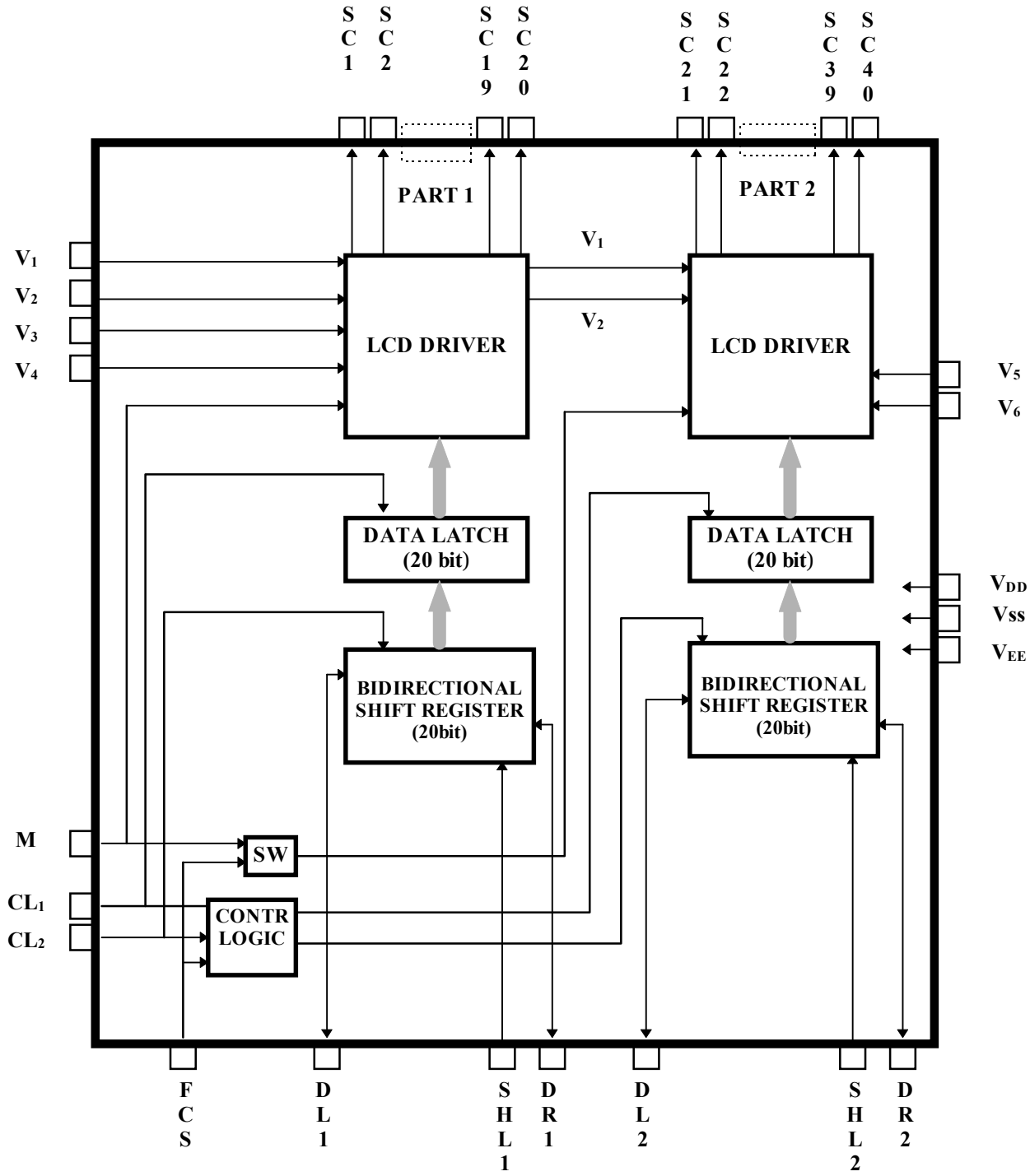
* V_{DD}-V_{EE}=4V

AC characteristics (V_{DD}=2.7~5.5V, V_{DD} - V_{EE} =3~13V, V_{SS}=0V, Ta=-30 ~ +85^{O}C)

Characteristic	Symbol	Test Condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	KHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{LS}	from CL2 to CL1	500	-		CL1, CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DL1, DL2, DR1, DR2,
Data Hold Time	t_{DH}	-	300	-		FLM
Data Delay Time	t_D	CL=15pF	-	500		DL1, DL2, DR1, DR2

Input/Output current excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply,To avoid this, input level must be fixed at «H» or «L».

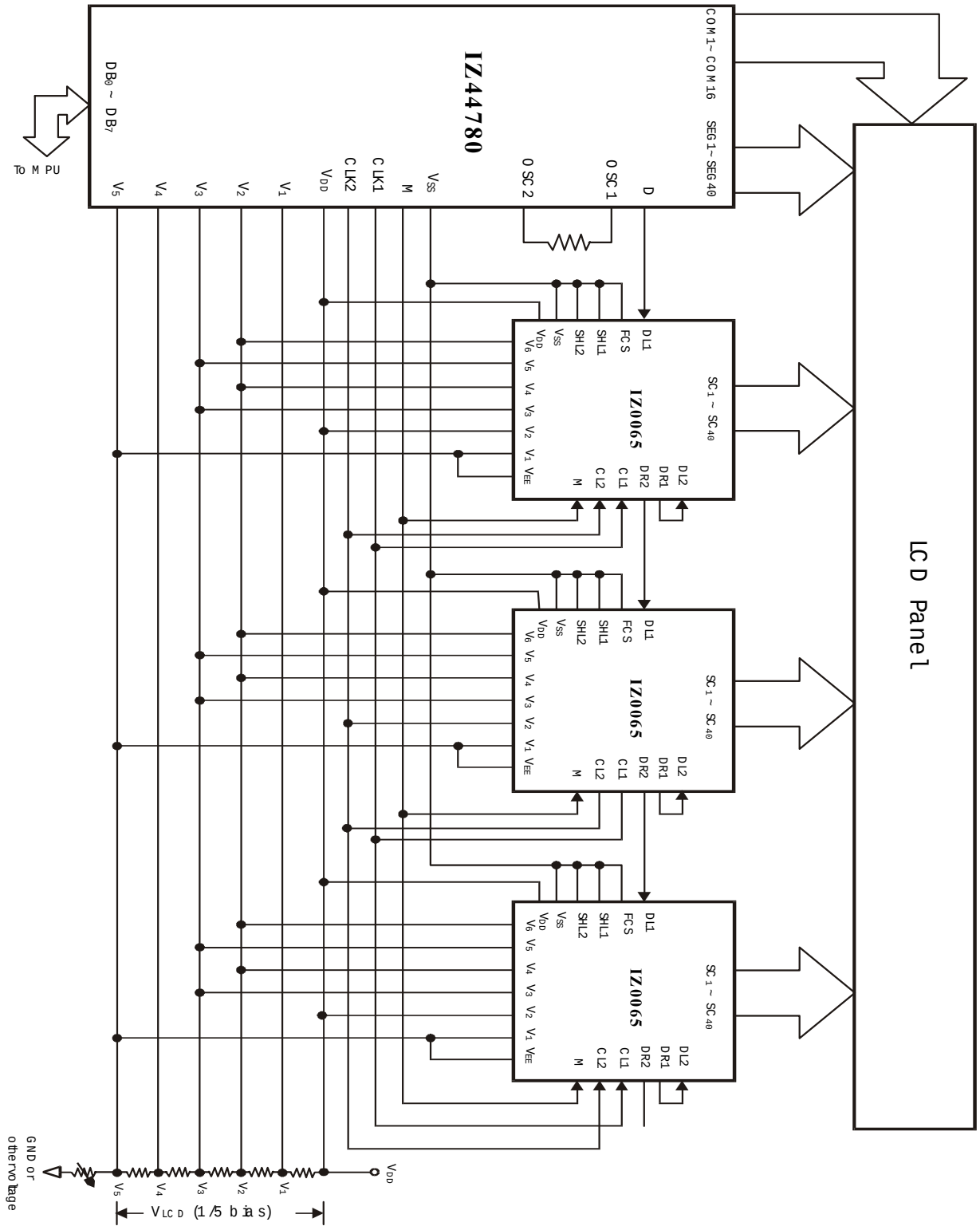
BLOCK DIAGRAM



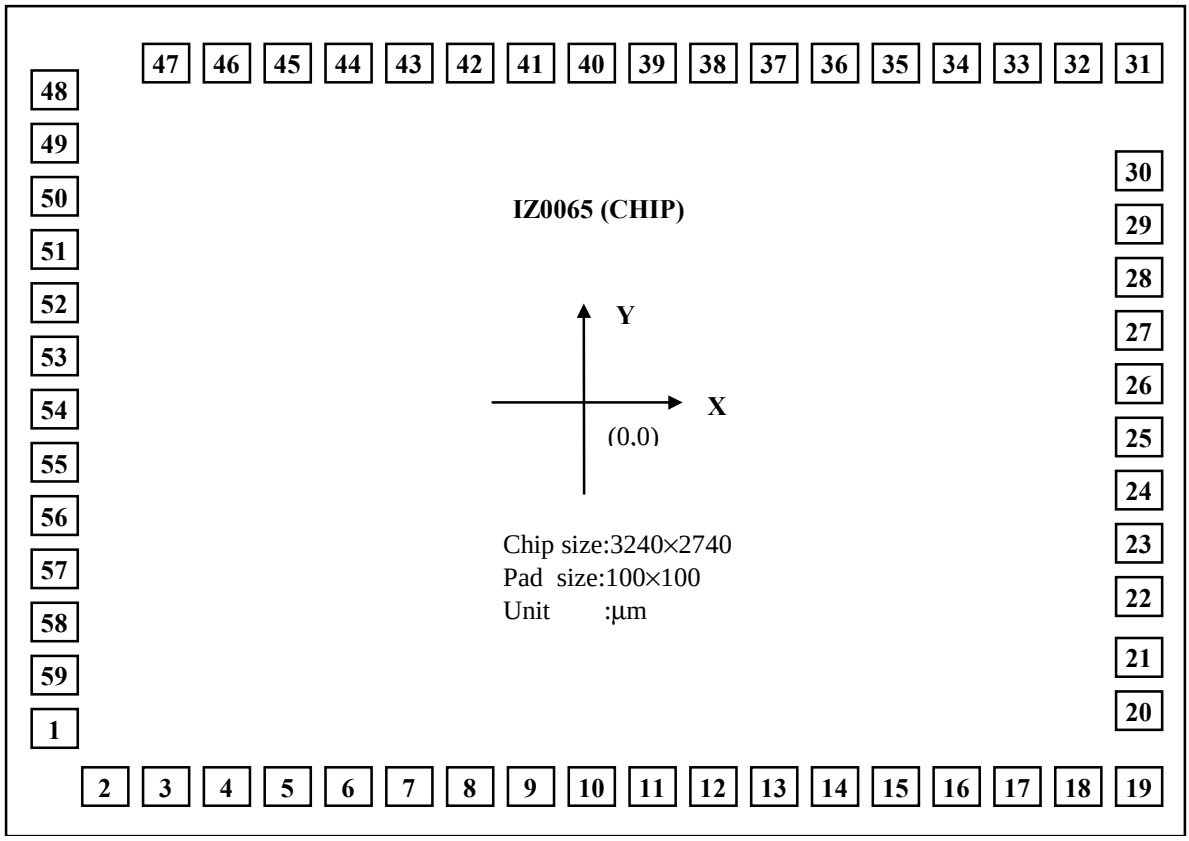
PIN DESCRIPTION

<table>
<tr><th>PIN №</th><th>INP/ OUTP</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTER-FACE</th></tr>
<tr><td>V_{DD} (24)</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (+5 V ± 10%, +3 V ± 10%)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND (34)</td><td>0 V (GND)</td></tr>
<tr><td>V_{EE} (31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit (-5 V)</td></tr>
<tr><td>V_1 V_2 (44,45)</td><td>Input</td><td colspan="2">Bias Voltage</td><td>Bias voltage level for LCD drive (select level)</td><td>Power</td></tr>
<tr><td>SC_1÷SC_{20}</td><td>Output</td><td rowspan="4">PART 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V_3 V_4 (46,47)</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (nonselect level)</td><td>Power</td></tr>
<tr><td>SHL1 (41)</td><td>Input</td><td>Data interface</td><td>Selection of the shift direction of Part 1 shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1,DR1 (35,36)</td><td>Input/ Output</td><td>Data input/output of Part 1 shift register</td><td>Controller or IZ0065</td></tr>
<tr><td>SC_{21}÷ SC_{40}</td><td>Output</td><td rowspan="4">PART 2</td><td>LCD driver</td><td>LCD driver output</td><td></td></tr>
<tr><td>V_5 V_6 (48,49)</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (nonselect level)</td><td>Power</td></tr>
<tr><td>SHL2 (42)</td><td>Input</td><td>Data interface</td><td>Selection of the shift direction of Part 2 shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2,DR2 (37,38)</td><td>Input/ Output</td><td>Data input/output of Part 2 shift register</td><td>Controller or IZ0065</td></tr>
<tr><td>M (40)</td><td>Input</td><td colspan="2">Alternated signal for LCD driver output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polarity</th></tr><tr><td rowspan="2">1</td><td>V_{SS}</td><td rowspan="2">latch clock (⎍↓⎍)</td><td rowspan="2">shift clock (⎍↓⎍)</td><td rowspan="2">M</td></tr><tr><td>V_{DD}</td></tr><tr><td rowspan="2">2</td><td>V_{SS}</td><td rowspan="2">shift clock (⎍↑⎍)</td><td rowspan="2">latch clock (⎍↑⎍)</td><td rowspan="2">$\overline{M}$</td></tr><tr><td>V_{DD}</td></tr></table>Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level , user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.</td><td>Controller</td></tr>
<tr><td>CL1,CL2 (32,33)</td><td>Input</td><td colspan="2">Data shift / latch clock</td></tr>
<tr><td>FCS (43)</td><td>Input</td><td colspan="2">Mode selection</td></tr>
<tr><td>NC(39)</td><td></td><td colspan="2"></td><td>No connection pin</td><td>N.C</td></tr>
</table>

APPLICATION CIRCUIT



PAD DIAGRAM



PAD LOCATION

Pad №	Pad Name	X	Y	Pad №	Pad Name	X	Y	Pad №	Pad Name	X	Y
1	VEE	-1384	-840	21	SC38	1381	-627.5	41	SC18	-185	1135
2	CL1	-1344	-1140	22	SC37	1381	-477.5	42	SC17	-335	1135
3	CL2	-1190	-1140	23	SC36	1381	-327.5	43	SC16	-485	1135
4	VSS	-1002	-1140	24	SC35	1381	-177.5	44	SC15	-635	1135
5	DL1	-852	-1140	25	SC30	1381	-29.5	45	SC14	-785	1135
6	DR1	-702	-1140	26	SC31	1381	120.5	46	SC13	-1033	1135
7	DL2	-552	-1140	27	SC32	1381	270.5	47	SC12	-1183	1135
8	DR2	-402	-1140	28	SC33	1381	420.5	48	SC9	-1384	970
9	M	-252	-1140	29	SC34	1381	570.5	49	SC10	-1384	820
10	SHL1	-102	-1140	30	SC29	1381	720.5	50	SC11	-1384	670
11	SHL2	48	-1140	31	SC28	1380	1135	51	SC8	-1384	520
12	FCS	198	-1140	32	SC27	1232	1135	52	SC7	-1384	370
13	V1	482	-1140	33	SC26	1082	1135	53	VDD	-1384	220
14	V2	632	-1140	34	SC25	932	1135	54	SC6	-1384	70
15	V3	782	-1140	35	SC24	782	1135	55	SC5	-1384	-80
16	V4	932	-1140	36	SC23	632	1135	56	SC4	-1384	-230
17	V5	1082	-1140	37	SC22	482	1135	57	SC3	-1384	-380
18	V6	1232	-1140	38	SC21	332	1135	58	SC2	-1384	-528
19	SC40	1382	-1140	39	SC20	115	1135	59	SC1	-1384	-678
20	SC39	1381	-777.5	40	SC19	-35	1135				