

IZ0066

DOT MATRIX LCD CONTROLLER & DRIVER

The IZ0066 is a dot matrix liquid crystal display controller & driver LSI that displays alphanumeric, characters and symbols.

It drives dot matrix LCD under microcomputer control. All functions needed for dot matrix LCD drive are internally provided on one chip.

FEATURES

- Internal Memory
 - Character Generator ROM: 8320 bits
 - Character Generator RAM: 512 bit
 - Display Data RAM: 80 x 8 bits for 80 digits
- Internal automatic reset circuit at power ON
- Internal oscillation circuit
- Power Supply Voltage: +5V ± 10%
- LCD Driving Voltage for display: 0 ~ -5V(V₅)
- Duty factor selection (selected by programs)
 - 1/8 duty: 5 x 7 dots format 1 line,
 - 1/11 duty: 5 x 10 dots format 1 line
 - 1/16 duty: 5 x 7 dots format 2 line
- Bare chip available
- Pin-to-Pin replacement for KS0066, HD44780, SED1278

FUNCTION

- Character type dot matrix LCD driver & controller
- Internal driver: 16 common and 40 segment signal output
- Display character format: 5 x 7 dots + cursor, 5 x 10 dots + cursor
- Easy interface with a 4-bit or 8-bit MPU
- Display character pattern:
 - 5 x 7 dots format: 192 kinds, 5 x 10 dots format: 32 kinds
- The special character pattern can be programmable by Character Generator RAM directly
- A customer character pattern can be programmable by mask option
- Wide range of instruction function:
 - Display clear, Cursor home, Display ON/OFF, Display shift
 - Cursor ON/OFF, Display character blink, Cursor shift

ORDERING INFORMATION

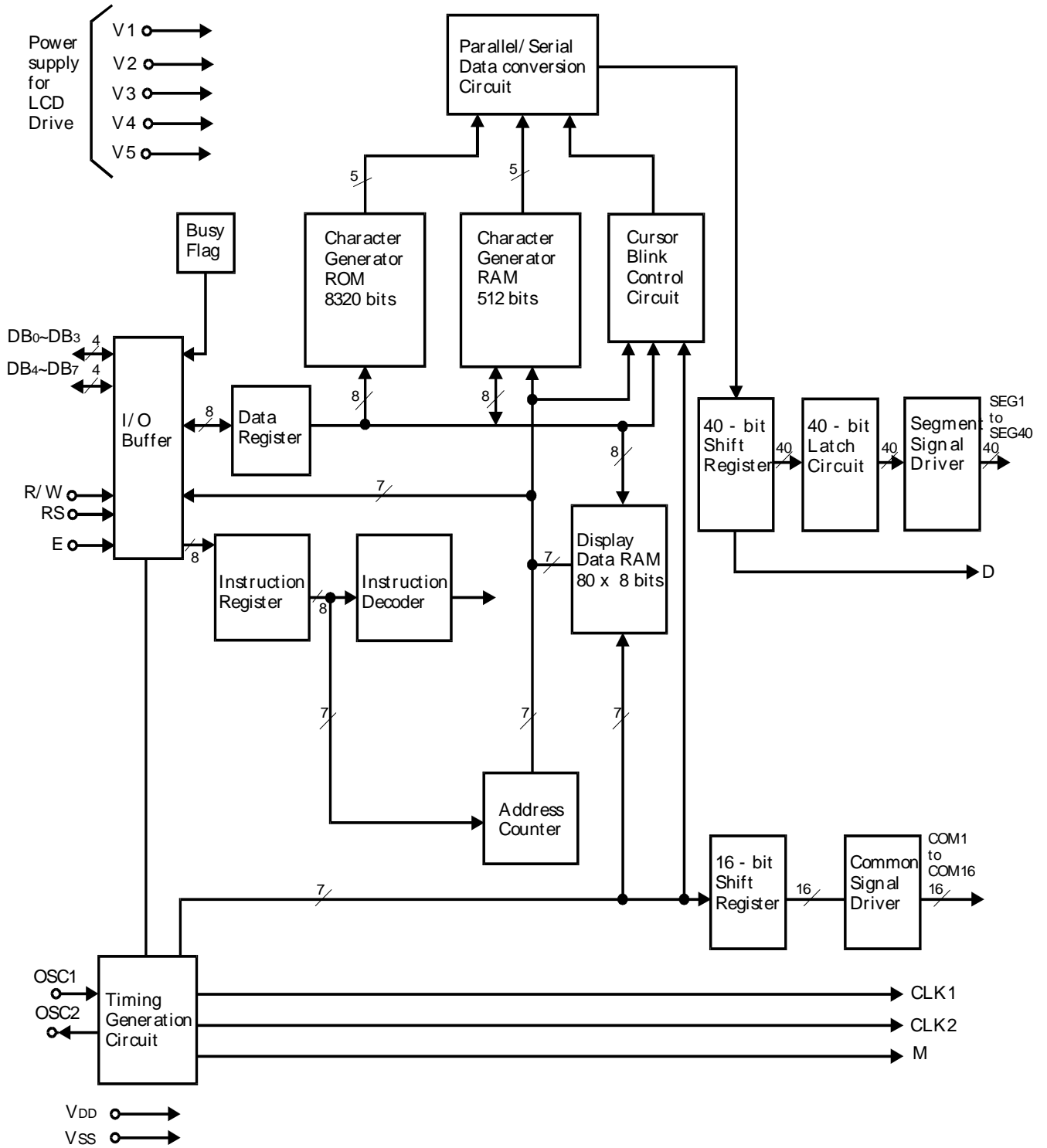
Type	CGROM		
IZ0066 - 00	English	Numeral	Japanese
IZ0066 - 01	English	Numeral	Cyrillic
IZ0066 - XX	Custom font (XX – ROM code)		

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V _{DD}	- 0.3 ~ 7.0	V
Driver Supply Voltage	V ₁ ~ V ₅	V _{DD} - 13.5 ~ V _{DD} + 0.3	V
Input Voltage	V _I	-0.3 ~ V _{DD} + 0.3	V
Operating Temperature	T _a	- 20 ~ + 75	°C
Storage Temperature	T _{stg}	- 55 ~ + 125	°C

Notes: Must keep the relation of V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V₅

BLOCK DIAGRAM

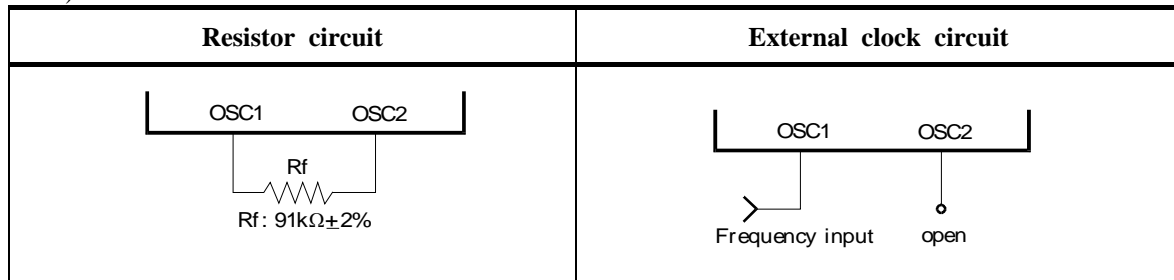


ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{DD} = +5V, V_{SS} = 0V unless otherwise specified)

Characteristic		Symbol	Test Condition		Applicable Terminals	Min	Typ	Max	Unit
Operating Voltage		V _{DD}				4.5		5.5	V
Operating Current (*1)		I _{DD}	Internal oscillation or external clock f _{OSC} = 270KHz				0.35	0.6	
HIGH Input Voltage		V _{IH}			E, DB ₀ ~ DB ₇ , R/W, RS	2.2		V _{DD}	V
					OSC1	V _{DD} -1.0		V _{DD}	
LOW Input Voltage		V _{IL}			E, DB ₀ ~ DB ₇ , R/W, RS	-0.3		0.6	V
					OSC1	-0.2		1.0	
HIGH Output Voltage		V _{OH}	I _{OH} = -0.205 mA		DB ₀ ~ DB ₇	2.4			V
			I _{OH} = -40μA		CLK1, CLK2, M, D	0.9V _{DD}			
LOW Output Voltage		V _{OL}	I _{OL} = 1.2mA		DB ₀ ~ DB ₇			0.4	V
			I _{OL} = 40μA		CLK1, CLK2, M, D			0.1V _D D	
Driver Voltage Descending		V _{COM}	I _O = ± 0.1mA		COM1 ~ COM16			1.0	V
		V _{SEG}			SEG1 ~ SEG40			1.0	
Input Leakage Current		I _{LKG}	V _{IN} = 0V ~ V _{DD}		E	-1		1	μA
Input LOW Current		I _{IL}	V _{CC} = 5V (test pull up R)		RS, R/W, DB ₀ ~ DB ₇	-50	-125	-250	μA
External Clock	Frequency(*1)	f _{EC}			OSC1	125	250	350	KHz
	Duty	DUTY				46	50	55	%
	Rise time	t _r						0.2	μs
	Fall time	t _f						0.2	μs
Internal Clock Frequency(*1)		f _{OSC1}	Rf = 91KΩ ± 2%		OSC1, OSC2	190	270	350	KHz
Ceramic Resonator Oscillation Frequency (*1)		f _{OSC2}				245	250	255	
LCD Driving Voltage (*2)		V _{LCD1}	V _{DD} - V ₅	1/5 bias	V ₁ ~ V ₅	4.6		10.0	V
		V _{LCD2}				1/4 bias	3.0		

Notes: *1). Oscillation circuit



*2). Input the voltage listed in table below to $V_1 \sim V_5$

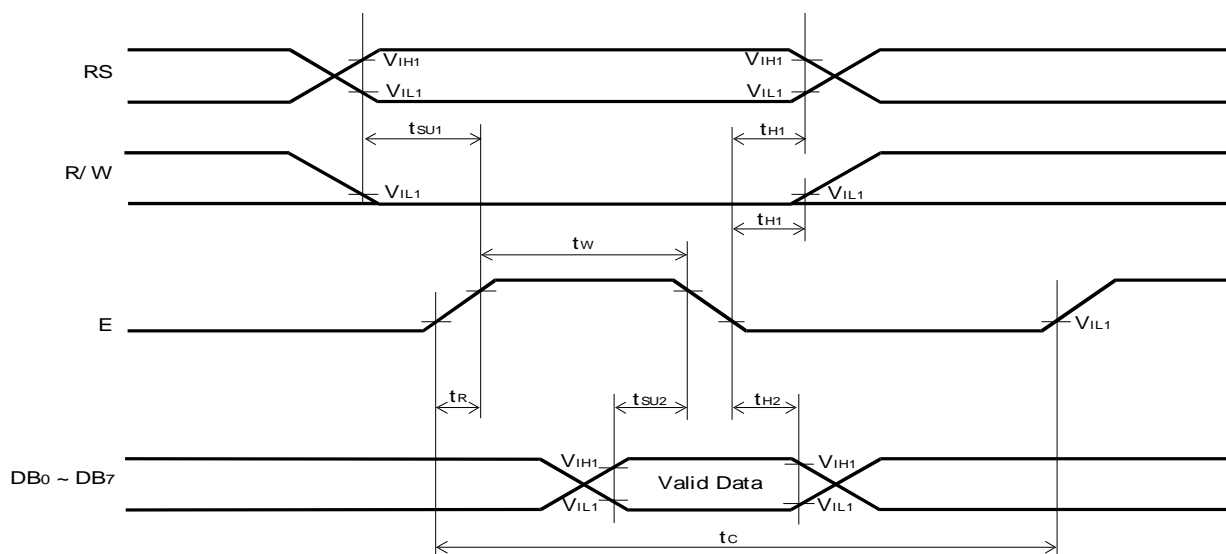
Power supply	Duty	1/8, 1/11	1/16
	Bias	1/4	1/5
V_1		$V_{DD} - V_{LCD}/4$	$V_{DD} - V_{LCD}/5$
V_2		$V_{DD} - V_{LCD}/2$	$V_{DD} - 2V_{LCD}/5$
V_3		$V_{DD} - V_{LCD}/2$	$V_{DD} - 3V_{LCD}/5$
V_4		$V_{DD} - 3V_{LCD}/4$	$V_{DD} - 4V_{LCD}/5$
V_5		$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

* V_{LCD} is the LCD driving voltage, refer to the initial set of the instruction code.

AC CHARACTERISTICS ($V_{DD} = 5V, V_{SS} = 0V, T_a = 25^\circ C$)

(1) Write mode (Writing data from MPU to IZ0066)

Characteristic	Symbol	Test pin	Min	Typ	Max	Unit
E Cycle Time	t_c	E	500			ns
E Rise Time	t_R	E			25	ns
E Fall Time	t_F	E			25	ns
E Pulse Width (High, Low)	t_w	E	220			ns
R/W and RS Set-up Time	t_{SU1}	R/W, RS	40			ns
R/W and RS Hold Time	t_{H1}	R/W, RS	10			ns
Data Set-up Time	t_{SU2}	DB ₀ ~ DB ₇	60			ns
Data Hold Time	t_{H2}	DB ₀ ~ DB ₇	10			ns

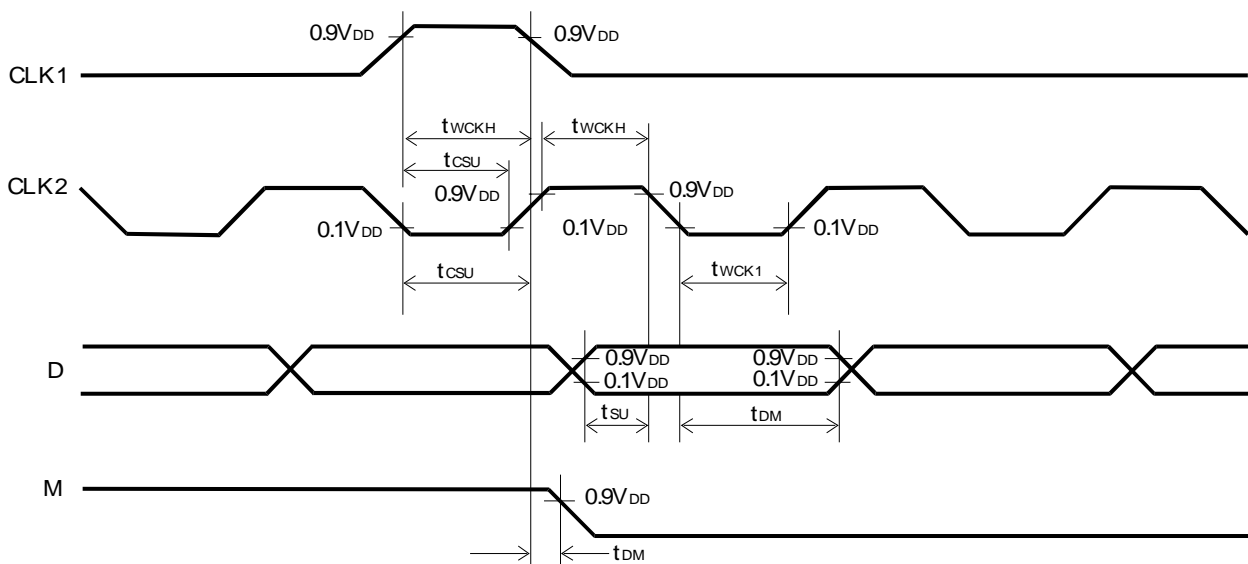


(2) Read mode (Reading data from IZ0066 to MPU)

Characteristic	Symbol	Test pin	Min	Typ	Max	Unit
E Cycle Time	t_C	E	500			ns
E Rise Time	t_R	E			25	ns
E Fall Time	t_F	E			25	ns
E Pulse Width (High, Low)	t_W	E	220			ns
R/W and RS Set-up Time	t_{SU1}	R/W, RS	40			ns
R/W and RS Hold Time	t_{H1}	R/W, RS	10			ns
Data Output Delay Time	t_D	DB ₀ ~ DB ₇			120	ns
Data Hold Time	t_{H2}	DB ₀ ~ DB ₇	20			ns

(3) Interface mode with IZ0065

Characteristic	Symbol	Test pin	Min	Typ	Max	Unit
Clock Pulse Width High	t_{WCKH}	CLK	800			ns
Clock Pulse Width Low	t_{WCKL}	CLK	800			ns
Data Set-up Time	t_{SU}	D	300			ns
Data Hold Time	t_{DH}	D	300			ns
Clock Set-up Time	t_{CSU}	CLK	500			ns
M Delay Time	t_{DM}	M	-1000		1000	ns



TERMINAL DESCRIPTION

Pin	INP/OUT	Name	DESCRIPTION	INTERFACE		
V _{DD}	Power	Operating Voltage	For logical circuit (+5V ± 10%)	Power Supply		
V _{SS}			0V(GND)			
V ₁ – V ₅		Negative Supply Voltage	Bias voltage level for LCD driving			
SEG1–SEG40	Output	Segment output	Segment signal output for LCD driving	LCD		
COM1–COM16	Output	Common output	Common signal output for LCD driving	LCD		
OSC1	Input	Oscillator	Both pin connected to Rf resistor or ceramic resonator for internal oscillator circuit. In case of external frequency use only, the frequency is input to OSC1 terminal.	Resistor or Ceramic Resonator		
OSC2	Output					
CLK1	Output	Data latch clock	Clock output terminal for the serially transferred data to be latched to the driver.	IZ0065		
CLK2		Data shift clock	Clock output terminal used when D terminal data output shifts the inside of the driver.			
M		Alternated signal for LCD driver output	The alternating signal to convert LCD drive waveform to AC.			
D		Display data interface	Character pattern data, which is corresponding to each common signal, is supplied to driver serially.			
					High	Selection
					Low	Non selection
E	Input	Enable	Start enable signal to read or write the data	MPU		
R/W		Read/Write	R/W signal input is used to select the read/write mode			
					High	Read mode
				Low	Write mode	
RS		Register select	Register selection input			
					High	Data register (for read and write)
					Low	Instruction register (for write), Busy flag, address counter (for read)
DB ₀ – DB ₇	Input/Output	Data interface	Used for data transfer between the MPU and IZ0066. These terminals are for data bus with bidirectional three-state. Initial 4 bit (DB ₀ -DB ₃) are not used during 4 bit operation (DB ₇ can be used as a busy flag)			

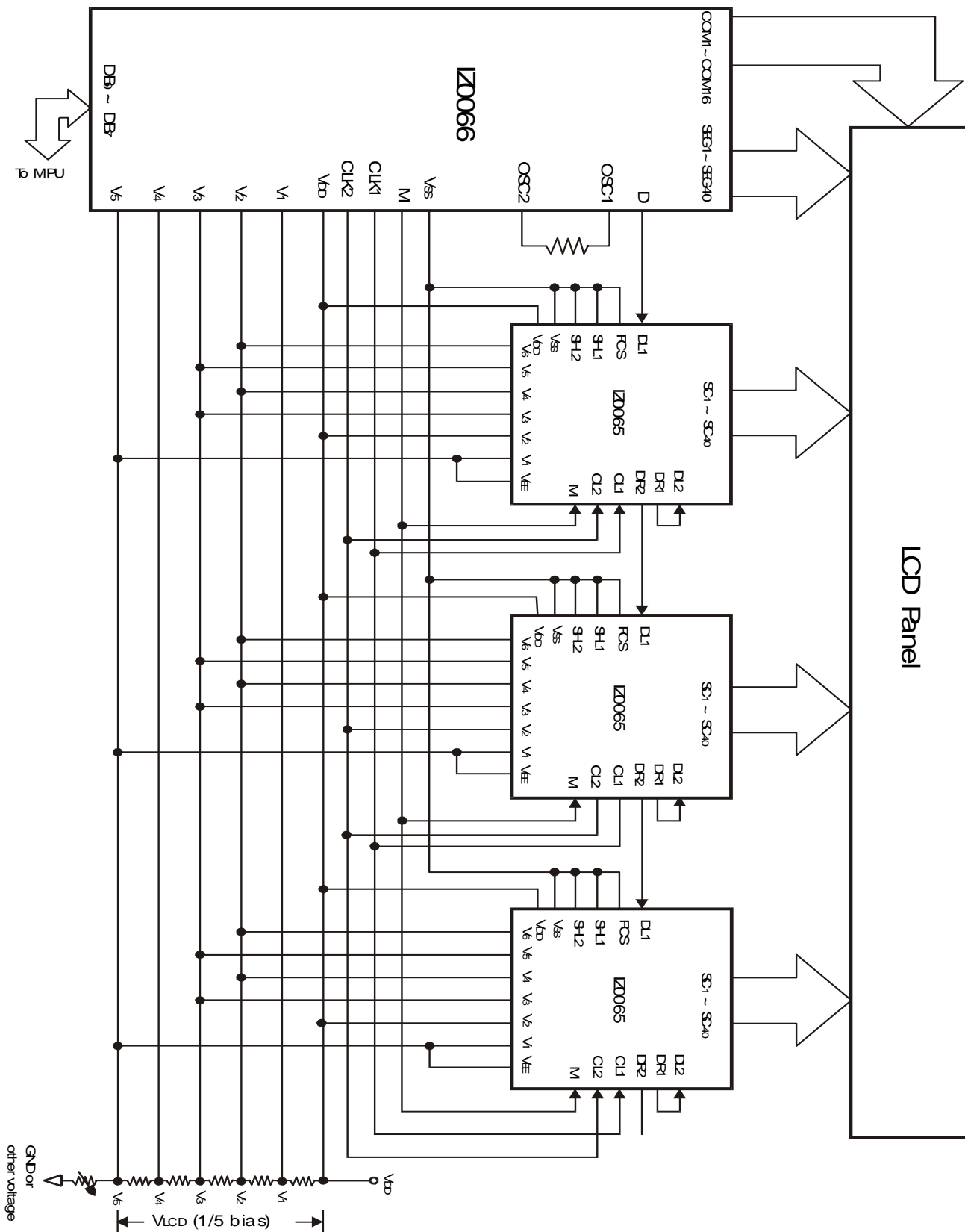
CONTROL AND DISPLAY COMMANDS

Command	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	Execution time (f _{osc} =250KHz)	Remark															
DISPLAY CLEAR	L	L	L	L	L	L	L	L	L	H	1.64 ms																
RETURN HOME	L	L	L	L	L	L	L	L	H	X	1.64 ms	Cursor move to first digit															
ENTRY MODE SET	L	L	L	L	L	L	L	H	I/D	SH	40μs	<p>*I/D: set cursor move direction</p> <table border="1"> <tr> <td rowspan="2">I/D</td> <td>H</td> <td>Increase</td> </tr> <tr> <td>L</td> <td>Decrease</td> </tr> </table> <p>*SH: Specifies shift of display</p> <table border="1"> <tr> <td rowspan="2">SH</td> <td>H</td> <td>Display is shifted</td> </tr> <tr> <td>L</td> <td>Display is not shifted</td> </tr> </table>	I/D	H	Increase	L	Decrease	SH	H	Display is shifted	L	Display is not shifted					
I/D	H	Increase																									
	L	Decrease																									
SH	H	Display is shifted																									
	L	Display is not shifted																									
DISPLAY ON/OFF	L	L	L	L	L	L	H	D	C	B	40μs	<p>*Display</p> <table border="1"> <tr> <td rowspan="2">D</td> <td>H</td> <td>Display on</td> </tr> <tr> <td>L</td> <td>Display off</td> </tr> </table> <p>*Cursor</p> <table border="1"> <tr> <td rowspan="2">C</td> <td>H</td> <td>Cursor on</td> </tr> <tr> <td>L</td> <td>Cursor off</td> </tr> </table> <p>*Blinking</p> <table border="1"> <tr> <td rowspan="2">B</td> <td>H</td> <td>Blinking on</td> </tr> <tr> <td>L</td> <td>Blinking off</td> </tr> </table>	D	H	Display on	L	Display off	C	H	Cursor on	L	Cursor off	B	H	Blinking on	L	Blinking off
D	H	Display on																									
	L	Display off																									
C	H	Cursor on																									
	L	Cursor off																									
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SHIFT	L	L	L	L	L	H	S/C	R/L	X	X	40μs	<table border="1"> <tr> <td rowspan="2">SC</td> <td>H</td> <td>Display shift</td> </tr> <tr> <td>L</td> <td>Cursor move</td> </tr> </table> <table border="1"> <tr> <td rowspan="2">R/L</td> <td>H</td> <td>Right shift</td> </tr> <tr> <td>L</td> <td>Left shift</td> </tr> </table>	SC	H	Display shift	L	Cursor move	R/L	H	Right shift	L	Left shift					
SC	H	Display shift																									
	L	Cursor move																									
R/L	H	Right shift																									
	L	Left shift																									

Command	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	Executi on time (f _{osc} =2 50KHz)	Remark															
SET FUNCTIO N	L	L	L	L	H	DL	N	F	X	X	40µs	<table border="1"> <tr> <td rowspan="2">DL</td> <td>H</td> <td>8 bits interface</td> </tr> <tr> <td>L</td> <td>4 bits interface</td> </tr> </table> <table border="1"> <tr> <td rowspan="2">N</td> <td>H</td> <td>2 line display</td> </tr> <tr> <td>L</td> <td>1 line display</td> </tr> </table> <table border="1"> <tr> <td rowspan="2">F</td> <td>H</td> <td>5x10 dots</td> </tr> <tr> <td>L</td> <td>5x7 dots</td> </tr> </table>	DL	H	8 bits interface	L	4 bits interface	N	H	2 line display	L	1 line display	F	H	5x10 dots	L	5x7 dots
DL	H	8 bits interface																									
	L	4 bits interface																									
N	H	2 line display																									
	L	1 line display																									
F	H	5x10 dots																									
	L	5x7 dots																									
SET CG RAM ADDRESS	L	L	L	H	CG RAM address (corresponds to cursor address)					40µs	CG RAM Data is sent and received after this setting																
SET DD RAM ADDRESS	L	L	H	DD RAM address					40µs	DD RAM Data is sent and received after this setting																	
READ BUSY FLAG & ADDRESS	L	H	BF	Address Counter used for Both DD & CG RAM address					0µs	<table border="1"> <tr> <td rowspan="2">BF</td> <td>H</td> <td>Busy</td> </tr> <tr> <td>L</td> <td>Ready</td> </tr> </table> -Reads BF indication internal operating is being performed. -Reads address counter contents	BF	H	Busy	L	Ready												
BF	H	Busy																									
	L	Ready																									
WRITE DATA	H	L	Write Data					46µs	Write data DD or CG RAM																		
READ DATA	H	H	Read Data					46µs	Read data from DD or CG RAM																		

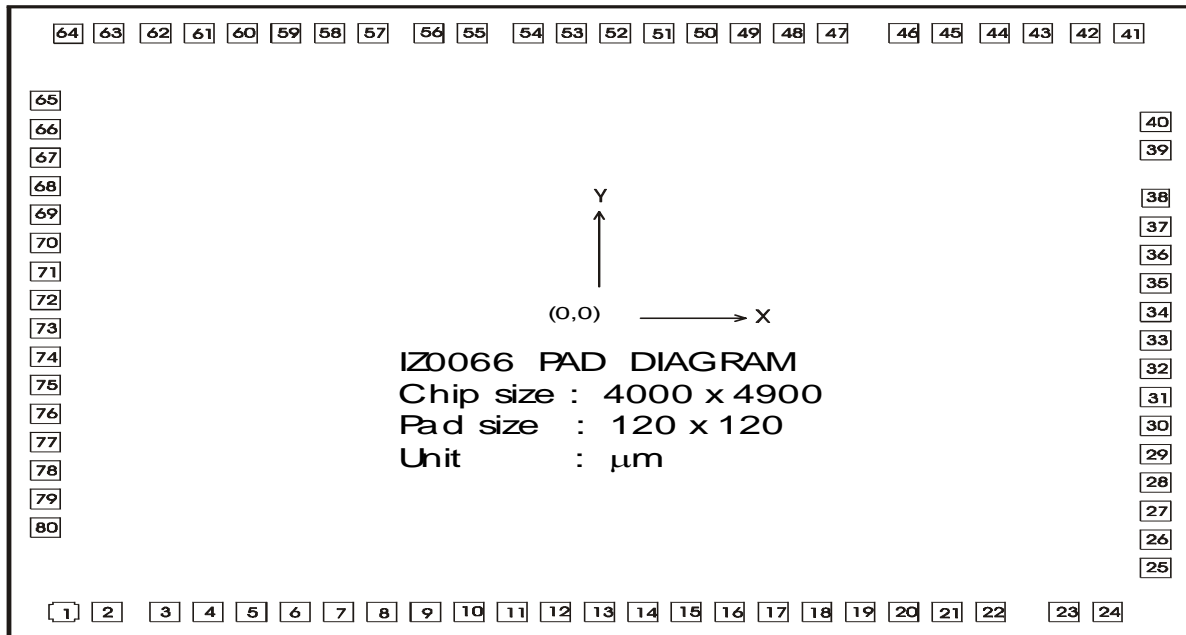
Note: X – Don't care.

APPLICATION CIRCUIT



When IZ0065 is externally connected to the IZ0066, you can increase the number of display digits up to 80 characters.

PAD DIAGRAM



The chip substrate is connected to V_{DD} .

PAD LOCATION

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG22	-2221	-1830	28	V3	2299	-1012	55	COM9	-530	1830
2	SEG21	-2041	-1830	29	V4	2299	-832	56	COM10	-710	1830
3	SEG20	-1804	-1830	30	V5	2299	-862	57	COM11	-941	1830
4	SEG19	-1624	-1830	31	CL1	2299	-472	58	COM12	-1121	1830
5	SEG18	-1444	-1830	32	CL2	2299	-292	59	COM13	-1301	1830
6	SEG17	-1264	-1830	33	V_{CC}	2299	-112	60	COM14	-1481	1830
7	SEG16	-1084	-1830	34	M	2299	68	61	COM15	-1661	1830
8	SEG15	-904	-1830	35	D	2299	248	62	COM16	-1841	1830
9	SEG14	-724	-1830	36	RS	2299	428	63	SEG40	-2036	1830
10	SEG13	-544	-1830	37	R/W	2299	608	64	SEG39	-2216	1830
11	SEG12	-364	-1830	38	E	2299	788	65	SEG38	-2298	1404
12	SEG11	-184	-1830	39	DB0	2299	1090	66	SEG37	-2298	1224
13	SEG10	-4	-1830	40	DB1	2299	1270	67	SEG36	-2298	1044
14	SEG9	176	-1830	41	DB2	2188	1830	68	SEG35	-2298	864
15	SEG8	35	-1830	42	DB3	2008	1830	69	SEG34	-2298	684
16	SEG7	536	-1830	43	DB4	1812	1830	70	SEG33	-2298	504
17	SEG6	716	-1830	44	DB5	1632	1830	71	SEG32	-2298	324
18	SEG5	896	-1830	45	DB6	1436	1830	72	SEG31	-2298	144
19	SEG4	1076	-1830	46	DB7	1256	1830	73	SEG30	-2298	-36
20	SEG3	1256	-1830	47	COM1	961	1830	74	SEG29	-2298	-216
21	SEG2	1436	-1830	48	COM2	781	1830	75	SEG28	-2298	-396
22	SEG1	1616	-1830	49	COM3	601	1830	76	SEG27	-2298	-576
23	GND	1920	-1830	50	COM4	421	1830	77	SEG26	-2298	-756
24	OSC1	2100	-1830	51	COM5	241	1830	78	SEG25	-2298	-936
25	OSC2	2299	-1552	52	COM6	61	1830	79	SEG24	-2298	-1116
26	V1	2299	-1372	53	COM7	-119	1830	80	SEG23	-2298	-1296
27	V2	2299	-1192	54	COM8	-299	1830				