

POWER LOGIC 8-BIT SHIFT REGISTER

(functional equivalent of TPIC6B595 «Texas Instruments» USA)

Description

The IZ6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for usage as power driver of inductance coil of relays, solenoids, and other medium-current or high-voltage loads

The device performs following functions:

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_c = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection.

The IZ6B595 is characterized for operation over the operating case temperature range of -40°C to 125°C .

Main features:

- Supply voltage $U_{CC}=5 \text{ V} \pm 10 \%$;
- Open state driver resistance $\leq 8 \text{ Ohm}$ for 350 mA current;
- Leakage current $I_{DSX} < 5,0 \mu\text{A}$ (for switching 40 V voltage);
- Continuous drain current, each output, all outputs on 150 mA (Peak drain current 500 mA)
- Single-pulse avalanche energy dissipated each drain, $E_{AS} = 30 \text{ mJ}$ (for switching off 500mA current in inductance coil 0,2 H);
- Breakdown avalanche voltage, $U_{(BR)DSX} > 50 \text{ V}$
- Operating temperature range, $-40 \dots +125^\circ\text{C}$;
- ESD 750 V.

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Table1 – Contact pad description

Contact pad number	Symbol	Description
01	TEST1	Testing pad
02	U_{cc}	Power supply
03	SERIN	Data input
04	DRAIN0	Highvoltage driver output
05	DRAIN1	Highvoltage driver output
06	DRAIN2	Highvoltage driver output
07	DRAIN3	Highvoltage driver output
08	SRCLR_L	Reset input
09	G_L	Driver closed state setup input
10	GND	Common
11	GND	Common
12	GND	Common
13	RCK	Latch data input
14	SRCK	Clock
15	DRAIN4	Highvoltage driver output
16	DRAIN5	Highvoltage driver output
17	DRAIN6	Highvoltage driver output
18	DRAIN7	Highvoltage driver output
19	SEROUT	Data output
20	GND	Common
21	TEST2	Testing pad
Notes		
1 Contact pads 01 and 21 (TEST1 и TEST2) are purposed for testing of ICs by manufacturer only and are not used (connected) in customer devices.		
2 Contact pads 10, 11, 12, 20 (GND) are connected together		



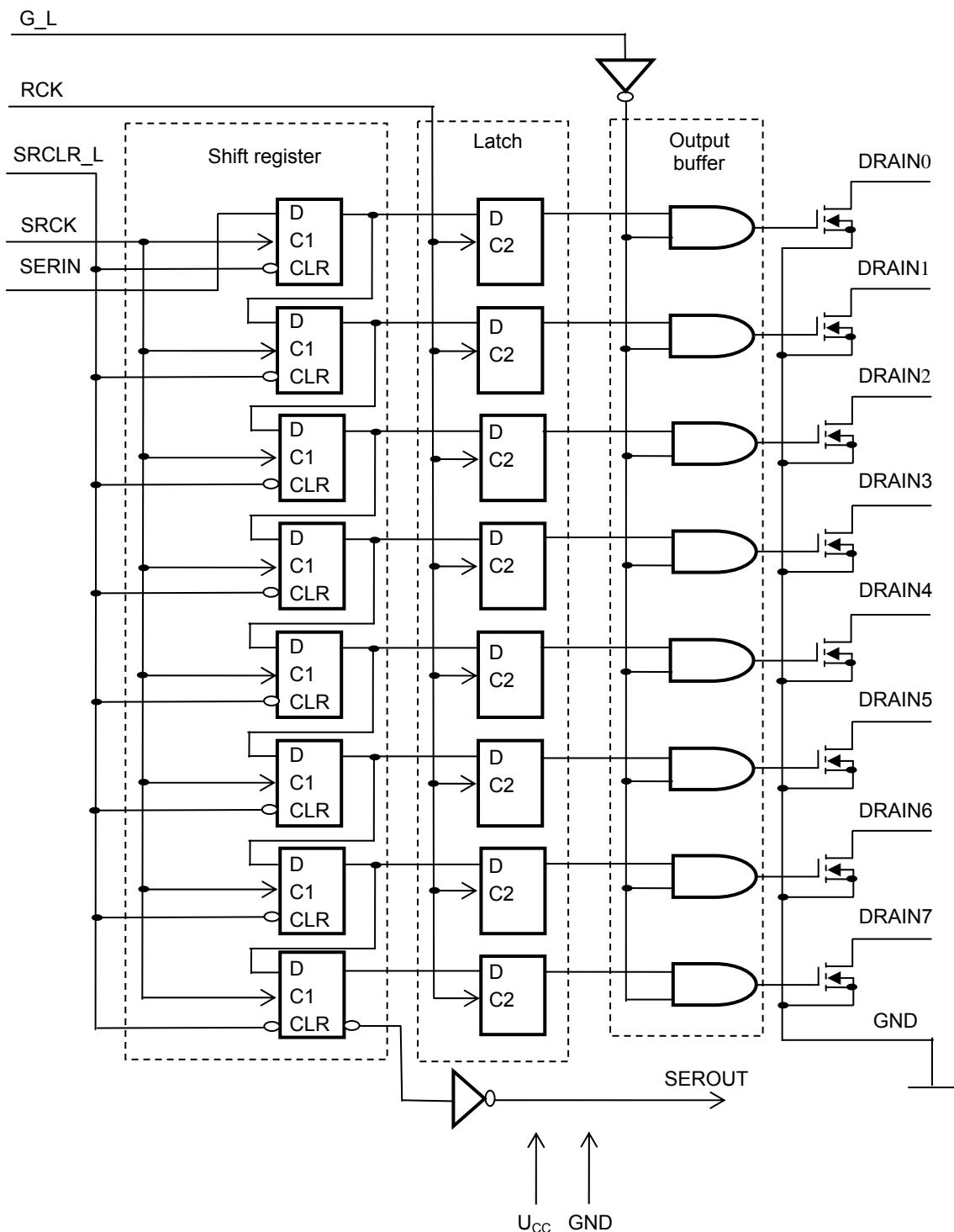


Fig 1 – Block diagram

Table 2 – Recommended operation modes

Symbol	Parameter	Value		Unit
		Min	Max	
U_{CC}	Supply voltage	4,5	5,5	V
U_{IL}	Low level input voltage	-0,3	0,15 U_{CC}	V
U_{IH}	High level input voltage	0,85 U_{CC}	$U_{CC}+0,3$	V
U_{DS}	Output driver drain-to-source voltage	-	40	V

Table 3 – Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
U_{CC}	Supply voltage	-	7,0	V
U_{IL}	Low level input voltage	-0,5	-	V
U_{IH}	High level input voltage	-	7,0	V
U_{DS}	Output driver drain-to-source voltage	-	50	V
I_{FC}	Forward-biased diode constant output current DRAIN0–DRAIN7	-	-500	mA
I_{FP}	Pulsed diode output current DRAIN0–DRAIN7	-	-1 *	A
I_{DP}	Pulsed drain output current DRAIN0–DRAIN7 (all drivers are open, $T_a=(25\pm10)$ °C)	-	500 *	mA
I_{DC}	Constant drain output current DRAIN0–DRAIN7 (all drivers are open, $T_a=(25\pm10)$ °C)	-	150	mA
I_{DM}	Peak drain current single output DRAIN0–DRAIN7	-	500 *	mA
E_{AS}	Single-pulse avalanche energy DRAIN0–DRAIN7	-	0,03	J
I_{AS}	Avalanche current DRAIN0–DRAIN7	-	500	mA

* Mode duration not more 100 us, mode spacing not less 5 ms



Table 4 – Electric parameters Ta -40 ... +125 °C

Symbol	Parameter	Mode	Value		Ambient temperature, °C	Unit
			Min	Max		
$U_{(BR)DSX}$	Drain-to-source breakdown voltage, DRAIN0-DRAIN7	$U_{CC} = 5,0 \text{ V}$ $I_D = 1 \text{ mA}$	<u>50</u> 45	-	<u>25±10</u> -40, 125	V
$I_{(BR)DSX}$	Drain current (drivers are closed), DRAIN0–DRAIN7	$U_{CC} = 5,0 \text{ V}$ $U_{DS} = 50 \text{ V}$	-	1	<u>25±10</u> -40, 125	mA
		$U_{CC} = 5,0 \text{ V}$ $U_{DS} = 45 \text{ V}$				
U_{DS}	Source-to-drain diode forward voltage DRAIN0–DRAIN7	$ I_F = 100 \text{ mA}$	-	<u> -1,0 </u> -1,5	<u>25±10</u> -40, 125	V
U_{OH1}	High level output voltage, SEROUT	$U_{CC}=4,5 \text{ V}$ $I_{OH1}= -0,02 \text{ mA}$	<u>4,4</u> 4,3	-		V
U_{OH2}	High level output voltage, SEROUT	$U_{CC}=4,5 \text{ V}$ $I_{OH2}= -4,0 \text{ mA}$	<u>4,0</u> 3,8	-		V
U_{OL1}	Low level output voltage, SEROUT	$U_{CC}=4,5 \text{ V}$ $I_{OL1}=0,02 \text{ mA}$	-	<u>0,1</u> 0,2		V
U_{OL2}	Low level output voltage, SEROUT	$U_{CC}=4,5 \text{ V}$ $I_{OL2}=4,0 \text{ mA}$	-	<u>0,5</u> 0,7		V
I_{IH}	High level input current	$U_{CC}=5,5 \text{ V}$ $U_{IH}=5,5 \text{ V}$	-	<u>1,0</u> 1,5		uA
I_{IL}	Low level input current	$U_{CC}=5,5 \text{ V}$ $U_{IL}=0 \text{ V}$	-	<u> -1,0 </u> -1,5		uA
I_{CC1}	Consumption current (drivers are closed),	$U_{CC}=5,5 \text{ V}$	-	<u>100</u> 150		uA
I_{CC2}	Consumption current (drivers are open),	$U_{CC}=5,5 \text{ V}$	-	<u>300</u> 450		uA



Table 4 (continued)

Symbol	Parameter	Mode	Value		Ambient temperature, °C	Unit
			Min	Max		
I_{occ}	Operation consumption current (drivers are closed)	$U_{CC}=5,5\text{ V}$ $f_{SRCK}= 1\text{ MHz}$ $C_L=30\text{ pF}$	-	<u>1,0</u> 1,5	<u>25±10</u> -40, 125	mA
I_{occ1}	Operation consumption current (drivers are closed)	$U_{CC}=5,5\text{ V}$ $f_{SRCK}= 5\text{ MHz}$ $C_L=30\text{ pF}$	-	<u>5,0</u> 7,5		mA
I_{DSX}	Drain current (drivers are closed) DRAIN0–DRAIN7	$U_{CC} = 5,5\text{ V}$ $U_{DS} = 40\text{ V}$	-	<u>5,0</u> 8,0		uA
R_{DS1}	Drain-source resistance DRAIN0–DRAIN7 (drivers are open)	$U_{CC}= 4,5\text{ V}$ $I_{DS1}= 100\text{ mA}$	-	<u>5,7</u> 9,5		Ohm
R_{DS2}	Drain-source resistance DRAIN0–DRAIN7 (drivers are open)	$U_{CC}= 4,5\text{ V}$ $I_{DS2}= 350\text{ mA}$	-	<u>8</u> 15		Ohm

Operation description

The device is an 8-bit register with serial data input and parallel data output. If reset input of shift register SRCLR_L is in low state, all bits of shift register are switched to low state. High level state on SRCLR_L input enable serial data input to shift register.

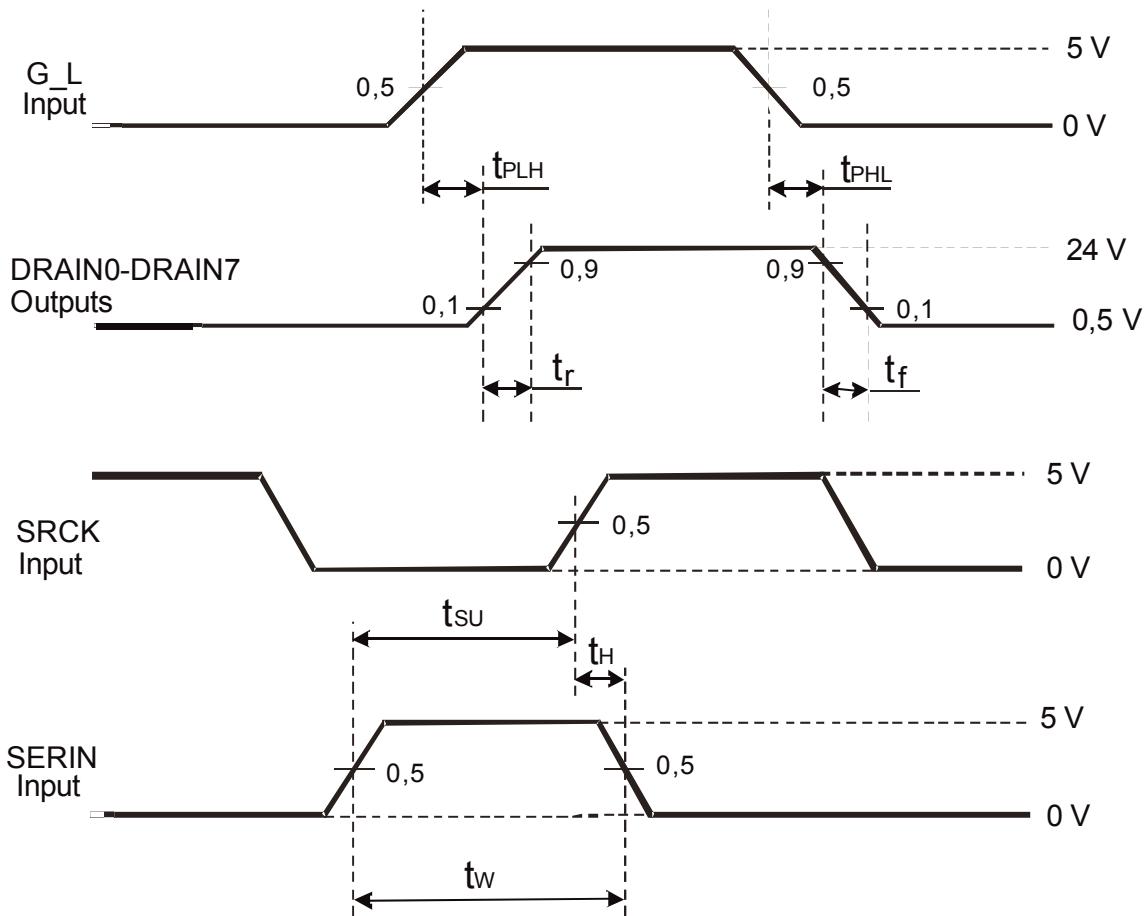
Data are loading to shift register on leading edge of clock signal SRCK, at that data on SERIN input are written to first bit, to all other bits data stored in previous bit are transferred to next. SEROUT output is in state that correspond to data written to eight bit of shift register and can be used for ICs cascading.

Data from shift register can be written to latch on leading edge of RCK signal.

If high level is applied to G_L (driver set up) input, all bits of output buffer are holding in low level state and all outputs of driver are closed.

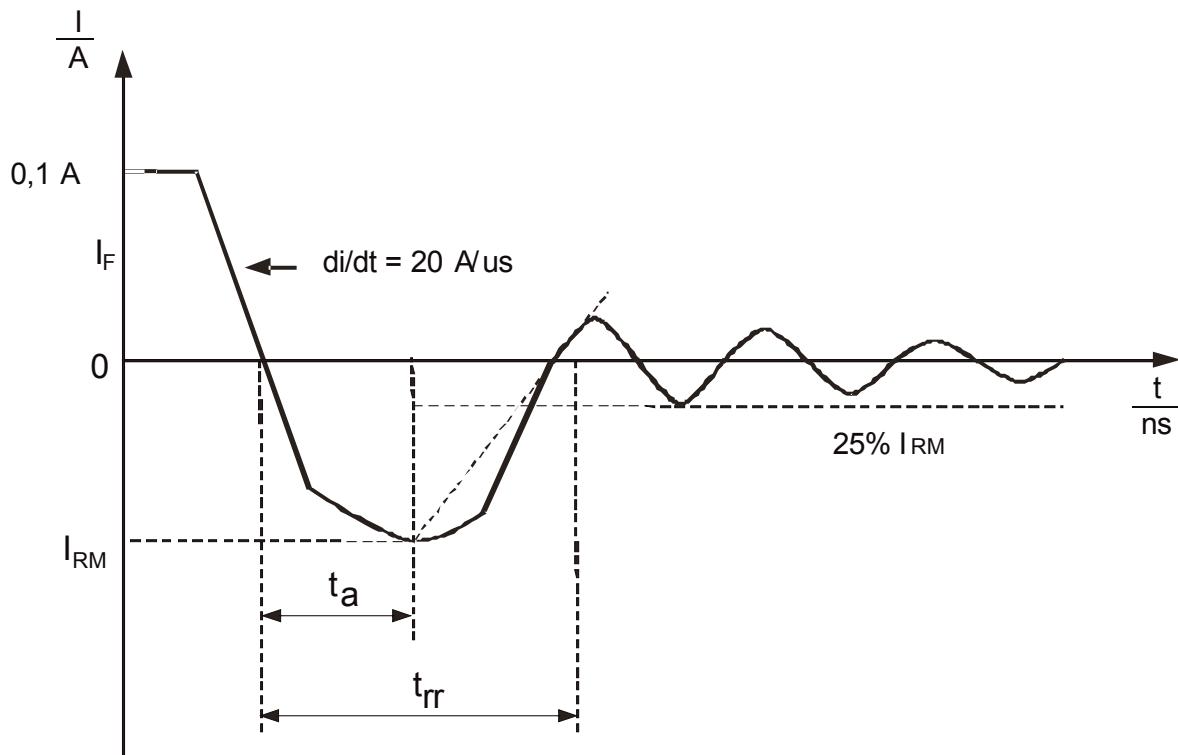
If low level is applied to G_L input, data stored in latch are transferred to output buffer, and if bits of output buffer are switched to high state, correspondent to them drivers will be open.



**Fig. 2 – Timing diagram****Table 5 - Switching Parameters** $U_{CC}=5\text{ V}$, $T_a=(25\pm 10)\text{ }^\circ\text{C}$; output driver load $C_L=30\text{ pF}$, $R_L=235\text{ Ohm}$; $U_{DS}=24\text{ V}$

Parameter, unit	Symbol	Norm		
		Min.	Typ.	Max.
Propagation delay time, low-to-high-level, ns	t_{PHL}	-	85	-
Propagation delay time, high-to-low-level, ns	t_{PLH}	-	202	-
Rise time, (drain output), ns	t_r	-	200	-
Fall time (drain output), ns	t_f	-	110	-
SERIN input signal duration , ns	t_W	40	-	-
Data setup time, ns	t_{SU}	20	-	-
Data hold time, ns	t_H	20	-	-





I_F – diode direct current

I_{RM} – maximum diode reverse current

Fig. 3 – Reverse-recovery-current time t_a and reverse-recovery-current rise time t_{rr} timing diagram

Table 6 - **Switching Parameters** $U_{CC}=5 V$, $T_a=(25\pm 10) ^\circ C$

Parameters, unit	Symbol	Typical value
Reverse-recovery-current time, ns	t_a	90
Reverse-recovery-current rise time, ns	t_{rr}	210



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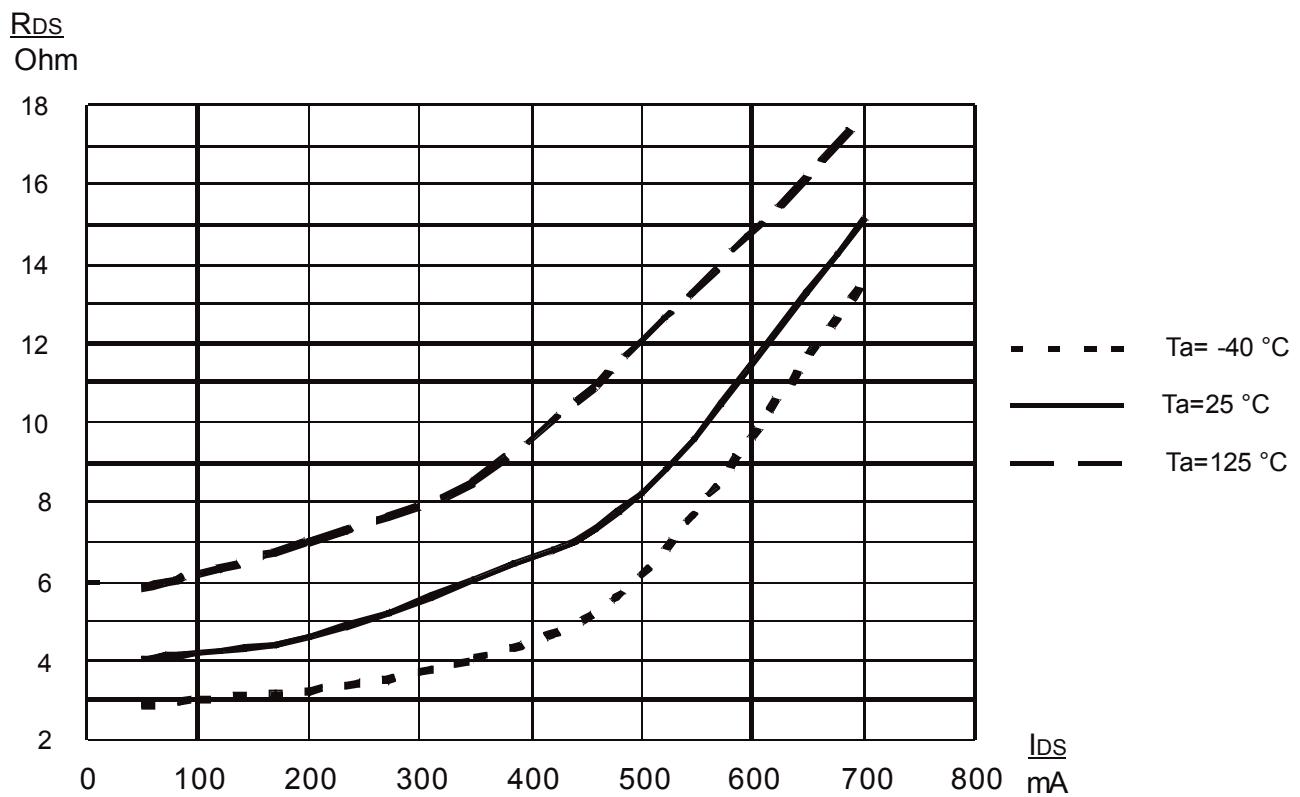


Fig. 4 – Typical drain-source resistanse R_{DS} of DRAIN0-DRAIN7 outputs (drivers are open) vs drain current I_{DS} ($U_{CC} = 5,0\text{ V}$)

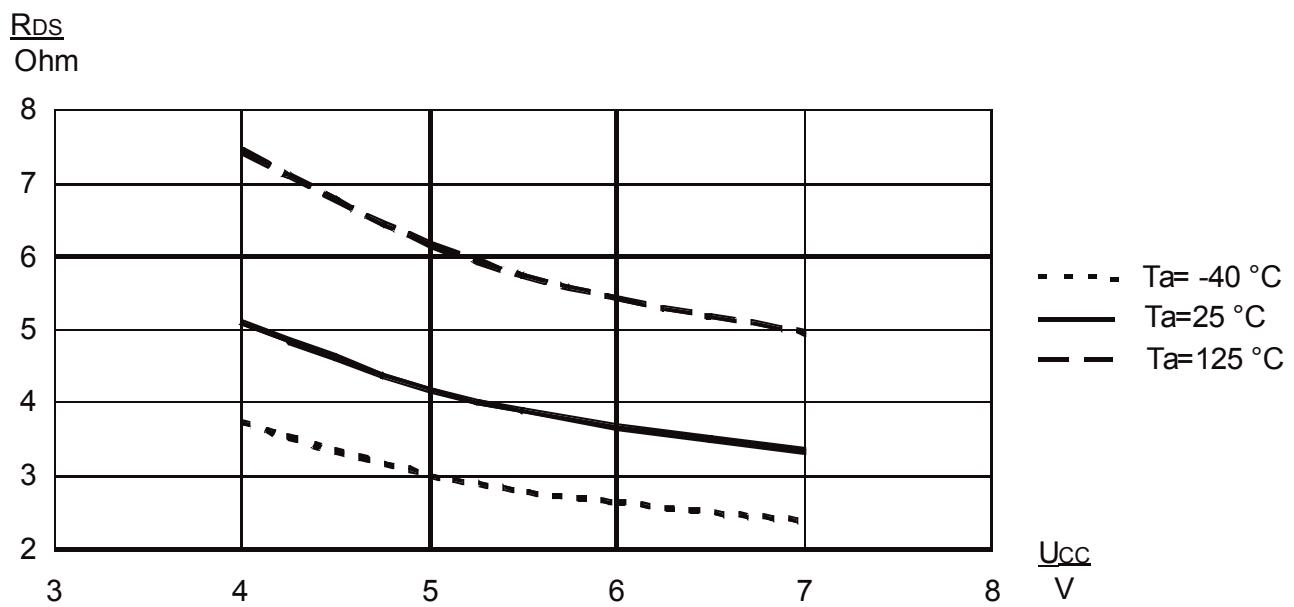


Fig. 5 – Typical drain-source resistanse R_{DS} of DRAIN0-DRAIN7 outputs (drivers are open) vs supply voltage U_{CC} ($I_{DS} = 100\text{ mA}$)

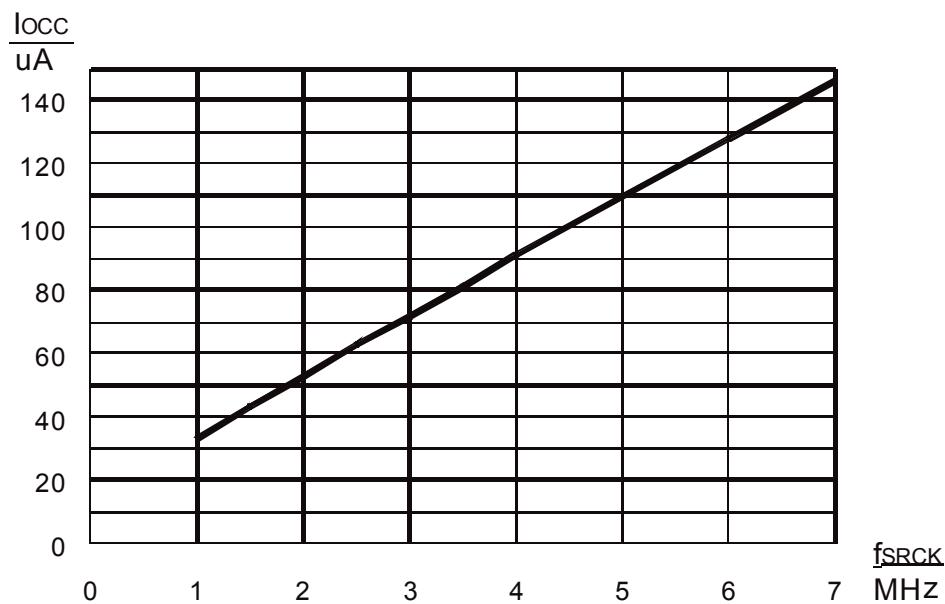


Fig. 6 – Typical operation consumption current I_{OCC} vs frequuency f_{SRCK} ($U_{CC} = 5,5V$; $T_a = (25 \pm 10)^\circ C$)

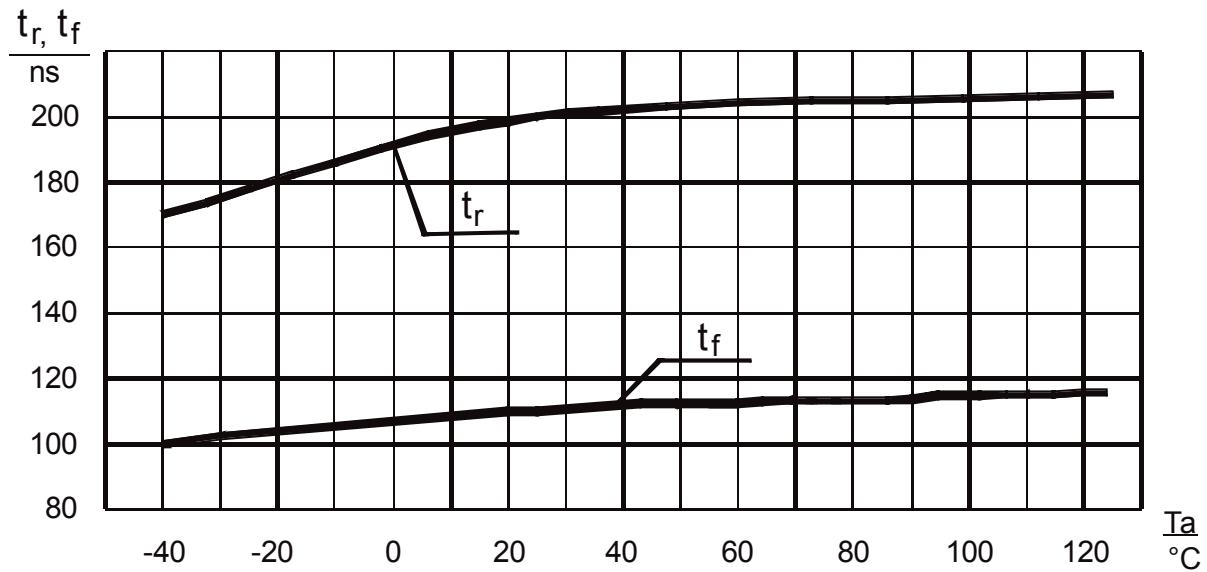


Fig. 7 – Typical signal rise time t_r and typical fall time t_f for DRAIN0-DRAIN7 output vs ambient temperature T_a ($U_{CC} = 5,0 V$, $C_L = 30 pF$, $R_L = 235$ Ohm, $U_{DS} = 24$ V)

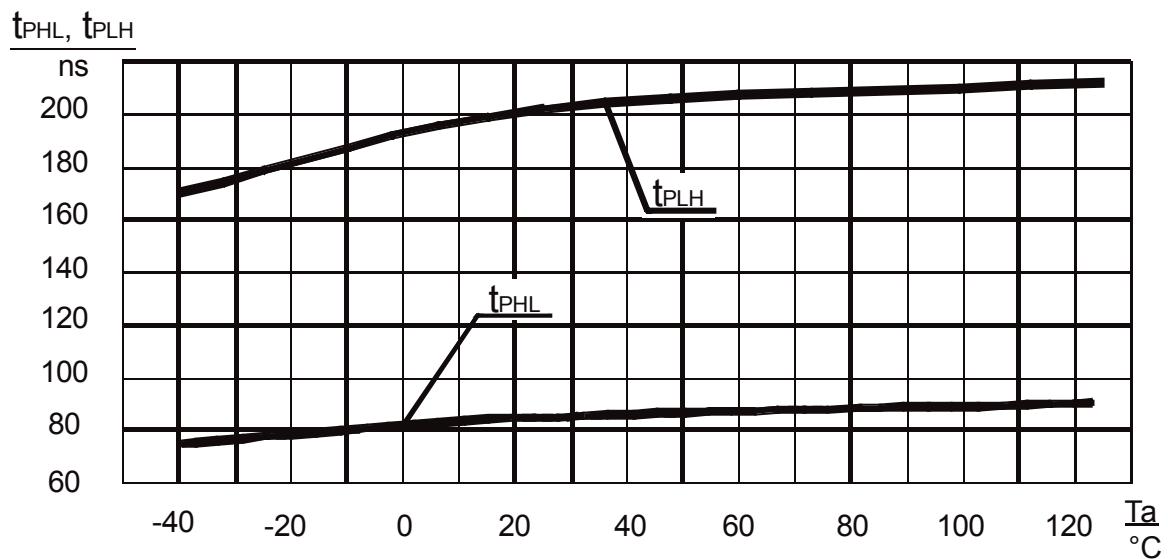
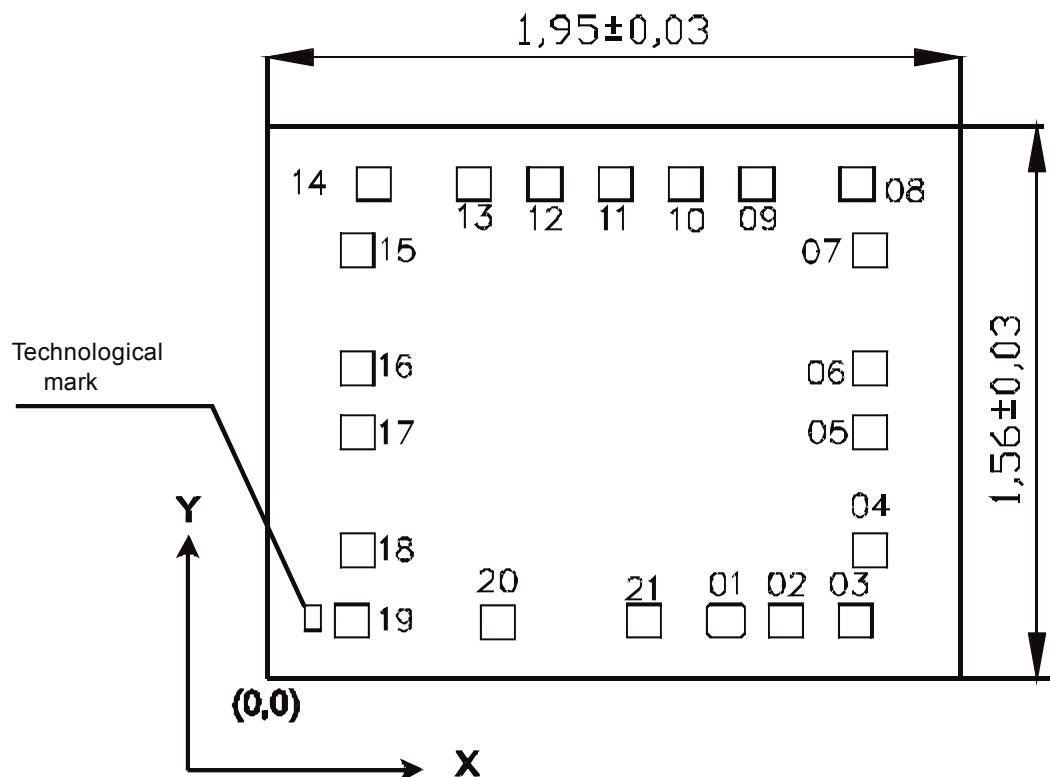


Fig 8 – Typical propagation delay times high to low t_{PHL} and low to high t_{PLH} on DRAIN0-DRAIN7 outputs vs ambient temperature T_a ($U_{CC} = 5,0 \text{ V}$, $C_L = 30 \text{ pF}$, $R_L = 235 \text{ Ohm}$, $U_{DS} = 24\text{V}$)

Contact pad location diagram

ICs are shipped on not sawed wafers.
IC weight is not more than 0,003 g.



Die thickness $0,460 \pm 0,022$ mm.

Technological mark 6B595.1 coordinates $x=0,105, y=0,140$ (left bottom corner)

Fig. 9 – Pad location diagram

Table 7 – Contact pad coordinates and size

Contact pad number	Coordinates (left bottom corner), mm	
	X	Y
01	1,0340	0,1145
02	1,4120	0,1145
03	1,6090	0,1145
04	1,6510	0,3135
05	1,6510	0,6480
06	1,6510	0,8275
07	1,6510	1,1620
08	1,6125	1,3505
09	1,3305	1,3505
10	1,1290	1,3505
11	0,9320	1,3505
12	0,7335	1,3505
13	0,5330	1,3505
14	0,2510	1,3505
15	0,2040	1,1620
16	0,2040	0,8275
17	0,2040	0,6480
18	0,2040	0,3135
19	0,1890	0,1145
20	0,6015	0,1145
21	0,8200	0,1145

NOTE – CONTACT PAD COORDINATES AND SIZE 0,095 X 0,095 mm ARE INDICATED UNDER «PASSIVATION» LAYER

