8-BIT MICROCONTROLLER WITH LCD DRIVER

IZ7008 is one-chip 8-bit microcontroller made by CMOS technology. The microcontroller is multi-purpose and can be used in electronic watch, data acquisition systems, control systems. Low consumption power and full static CMOS logic allow to use MC in independent systems with limited energy consumption.
Technical characteristics of IZ7008:

ALU bit capacity	**– 8 bits**
RAM size	**– 40 bytes**
ROM size	**– 1,5 K of commands (16–bit instructions)**
RISC commands system	**– 30 types of commands**
Stack depth	**– 7 levels**
Interrupter	**– from 8- inputs and three timers**
Maximum number of the controlled LCD segments	**– 128 (32 LCD control drivers at multiplex levels 1/2,1/3,1/4)**

Operation temperature range -20°C to +70 °C.

INTEGRAL

Electrical parameters at 1.5V supply

Absolute maximum and maximum ratings

Parameter, unit	Symbol	Maximum ratings		Absolute maximum ratings	
		Value		Value	
		min	max	min	max
Primary supply voltage from voltage source, V	U_{CC1}	1,2	1,8	-0,3	2,0
Secondary supply voltage, V	U_{CC2}	$2U_{CC1}$-0,3	$2U_{CC1}$	-0,3	4,0
High input voltage, V	U_{IH}	U_{CC1}-0,3	U_{CC1}	-0,3	U_{CC1}+0,3
Low input voltage, V	U_{IL}	Uss	Uss+0,3	-0,3	U_{CC1}+0,3

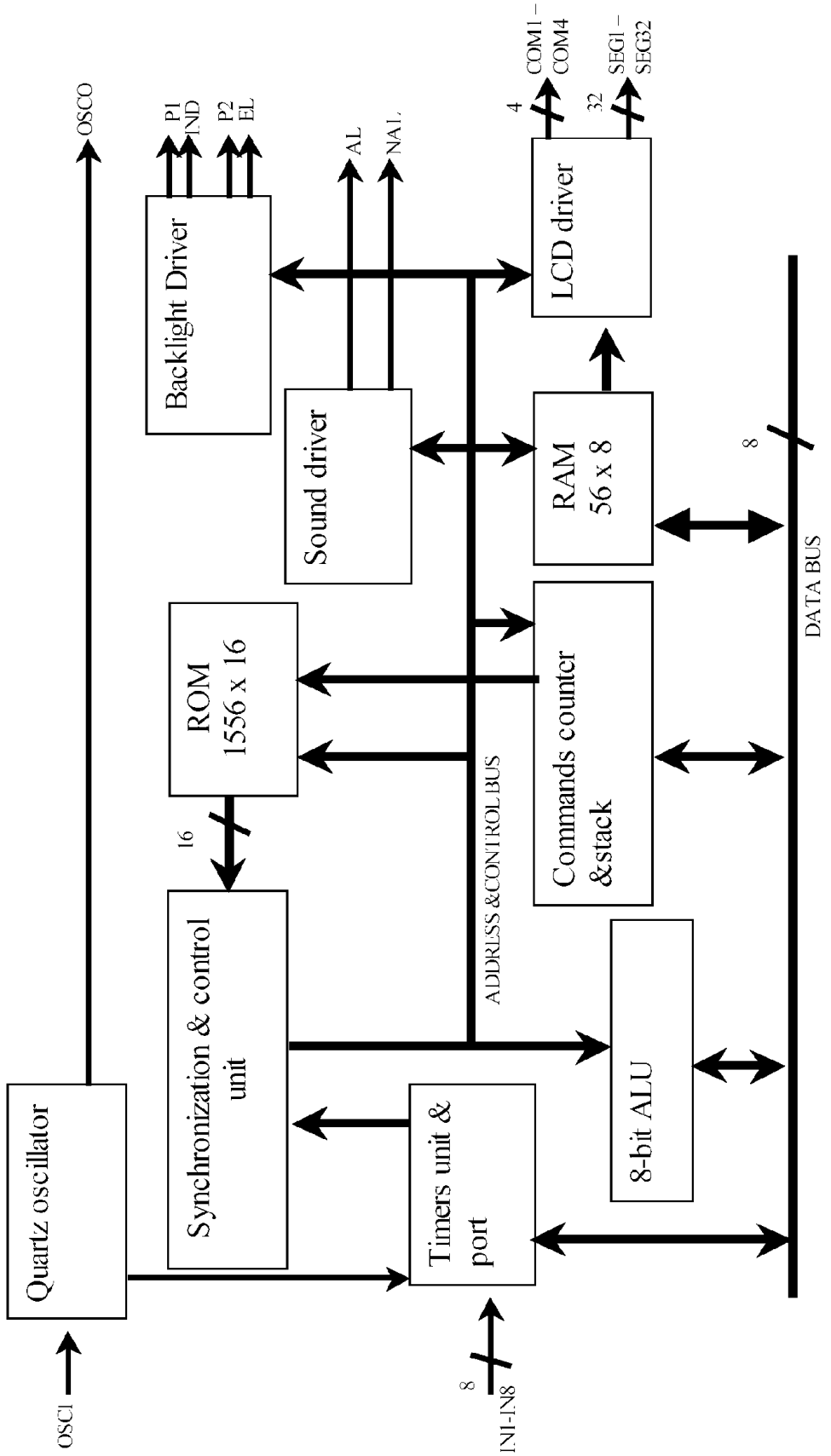
Cycle of command execution is not more than 150 mks at supply voltage 1.2V, and 100 mks at supply voltage 1.5V.

IC operation is not guaranteed under absolute maximum conditions, it's guaranteed under maximum conditions.

Electrical parameters (Ta = 25°C)

Parameter, unit	Symbol	Test conditions	Value		Note
			min	max	
Low output voltage on alarm-clock output, V	U_{OL}	U_{CC1}=1.2V I_{OL}=200mkA		0.2	
High output voltage on alarm-clock output, V	U_{OH}	U_{CC1}=1.2V I_{OH}=-200mkA	1.0		
Dynamic consumption current in shutdown conditions, mkA	I_{CC0}	U_{CC1}=1,5V	-	1,3	1,2
Low input current on buttons inputs, mkA	I_{IL}	U_{CC1}=1,8V U_{IL}=0,3V	-	10	
Oscillator start-up voltage, V	Uosc	Control time 3 sec	-	1,35	2
Oscillator supression voltage, V	Uosp	-	-	1,2	2
Notes: 1 Dynamic consumption current should be measured without load. 2 The parameters are controlled with oscillator crystal with oscillator nominal frequency 32768 Hz at capacitance values on oscillator input OSCI not more than 6pF, on output OSCO - not more than 3pF. 3 Nominal value of integrated capacitances on outputs OSCI and OSCO - 12pF and 12pF(crystal load capacity C_L=6 pF).					

MICROCONTROLLER BLOCK DIAGRAM



INTEGRAL

MICROCONTROLLER STRUCTURE

ROM

Internal ROM contains 1536 commands (16–bit instructions) at the addresses from 0x000 to 0x5FF. ROM area in the range from 0x000 to 0x0FF (256 commands) and from 0x3FE to 0x4A8 (178 commands) is reserved for interruptions processing programs, system reset and microcontroller testing. User's program if mainly located at the addresses from 0x100 to 0x3FD and from 0x4AA to 0x5FF (1110 commands).

MICROCONTROLLER REGISTER RAM

RAM is organized as banks by 8 registers and contains internal function registers, data RAM, special registers and data memory, directly displayed on LCD.

Microcontroller internal function registers are in the address area from 0x000 to 0x007 (bank 00). Their purpose:

R0, R1, R2, R3 - accumulators;

R4, R5, R6 - base address registers BL, BM, BH of storing number of addressed bank;

R7- register of microcontroller state (RGS).

Internal data RAM (RAM) of 40 bytes is in the address space from 0x008 to 0x02F (banks 01, 02, 03, 04, 05).

RAM registers addressing.

RO-R3, R4 (or BL), R5 (or BM), R6 (or BH), R8-R1F - names of RAM registers in the commands at direct addressing. For registers RO-R7 only direct addressing is possible. For registers R8-RF (or L0-L7), R10-R17 (or M0-M7), R18-R1F (or H0-H7) direct addressing is possible only if bit 0 in state register RGS (R7) is reset into 0, i.e. (R7_0)=0.

BL, BM, BH – base address registers (R4, R5, R6 respectively). At index register addressing the contents of base registers defines data bank number. At index addressing of RAM registers the contents of base registers defines data bank number.

L0-L7, M0-M7, H0-H7 – names of RAM registers in commands at index addressing. For names of registers LO-L7 data bank number is defined by contents of base register BL, for names of registers MO-M7 data bank number is defined by contents of base register BM, for names of registers HO-H7 data bank number is defined by contents of base register BH. To calculate physical address, the contents of base register indicated in the command should be multiplied by 8 and a number from 0 to 7 should be added respectively. For example: when recording in the command «M5» the physical address is equal to ((BM)*8+5).

Allocation of RAM and internal function registers addresses

Bank	N of register in the bank	Address	Symbol at direct addressing	Symbol at index addressing	Description
00	0	0x000	R0	-	Accumulator
	1	0x001	R1	-	Accumulator
	2	0x002	R2	-	Accumulator
	3	0x003	R3	-	Accumulator
	4	0x004	R4 or BL	-	Base register BL
	5	0x005	R5 or BM	-	Base register BM
	6	0x006	R6 or BH	-	Base register BH
	7	0x007	R7	-	State register
01	0	0x008	R8 или L0	L0,M0,H0	Data RAM
	1	0x009	R9 или L1	L1,M1,H1	
	2	0x00A	RA или L2	L2,M2,H2	
	3	0x00B	RB или L3	L3,M3,H3	
	4	0x00C	RC или L4	L4,M4,H4	
	5	0x00D	RD или L5	L5,M5,H5	
	6	0x00E	RE или L6	L6,M6,H6	
	7	0x00F	RF или L7	L7,M7,H7	
02	0	0x010	R10 илиM0 M7	L0,M0,H0	Data RAM
	1	0x011	R11 илиM1	L1,M1,H1	
	2	0x012	R12 илиM2	L2,M2,H2	
	3	0x013	R13 илиM3	L3,M3,H3	
	4	0x014	R14 илиM4	L4,M4,H4	
	5	0x015	R15 илиM5	L5,M5,H5	
	6	0x016	R16 илиM6	L6,M6,H6	
	7	0x017	R17 илиM7	L7,M7,H7	
03	0	0x018	R18 илиH0	L0,M0,H0	Data RAM
	1	0x019	R19 илиH1	L1,M1,H1	
	2	0x01A	R1A илиH2	L2,M2,H2	
	3	0x01B	R1B илиH3	L3,M3,H3	
	4	0x01C	R1C илиH4	L4,M4,H4	
	5	0x01D	R1D илиH5	L5,M5,H5	
	6	0x01E	R1E илиH6	L6,M6,H6	
	7	0x01F	R1F илиH7	L7,M7,H7	
04	0	0x020	-	L0,M0,H0	Data RAM
	1	0x021	-	L1,M1,H1	
	2	0x022	-	L2,M2,H2	
	3	0x023	-	L3,M3,H3	
	4	0x024	-	L4,M4,H4	
	5	0x025	-	L5,M5,H5	
	6	0x026	-	L6,M6,H6	
	7	0x027	-	L7,M7,H7	
05	0	0x028	-	L0,M0,H0	Data RAM
	1	0x029	-	L1,M1,H1	
	2	0x02A	-	L2,M2,H2	
	3	0x02B	-	L3,M3,H3	
	4	0x02C	-	L4,M4,H4	
	5	0x02D	-	L5,M5,H5	
	6	0x02E	-	L6,M6,H6	

	7	0x02F	-	L7,M7,H7

Index addressing is possible for all registers (except RO-R7) at setting bit 0 into 1 in the state register RGS (R7), i.e. at (R7_0)=1.

State register RGS (register R7 with address 0x007).

Bit	Symbol	Description and function	State at supply switch.
R7_7	MFR1	1 – masking of setting into 1 of interruption request flag FR1 on timer 1 cleaning	0
R7_6	FR3	Interruption request flag from timer 3 (set into 1 on timer cleaning front)	0
R7_5	FR2	Interruption request flag from timer 2 (set into 1 on timer cleaning front)	0
R7_4	FR1	Interruption request flag from timer 1 (set into 1 on timer cleaning front)	0
R7_3	SVD	1 – at supply voltage less than reference	0
R7_2	SVD/LAMP ON	0- switching-off supply voltage detector 1- switching-on supply voltage detector	0
R7_1	AL_EN	0 –sound inhibit (fixing output OUT_AL into 0) 1 – applying on output OUT_AL frequency 4096 Hz under tune off mode or note frequency in tune foramtion mode	0
R7_0	INDEX	0 –RAM index addressing inhibit, enable direct addressing of registers R8-R1F 1 – enable RAM index addressing, inhibit direct addressing of registers R8-R1F	0

Memory of data, displayed on LCD of maximum size 128 bits is located in address space from 0x7E8 to 0x7F7 (banks FD, FE). For LCD memory only index addressing is possible. Configuration of LCD memory at multiplexing level at 1/4 is shown in the figure

Bank	№	Address	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	COM
FD	0	0x7E8	SEG02	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	Com 1
	1	0x7E9	SEG02	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	Com 2
	2	0x7EA	SEG02	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	Com 3
	3	0x7EB	SEG02	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	Com 4
	4	0x7EC	SEG01	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	Com 1
	5	0x7ED	SEG01	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	Com 2
	6	0x7EE	SEG01	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	Com 3
	7	0x7EF	SEG01	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	Com 4
FE	0	0x7E0	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	SEG17	Com 1
	1	0x7E1	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	SEG17	Com 2
	2	0x7E2	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	SEG17	Com 3
	3	0x7E3	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	SEG17	Com 4
	4	0x7E4	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	SEG18	Com 1
	5	0x7E5	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	SEG18	Com 2
	6	0x7E6	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	SEG18	Com 3
	7	0x7E7	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	SEG18	Com 4

When multiplex level is 1/3 registers with addresses 0x7EB , 0x7EF, 0x7F3, 0x7F7 can be used as data memory, and when multiplex level is 1/2 additionally as data memory can be used the registers with addresses 0x7EA , 0x7E, 0x7F2, 0x7F6.

TIMERS UNIT AND PORT

System registers of timers unit have the addresses 0x7D8- 0x7DD (bank FB), of input-output unit have the addresses 0x7E0- 0x7E4 (bank FC). For system registers only index addressing is possible.

Bank	N	Address	Description	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	W/R
FB	0	0x7D8	Timers control register	IN1 T3	IN0 T3	IN1 T2	IN0 T2	CLR T3	CLR T2	EN T3	EN T2	W/R
	1	0x7D9	Timer T1	T1_7	T1_6	T1_5	T1_4	T1_3	T1_2	T1_1	T1_0	R
	2	0x7DA	Timer T2	T2_7	T2_6	T2_5	T2_4	T2_3	T2_2	T2_1	T2_0	R
	3	0x7DB	Timer T3	T3_7	T3_6	T3_5	T3_4	T3_3	T3_2	T3_1	T3_0	R
	4	0x7DC	Setting register T2	KT2_7	KT2_6	KT2_5	KT2_4	KT2_3	KT2_2	KT2_1	KT2_0	W/R
	5	0x7DB	Setting register T3	KT3_7	KT3_6	KT3_5	KT3_4	KT3_3	KT3_2	KT3_1	KT3_0	W/R
FC	0	0x7E0	Register settings PORT 1-4	M1 Setting	M0 PORT4	M1 Setting	M0 PORT3	M1 Setting	M0 PORT2	M1 Setting	M0 PORT1	W/R
	1	0x7E1	Register Settings PORT 5-8	M1 Setting	M0 PORT8	M1 Setting	M0 PORT7	M1 Setting	M0 PORT6	M1 Setting	M0 PORT5	W/R
	2	0x7E2	Register of flags EN/CLR 1-interruption enable 0-interruption request reset	EN/CL IR8	EN/CL IR7	EN/CL IR6	EN/CL IR5	EN/CL IR4	EN/CL IR3	EN/CL IR2	EN/CL IR1	W/R
	3	0x7E3	Register (indicator) of requests for interruption from bits PORT	IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1	R

	4	0x7E4	Register (indicator) of input/output port bits state	HE PORT8	HE PORT7	HE PORT6	HE PORT5	HE PORT4	HE PORT3	HE PORT2	HE PORT1		R

Organisation of interruptions.

The interruptions may be initiated:

а) by external devices from bits PORT1-PORT8;

б) by internal devices (timers T1,T2,T3).

The initial addresses of subprograms of processing interruptions as their priority decrease are shown in the table.

Address	Source of interruption	Note
0x000	Supply switching on	
0x08F	Timers 1, 2 and 3 simultaneously	Simultaneously with timers there may be initiated interruption from input port which should be taken into consideration in interrupt service routine
0x09F	Timers 2 and 3 simultaneously	
0x0AF	Timers 1 and 3 simultaneously	
0x0CF	Timers 1 and 2 simultaneously	
0x0BF	Timer 3	
0x0DF	Timer 2	
0x0EF	Timer 1	
0x0FF	Input / output port	

Interruptions are executed after complete execution of the command of main program when there is a request. Interruptions are inhibited after the jump instructions: JMP, JMI and JC, JNC, JZ, JNZ when executing jump conditions, commands JSR of return from subprogram.

Interruptions from port bits may be initiated if the corresponding bit of interrupt enabling register in register RFC_2 is program-set into 1.

At the same time, reading the register RFC_3 (read-only) allows to display from which port bits interrupt requests are called. Interrupt request from any port bit can be reset after executing interrupt service routine by recording 0 into the corresponding bit in the register RFC_2 with the following setting of this bit into 1 for enabling thhe further inmterrupt request. Each port bit can be individually tuned by presetting bits M1, M0 in the registers RFC_3 and RFC_3 with the following possible options of internal states.

Bits		Internal port state	Interrupts	Notes
M1	M0			
0	0	OUT ZL (high-impedance 0)	Interrupts from external actions inhibited	By mask «programming» internal level ZL (high-impedance 0) can be disconnected
0	1	OUT L (“strong” zero)		
1	0	IN RL (resistive 0)	Interrupts from external actions enabled	Interrupts evocation under high level
1	1	IN RH (resistive 1)		Interrupts evocation under low level

Mask «programming» can disconnect internal level (ZL, RL,RH) with possible replacement of them by external resistors.

Reading of the register R FC_4 (read-only) allows to display state of all port bits given either, one or another external action.

External actions may be the following:

H – «strong» 1

HR – «weak» 1

L – «strong» 0

LR – «weak» 0

Z – high impedance state

State of port bits under all possible combinations of external actions and internal states are shown

in the table

Internal state	External action				
	H	HR	L	LR	Z
IN RH	1	1	0	0	1
IN RL	1	1	0	0	0
OUT L	1	0	0	0	0
OUT ZL	1	1	0	0	0

It's assumed that internal state and external actions are levelized stronger as for external actions.

MC includes three timers-counters T1, T2, T3. All the timers are binary octal counters with weight 128, 64, 32, 16, 8, 4, 2, 1.

Timer T1 (register RFB_1 with address 0x7D9)

Timer T1 is 8-bit counter with division factor 256 . The frequency of quartz oscillator 32768 Hz is applied on the counter input.
The counter is for reading only. Data read out on data bus is shown below.

D7	D6	D5	D4	D3	D2	D1	D0
T1_7	T1_6	T1_5	T1_4	T1_3	T1_2	T1_1	T1_0
128 Hz	256 Hz	512 Hz	1024 Hz	2048 Hz	4096 Hz	8192 Hz	16384 Hz

When reading the counter, the problems related to the possibility of reading changeable data, may occur. For the correct reading, if necessary, reading of data can be done several times in succession with the following comparison of the results. At the reset when switching on the supply, timer T1 is cleared (the counter is reset into zero state).
After execution of HLT command timer counter is reset and fixed in zero state (in zero state input OCSI is also fixed) until the next program starts (from external actions on IN_PORT).
At ripple-through carry of timer T1 which happens with period of 1/128 sec, FrT1 "short" pulse is formed, it sets interrupt request flag FR1 in the state register R7 into 1 (bit 4 of the state register R7), if masking bit of timer MFR1 (bit 7 of the state register R7) is reset into 0.
When setting masking bit of oftimer MFR1 into 1 state of flag FR1 doesn't change, but its setting during the next ripple-through carry on timer counter T1 is inhibited. There can be done reprogramming of T1 (by mask "programming") ensuring setting of FR1 flag with periods of 1/32 sec (at LCD multiplex 1/4) or 6/256 sec (at LCD multiplex 1/3). The data read-out on data bus can be the following:

D7	D6	D5	D4	D3	D2	D1	D0
T1_7	T1_6	T1_5	T1_4	T1_3	T1_2	T1_1	T1_0
32 Hz	256 Hz (64 Hz)	512 Hz	1024 Hz	2048 Hz	4096 Hz	8192 Hz	16384 Hz

or:

D7	D6	D5	D4	D3	D2	D1	D0
T1_7	T1_6	T1_5	T1_4	T1_3	T1_2	T1_1	T1_0
256/6 Hz	256 Hz	512 Hz	1024 Hz	2048 Hz	4096 Hz	8192 Hz	16384 Hz

Timers T2, T3 (registers RFB2, RFB3 with addresses 0x7DA and 0x7DB)

Timers T2, T3 are 8-bit counters with programmable division factor from setting registers KT2 (register RFB4 with address 0x7DC), KT3 (register RFB5 with address 0x7DE) . Division factors are programmed from maximum value 256 (when recording 0x00 into registers KT2, KT3) to the value equal to the contents of registers KT2, KT3 (from 0x01 to 0xFF except mode of notes

frequency forming in timer T2).
The counters are for reading only. When reading count register the problems related to the possibility of reading changeable data may occur. For the correct reading, if necessary, reading of the data can be done several times in succession with the following comparing of the results.

When the code equal to the contents of registers KT2, KT3 (or at ripple-through carry when recording 0x00 into registers KT2, KT3), timers T2, T3 are cleared (except mode of notes frequency forming in timer 2) and "short" pulses FrT2, FrT3 setting respectively interrupt request flag FR2 into 1 (bit 5 of the state register R7) and Interrupt request flag FR3 in the states register R7 (bit 6 of the state register R7) are formed.

Flag FR2 is not set into mode of notes frequency forming in timer T2 and in mode when "short" pulse FrT2 of timer T2 clearing is input signal of timer T3.

The timers are controlled by timers control register RFBO (address 0x7D8)

Description of RFBO control register bits:

Bit	Symbol	Description	After reset
RFBO_7	IN1-T3	7,6 bits choose source of timer T3 input signal 00 – signal of ripple-through carry of timer T1 («short» pulse FrT1) 01 – output T1_3 of timer T1 (2048Hz)	0
RFBO_6	IN0-T3	10 – signal of clearing timer T2 («short» pulse FrT2), in this mode setting of flag FR2 is inhibited 11 – external signal IN6 (output 06 when disconnecting SEG 01 by mask)	0
RFBO_5	IN1-T2	5,4 bits choose source of timer T2 input signal 00 – signal of ripple-through carry of timer T1 («short» pulse FrT1) 01 – output T1_3 of timer T1 (2048Hz)	0
RFBO_4	IN0-T2	10 – signal 65565 Hz (notes frequency forming mode), in this mode setting of FR2 flag is inhibited 11 –external signal IN6, IN7, IN8 (from outputs 06, 07 or 08 when disconnecting corresponding SEG 01, SEG 02, SEG 03 by mask)	0
RFBO_3	CLR-T3	1-clearing (reset and zero code fixation) of T3 timer counter, reset of FR3 flag (except mode, when T3 is clocked by FrT2 signal; in this mode RFBO_3 and RFBO_1 shoose source of input signal T2: 00-IN7, 01-IN6 ,1X –IN8)	0
RFBO_2	CLR-T2	1-clearing (reset and zero code fixation) of T2 timer counter, reset of FR2 flag and T3 timer with reset of FR3 flag (when T3 is clocked by FrT2 signal)	0
RFBO_1	EN-T3	1/0- (count enable) /(count inhibit) T3 (except mode when T3 is clocked by FrT2 signal; in this mode RFBO_3 and RFBO_1 shoose source of input signal T2: 00-IN7, 01-IN6 ,1X –IN8))	0
RFBO_0	EN-T2	1/0- (count enable) / (count inhibit) T2 (always) and (count enable) / (count inhibit) T3 (when T3 is clocked by FrT2 signal)	0

Timer T2 can be used in the mode of notes frequency forming for tunes synthesis. The mode is selected when recording code «10» into 5,4 bits of RFBO control register (IN1-T2=1, IN0-T2 = 0) and timer count enabling.

RFBO_7	RFBO_6	RFBO_5	RFBO_4	RFBO_3	RFBO_2	RFBO_1	RFBO_0
IN1-T3	IN0-T3	IN1-T2	IN0-T2	CLR-T3	CLR-T2	EN-T3	EN-T2
X	X	1	0	X	0	X	1

In this mode setting of interrupt request flag FR2 in the state register R7 is inhibited. Signal of 65565 Hz is applied on counter input.. Notes frequency is formed on counter output (output T2_7) and can be applied on external output "AL" at the set into 1 flag AL_EN in the state register R7.

Seven lower counter bits count in the beginning of zero semi-period of note. After reaching the code equal to the contents of 7 lower bits of KT2 register, 7 lower bits of the counter are cleared but the highest bit is switched into logic 1 and then the note second (unit) semi-period is counted in the same way.
As a result on output the frequency of 65565Hz/2N is formed, where N is number from 2 to 127, set in 7 lower bits of register KT2. To form notes period with accuracy to one period of input frequency 65565 Hz the following possibility is forseen. When setting in register KT2 the higher bit of KT register in logic 1 when counting the second (unit) semi-period at code reaching, equal to the contents of 7 lower bits of register KT2, 1-6 bits of timer are set into 0, but the lowest bit is set into 1 and, thus, the following zero semi-period of note is "cut" for one period of input signal. In this case the frequency equal to 65565 Hz / (2N-1) can be formed.
Formed notes frequency (output T2_7) can be supplied on external output "AL" at set into 1 flag AL_EN in the state register R7.
On output "AL" output T2_7 is also applied (at set into 1 flag AL_EN) at the following state of timers control register RFBO:

RFBO_7	RFBO_6	RFBO_5	RFBO_4	RFBO_3	RFBO_2	RFBO_1	RFBO_0
IN1-T3	IN0-T3	IN1-T2	IN0-T2	CLR-T3	CLR-T2	EN-T3	EN-T2
1	0	1	1	X	0	X	1

In this mode T2 is clocked by external signal (RC-oscillator), T3 by clearing signal T2 («short» pulse FrT2) , injection of the signal from output T2_7 on output «AL» is used for testing (measurement of RC-oscillator frequency).
Configuration of timers may by the following

Contents of register RFB0	Input T2	Interrupt request flag FR2	Input T3	Interrupt request flag FR3	Note
00000000	0(no count)	0	0(no count)	0	State after system reset
0000C3C2E3E2	FrT1	+	FrT1	+	
0001C3C2E3E2	2048 Hz	+	FrT1	+	
0100C3C2E3E2	FrT1	+	2048 Hz	+	
0101C3C2E3E2	2048 Hz	+	2048 Hz	+	
0010C3C2E3E2	65536 Hz	Set. inhibited	FrT1	+	Tune mode
0110C3C2E3E2	65536 Hz	Set. inhibited	2048 Hz	+	
1110C3C2E3E2	65536 Hz	Set. inhibited	IN6	+	
1010C3C2E3E2					Inhibited combination
1000XC32XE32	FrT1	Set. inhibited	FrT2	+	
1001XC32XE32	2048 Hz	Set. inhibited	FrT2	+	
0011C3C2E3E2	0(no count)	-	FrT1	+	
0111C3C2E3E2	0(no count)	-	2048 Hz	+	
1111C3C2E3E2	0(no count)	-	IN6	+	
10110C320 E32	IN7	Set. inhibited	FrT2	+	
10110C321 E32	IN6	Set. inhibited	FrT2	+	
10111C32X E32	IN8	Set. inhibited	FrT2	+	

E2 , E3 - bits (count enable) /(count inhibit) of timer 2 or 3
E32 bit (count enable) /(count inhibit) of timers 2 and 3 simultaneously
C2 , C3 - bits of clearing timer 2 or 3
C32 bit of clearing timers 2 and 3 simultaneously

Table of commands

N	Mnemonic	Instruction Code																Functions	Flag Change	
1	MV	1	0	1	1	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	(Rd) <= (Rs)		Z
2	MVI	1	0	0	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0	(Rd) <= C7-0		Z
3	ORI	1	0	1	0	0	1	0 1	C3	C2	C1	C0	D4	D3	D2	D1	D0	(Rd) <= (Rd) OR C3C2C1C0 0000 (record 1) (Rd) <= (Rd) OR 0000 C3C2C1C0		Z
4	AN	1	0	1	1	0	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	(Rd) <= (Rd) AND (Rs)		Z
5	ANI	1	0	1	1	1	1	0 1	C3	C2	C1	C0	D4	D3	D2	D1	D0	(Rd) <= (Rd) AND C3C2C1C0 1111 (record 0) (Rd) <= (Rd) AND 1111 C3C2C1C0		Z
6	ANI/	1	0	1	1	1	0	1 0	C3	C2	C1	C0	D4	D3	D2	D1	D0	<= (Rd) AND C3C2C1C0 0000 (bit analy- <= sis) (Rd) AND 0000 C3C2C1C0)		Z
7	XR	1	0	1	0	0	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	(Rd) <= (Rd) XR (Rs)		Z
8	XR/	1	0	1	0	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	<= (Rd) XR (Rs) (registers comparison)		Z
9	XRI	1	0	1	0	1	1	0 1	C3	C2	C1	C0	D4	D3	D2	D1	D0	(Rd) <= (Rd) XR C3C2C1C0 0000 (bit inver- (Rd) <= sion) (Rd) XR 0000 C3C2C1C0		Z
10	A	1	1	1	0	0	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	(Rd) <= (Rd) + (Rs)	C F	Z
11	S/	1	1	1	0	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	<= (Rd) + N(Rs) + 1	C F	Z
12	AC	1	1	1	0	0	1	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	(Rd) <= (Rd) + (Rs) + CF	C F	RZ
13	SC/	1	1	1	0	1	1	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	<= (Rd) + N(Rs) + CF	C F	RZ
14	S	1	1	1	1	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0	(Rd) <= (Rd) + N(Rs) + 1	C F	Z
15	AI	0	0	1	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0	(Rd) <= (Rd) + C7-0	C F	Z
16	SI/	1	1	0	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0	<= (Rd) + NC7-0 + 1	C F	Z
17	AIC	0	1	1	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0	(Rd) <= (Rd) + C7-0 +CF	C F	RZ
18	MVB	0	0	0	1	R3/ R2	SB 2	SB 1	SB 0	DB 2	DB 1	DB 0	D4	D3	D2	D1	D0	(Rd) <= MV bit from (R3 or R2)		

N	Mnemonic	Instruction Code																Functions	Flag Change	
19	TBL	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	(Addr. ROM) <= (R1, R0) (R2) <= ROM 7 -0 (R3) <= ROM 15 -8 (PC) <= (PC)+1		
20	JMI	1	1	1	1	0	1	0	0	X7	X6	X5	X4	X3	X2	X1	X0	(PC7-0) <= (R0) (PC15-8) <= X 7-0		
21	JMP	0	0	0	0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	(PC11-0) <= X 11-0 (PC15-12) SAVED		
22	JZ	0	1	0	0	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	(PC10-0) <= X 10-0 if Z=0 (PC15-11) SAVED if Z=0 (PC) <= (PC)+1 if Z=1		
23	JNZ	0	1	0	0	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	(PC10-0) <= X 10-0 if Z=1 (PC15-11) SAVED Z=1 (PC) <= (PC)+1 if Z=0		
24	JC	0	1	0	1	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	(PC10-0) <= X 10-0 if CF=0 (PC15-11) SAVED if CF=0 (PC) <= (PC)+1 if CF=1		
25	JNC	0	1	0	1	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	(PC10-0) <= X 10-0 if CF=1 (PC15-11) SAVED if CF=1 (PC) <= (PC)+1 if CF=0		
26	JSR	1	1	1	1	1	1	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	(STACK) <= (PC)+1 SP=SP+1 (PC1-0) <= OO (PC11-2) <= X 9-0 (PC15-12) SAVED		
27	RTI	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	(PC) <= (STACK) SP=SP-1		
28	RTN	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	(PC) <= (STACK) SP=SP-1		
29	WT	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	Program halt, (waiting)		
30	HLT	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Program halt, timer 1 reset and oscillator stop		

Notes:
PC – program counter
STACK - 7 level stack
SP-stack indicator
CF-carry flag
Z- zero result flag

RZ means that in these commands flag Z can be reset at nonzero result (if in the previous commands was set into 1)

IZ7008 pins description

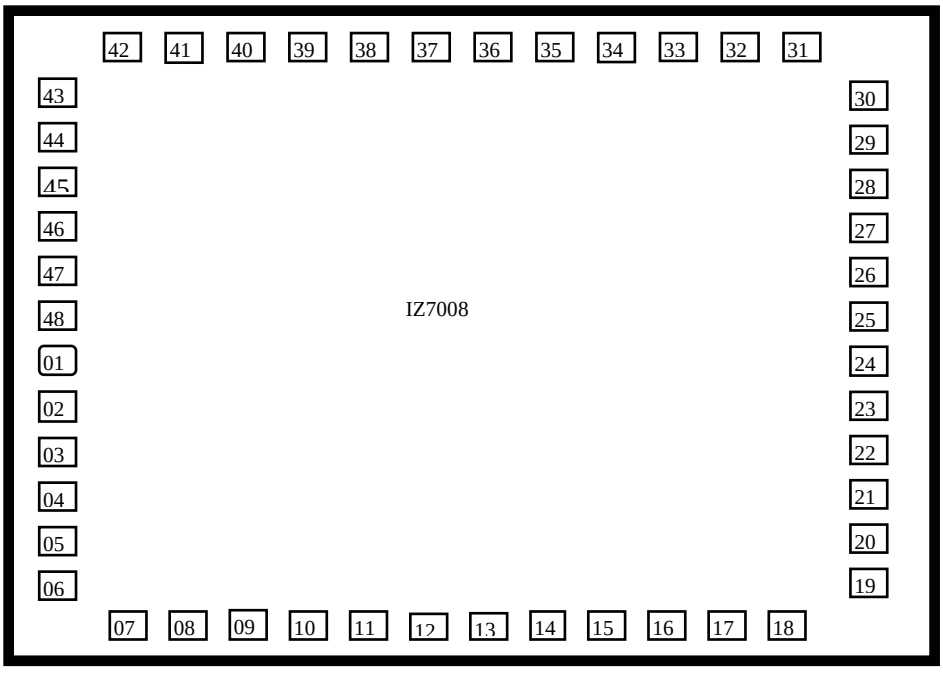
Contact pad No.	Symbol	Description
01	GND	Common output
02	IN3	Control input
03	OSCO	Output for connecting oscillator crystal
04	OSCI	Input for connecting oscillator crystal
05	COM1	Output of LCD common electrode control
06	SEG1/ IN6	Output of LCD segment electrode control / Control input*
07	SEG2/ IN7	Output of LCD segment electrode control / Control input*
08	SEG3/ IN8	Output of LCD segment electrode control / Control input*
09	SEG4	Output of LCD segment electrode control
10	SEG5	Output of LCD segment electrode control
11	SEG6	Output of LCD segment electrode control
12	SEG7	Output of LCD segment electrode control
13	SEG8	Output of LCD segment electrode control
14	SEG9	Output of LCD segment electrode control
15	SEG10	Output of LCD segment electrode control
16	SEG11	Output of LCD segment electrode control
17	SEG12	Output of LCD segment electrode control
18	SEG13	Output of LCD segment electrode control
19	SEG14	Output of LCD segment electrode control
20	SEG15	Output of LCD segment electrode control
21	COM3/ SEG16	Output of LCD common electrode control / Output of LCD segment electrode control
22	P2/ EL/ SEG02/ COM3	Voltage transducer output/ Electroluminiscent backlighting control output/ LCD segment electrode ocntrol output/ Output of LCD common electrode control *
23	P1/ IND/ COM3/ SEG16/ SEG01	Voltage transducer output/ Electroluminiscent backlighting control output/ LCD segment electrode ocntrol output/ Output of LCD common electrode control * LCD segment electrode ocntrol output// LCD segment electrode ocntrol output/*
24	IN2	Control input
25	IN1	Control input
26	UCC1	Supply voltage output from voltage source
27	AL	Alarm clock control output
28	COM2/ NAL	LCD common electrode control output/ Alarm clock control Inverse output*
29	SEG16/ COM2	LCD segment electrode control output/ LCD common electrode control output*
30	SEG17	LCD segment electrode control output
31	SEG18	LCD segment electrode control output

Table continued

Contact pad No.	Symbol	Description
32	SEG19	LCD segment electrode control output
33	SEG20	LCD segment electrode control output
34	SEG21	LCD segment electrode control output
35	SEG22	LCD segment electrode control output
36	SEG23	LCD segment electrode control output
37	SEG24	LCD segment electrode control output
38	SEG25	LCD segment electrode control output
39	SEG26	LCD segment electrode control output
40	SEG27	LCD segment electrode control output
41	SEG28	LCD segment electrode control output
42	SEG29	LCD segment electrode control output
43	SEG30	LCD segment electrode control output
44	SEG31	LCD segment electrode control output
45	SEG32	LCD segment electrode control output
46	U_{CC2}/ COM4/ SEG32	Supply voltage output from secondary voltage source LCD common electrode control output / LCD segment electrode control output *
47	IN5	Control input
48	IN4	Control input

LCD - liquid crystal display

* - function to be chosen by coding



INTEGRAL

Chip size: 3420±30 x 2430±30 mkm.
Chip width: 460±20 mkm.

Contact pad size 100x100 mkm in «Metallization layer»

Contact pad No.	Co-ordinates (mkm)		Contact pad No.	Co-ordinates (mkm)	
	X	Y		X	Y
01	106	1068	25	3216	1292
02	106	891	26	3216	1462
03	106	721	27	3216	1632
04	106	552	28	3216	1801
05	106	382	29	3216	1971
06	106	212	30	3216	2140
07	419	105	31	2902	2224
08	643	105	32	2678	2224
09	867	105	33	2454	2224
10	1091	105	34	2230	2224
11	1315	105	35	2006	2224
12	1539	105	36	1782	2224
13	1763	105	37	1558	2224
14	1987	105	38	1334	2224
15	2211	105	39	1110	2224
16	2435	105	40	886	2224
17	2659	105	41	662	2224
18	2883	105	42	438	2224
19	3216	275	43	106	2078
20	3216	444	44	106	1908
21	3216	614	45	106	1739
22	3216	784	46	106	1569
23	3216	953	47	106	1400
24	3216	1123	48	106	1230