# 8-BIT CONTROLLER WITH FLASH MEMORY OF PROGRAMS

The microcircuit IZ7012 – 8-bit controller with the FLASH – memory of programs (ROM testing coding with the watch functions, stopwatch with the possibility of the intermediate values fixation and writing of thirty results into memory).

The microcircuit is intended for receipt, processing and indication of data on the liquid crystal indicator The microcircuit is applicable in the electronic household appliance devices (counters, electronic watches, electronic thermometers, pedometers).

**Main characteristics:**

- ROM capacity, $Q_{ROM}$, bit……3072x16;
- PROM capacity, $Q_{ROM1}$, bit……1024x16;
- RAM capacity, $Q_{RAM}$, byte……..……....128;
- Number of bits of ALU, bits……8;
- Sources of interruptions…….….from 8 inputs,
  From event counter at input IN8,
  from three timers;
- Maximum number of controlled……..…….136 (34 LCD control drivers
  LCD segments…….....at multiplex levels 1/2,1/3,1/4);
- RISC-system of commands……30 types of commands;
- Stack……7 levels;
- Permissible value of potential
  of static electricity, V……..……..…....1500
  (for pins IN1-IN8, OSCI, OSCO)……..…..….(1000)

- Operating temperature range ……..….- 40 … +85 °C.

**Software of programs design for microcircuit**

Microcircuit IZ7012 contains in its composition EEPROM and mask ROM. ROM coding contains the control program, supporting programming the microcircuit EEPROM with application of software on the platform WINDOWS.

The integrated programming environment for the controller IZ70XX permit to write and debug the applications for development and fabrication of the company devices. The software of IZ70XX includes the text editor, emulator, compilator, debugger. Software of IZ70XX supports also operation with LCD editor, utility of ROM "encoding", utility of the EEPROM programming.

LCD editor – editor for creation of files, containing description of LCD segments. These files are required for visualization of information, applied to LCD in process of debugging, and are used by the controller operation emulator.

The program LCDDoc is intended for formation of the images, showing the controller operation modes, and their indication on LCD. The input information for the utility is the LCD description file, created by the LCD editor.

The utility LCDset is intended for the LCD automatic routing and creation of the files, containing the compliance description between the LCD segments and the microcontroller pins.

The ROM "encoding" utility RomTop is intended for formation of the layout layer from the executed program file.

For EEPROM programming it is required to connect the computer parallel port with the installed software of IZ70XX by means of the four wire bunch to the microcircuit IZ7012 on the device PCB.

**Table 1 – Connection of microcircuit IZ7012 to the parallel port of the computer.**

| Parallel Computer Port | | Microcircuit | | |
|---|---|---|---|---|
| Pin Number | Port Signal | Contact Pad Number | Identification | Purpose |
| 18, 19 | Ground | 06 | GND | Common pin (negative supply terminal) |
| 02-07 | Data0-Data5 | 21 | $U_{CC}$ | Power supply terminal (positive supply terminal) |
| 08, 15 | Data6, nError/nFault | 11 | IN1 | Control input / output |
| 09, 10 | Data7, nAck | 12 | IN2 | Control input / output |

Integrated environment of the programs design for the microcontroller IZ70XX is oriented for operation within the framework of the standard set of the technical and software means of the operating system WINDOWS on the personal computer. The minimum requirements to the technical means are determined by the installation requirements of the system WINDOWS 9X, WINDOWS 2000/XP. The graphics application within the framework of the given software requires the minimum display resolution of 640 × 480 dots and the color palette of not less than 256 colors.

Software of IZ70XX can be submitted to the interested consumers.

**Table 2 – Contact pads description**

| Contact Pad Number | Symbol | Description |
|---|---|---|
| 01 | COM1 | Control output of LCD common |
| 02 | COM2 | Control output of LCD common |
| 03 | COM3 | Control output of LCD common |
| 04 | COM4 | Control output of LCD common |
| 05 | $U_{TEST}$ | Supply voltage test pin / LCD supply voltage pin |
| 06 | GND | Common pin |
| 07 | OSCI | Input for connection of the quartz resonator |
| 08 | OSCO | Output for connection of the quartz resonator |
| 09 | OUT1 | Control output |
| 10 | OUT2 | Control output |
| 11 | IN1 | Temperature sensor input, comparator input, control input / output |
| 12 | IN2 | Temperature sensor input, comparator input, control input / output |
| 13 | IN3 | Temperature sensor input, comparator input, control input / output |
| 14 | IN4 | Temperature sensor input, comparator input, control input / output |
| 15 | OUT3 | Control output |
| 16 | OUT4 | Control output |
| 17 | IN5 | Temperature sensor input, comparator input, control input / output |
| 18 | IN6 | Temperature sensor input, comparator input, control input / output |
| 19 | IN7 | Temperature sensor input, comparator input, control input / output |
| 20 | IN8 | Temperature sensor input, comparator input, control input / output, event counter input |
| 21 | $U_{CC}$ | Supply voltage pin |
| 22 | IND | Control output of electroluminescent backlight |
| 23 | EL | Control output of electroluminescent backlight |
| 24 | NAL | Alarm inverse control output |
| 25 | AL | Alarm control output |
| 26 | SEG01 | Output of LCD symbol (segment) control |
| 27 | SEG02 | Output of LCD symbol (segment) control |
| 28 | SEG03 | Output of LCD symbol (segment) control |
| 29 | SEG04 | Output of LCD symbol (segment) control |
| 30 | SEG05 | Output of LCD symbol (segment) control |
| 31 | SEG06 | Output of LCD symbol (segment) control |
| 32 | SEG07 | Output of LCD symbol (segment) control |

**Table 2 Continued**

| Contact Pad Number | Symbol | Description |
|---|---|---|
| 33 | SEG08 | Output of LCD symbol (segment) control |
| 34 | SEG09 | Output of LCD symbol (segment) control |
| 35 | SEG10 | Output of LCD symbol (segment) control |
| 36 | SEG11 | Output of LCD symbol (segment) control |
| 37 | SEG12 | Output of LCD symbol (segment) control |
| 38 | SEG13 | Output of LCD symbol (segment) control |
| 39 | SEG14 | Output of LCD symbol (segment) control |
| 40 | SEG15 | Output of LCD symbol (segment) control |
| 41 | SEG16 | Output of LCD symbol (segment) control |
| 42 | SEG17 | Output of LCD symbol (segment) control |
| 43 | SEG18 | Output of LCD symbol (segment) control |
| 44 | SEG19 | Output of LCD symbol (segment) control |
| 45 | SEG20 | Output of LCD symbol (segment) control |
| 46 | SEG21 | Output of LCD symbol (segment) control |
| 47 | SEG22 | Output of LCD symbol (segment) control |
| 48 | SEG23 | Output of LCD symbol (segment) control |
| 49 | SEG24 | Output of LCD symbol (segment) control |
| 50 | SEG25 | Output of LCD symbol (segment) control |
| 51 | SEG26 | Output of LCD symbol (segment) control |
| 52 | SEG27 | Output of LCD symbol (segment) control |
| 53 | SEG28 | Output of LCD symbol (segment) control |
| 54 | SEG29 | Output of LCD symbol (segment) control |
| 55 | SEG30 | Output of LCD symbol (segment) control |
| 56 | SEG31 | Output of LCD symbol (segment) control |
| 57 | SEG32 | Output of LCD symbol (segment) control |
| 58 | SEG33 | Output of LCD symbol (segment) control |
| 59 | SEG34 | Output of LCD symbol (segment) control |

Notes
1 LCD – liquid crystal display.
2 Purpose of contact pads 11-14, 17-20 is determined by coding

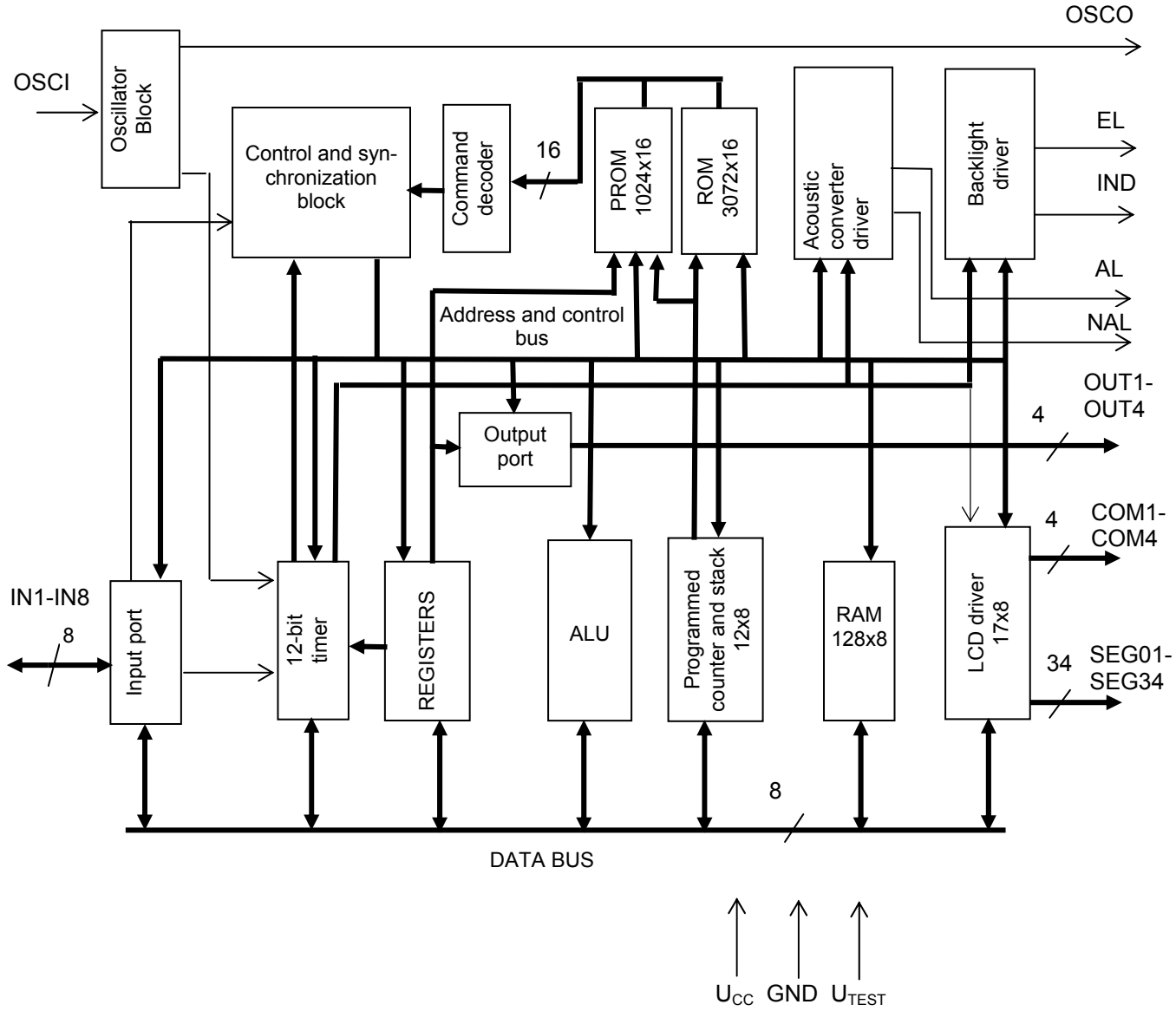



**Figure 1 – Layout Diagram**

**Table 3 – Recommended operation modes**

| Symbol | Parameter description | Norm | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $U_{CC}$ | Supply voltage | 2,4 | 5,5 | V |
| $U_{IL}$ | Low level input voltage | 0 | 0,3 | V |
| $U_{IH}$ | High level input voltage | $U_{CC}$-0,3 | $U_{CC}$ | V |
| $C_{OSCI}$ | Oscillator input stray capacitance | - | 8 | pF |
| $C_{OSCO}$ | Oscillator output stray capacitance | - | 5 | pF |

**Table 4 – Absolute maximum rarings**

| Symbol | Parameter Description | Norm | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $U_{CC}$ | Supply voltage | -0,3 | 6,0 | V |
| $U_{IL}$ | Low level input voltage | -0,3 | - | V |
| $U_{IH}$ | High level input voltage | - | $U_{CC}$+0,3 | V |

**Table 5 – Electric Parameters of Microcircuits (Testing Coding)**

| Symbol | Parameter | Measurement Mode | Norm | | Ambient temperature, °C | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $I_{OCC}$ | Dynamic consumption current in the stand-by mode | $U_{CC}$=5,5 V (without load) | - | 2,0<br>3,0 | 25±10<br>85<br>-40 | μA |
| $I_{CC}$ | Consumption current | $U_{CC}$=5,5 V | - | 1,5<br>2,0 | | μA |
| $I_{IL}$ | Low level input current, μA<br>- at inputs / outputs IN1-IN8 | $U_{CC}$=5,5 V<br>$U_{IL}$= 0,3 V | 1,1<br>1,0 | 20<br>28 | | μA |
| $I_{OZL}$ | Low level output current in the status «Off»<br>- at inputs / outputs IN1-IN8, outputs OUT1-OUT4 | $U_{CC}$=5,5 V<br>$U_O$= 0,3 V | - | \|±1,2\|<br>\|±1,4\| | | μA |
| | High level output current | | | | | |
| $I_{OH1}$ | - at outputs AL, NAL | $U_{CC}$=2,4 V<br>$U_{OH}$ = $U_{CC}$-0,2 V | \|-0,2\|<br>\|-0,14\| | - | | mA |
| $I_{OH2}$ | - at output IND | $U_{CC}$=2,4 V<br>$U_{OH}$ = $U_{CC}$-0,8 V | \|-0,15\|<br>\|-0,1\| | \|-1,2\|<br>\|-1,56\| | | mA |
| $I_{OH3}$ | - at output EL | $U_{CC}$=2,4 V<br>$U_{OH}$ = $U_{CC}$-0,8 V | \|-0,1 \|<br>\|-0,07 \| | \|-0,9\|<br>\|-1,17\| | | mA |
| $I_{OH4}$ | - at outputs OUT1-OUT4 | $U_{CC}$=2,4 V<br>$U_O$ = $U_{CC}$-0,8 V | \|-0,2\|<br>\|-0,14\| | - | | mA |
| | Low level output current | | | | | |
| $I_{OL1}$ | - at outputs AL, NAL | $U_{CC}$=2,4 V<br>$U_{OL}$ = 0,2 V | 0,2<br>0,14 | - | | mA |
| $I_{OL2}$ | - at outputs OUT1-OUT4, IND, at inputs / outputs IN1-IN8 | $U_{CC}$=2,4 V<br>$U_{OL}$ = 0,8 V | 3,0<br>2,1 | - | | mA |
| $I_{OL3}$ | - at output EL | $U_{CC}$=2,4 V<br>$U_{OL}$ = 0,8 V | 1,0<br>0,7 | - | | mA |
| $U_{OSC}$ | Start voltage of quartz oscillator | t≤3 s<br>41 Hz ≤$f_C$≤ 44 Hz<br>$C_{OSCI}$ ≤ 8 pF<br>$C_{OSCO}$ ≤ 5 pF | - | 2,4<br>2,5 | | V |

**Operation description**
**Reprogrammed ROM**

Reprogrammed ROM is used for storage of commands or data and contains 1024 commands (16-bit instructions) at addresses from 0xC00 to 0xFFF. Area of the reprogrammed ROM within the address range from 0xC00 to 0xC01 (2 commands) is reserved for the 26-bit control total of the reprogrammed ROM codes and the six bit sign of the reprogrammed ROM initial testing and granting permission for writing. The reprogrammed ROM area within the address range from 0xC02 to 0xC0A (9 commands) is reserved for the transfer commands for the initial subprogram addresses of the interruptions processing, located in the reprogrammed ROM area. Transfer to these addresses is performed after execution of the interruption processing programs, located in ROM, transfer to which is executed by the hardware means.

**Table 6 – Initial addresses of interruption processing subprograms**

| Address | Interruption Source | Remarks |
|---|---|---|
| 0xC02 | Power supply switch | - |
| 0xC03 | Timers 1, 2 and 3 simultaneously | Simultaneously with the timers it is possible to initiate interruption from the input port, which is required to take into consideration in the interruption servicing programs |
| 0xC04 | Timers 2 and 3 simultaneously | |
| 0xC05 | Timers 1 and 3 simultaneously | |
| 0xC06 | Timers 1 and 2 simuiltaneously | |
| 0xC07 | Timer 3 | |
| 0xC08 | Timer 2 | |
| 0xC09 | Timer 1 | |
| 0xC0A | Input port | - |

Programming of the reprogrammed ROM is performed under control of the program from ROM.

**ROM**

ROM contains 3072 commands (16-bit instructions) at the addresses from 0x000 to 0xBFF. The ROM area within the range from 0x000 to 0x0FF (256 commands) is reserved for the interruption servicing and controller testing programs. The ROM areas with the addresses 0x7e, 0x7f and the addresses from 0x7FE to 0x801 (4 commands) are reserved for the control ROM total and the stack registers test, checked during the controller testing.

**Table 7 – Initial addresses of interruption processing subprograms (in the order of the priority diminishing)**

| Address | Interruption Source | Remarks |
|---|---|---|
| 0x000 | Power supply switch on | - |
| 0x08F | Timers 1, 2 and 3 simultaneously | Simultaneously with the timers it is possible to initiate interruption from the input port, which is required to be taken into consideration in the interruption servicing programs |
| 0x09F | Timers 2 and 3 simultaneously | |
| 0x0AF | Timers 1 and 3 simultaneously | |
| 0x0CF | Timers 1 and 2 simultaneously | |
| 0x0BF | Timer 3 | |
| 0x0DF | Timer 2 | |
| 0x0EF | Timer 1 | |
| 0x0FF | Input port | - |

ROM is for location of the interruption processing and controller testing programs, including the reprogrammed ROM block testing, the reprogrammed ROM erasure and writing control programs, library of the applied subprograms.

**Random Access Memory (RAM)**

RAM is arranged as banks of 8 registers each and contains the internal function registers with the direct addressing, the general purpose registers with the direct or index addressing R8, R9, RA, RB, RC, RD, RE, RF, othe RAM data area with the index addressing, the special registers and the data memory, directly indicated on LCD, with the index addressing.

The controller service registers are located in the address space from 0x000 to 0x007 (bank 00) and have the following purpose:

- R0, R1, R2, R3 - accumulator registers;
- R5, R6 - base index registers BM, BH of storing the addressed bank number;
- R4, R7- controller status registers.

RAM data area of the volume 128 bytes is located in the address space from 0x008 to 0x07F (banks 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10).

**Table 8 – RAM Data Area**

| Bank | Register Number in Bank | Address | Name in Direct Addressing | Name in Index Addressing | Purpose |
|---|---|---|---|---|---|
| 00 | 0 | 0x000 | R0 | - | Accumulator |
| | 1 | 0x001 | R1 | - | Accumulator |
| | 2 | 0x002 | R2 | - | Accumulator |
| | 3 | 0x003 | R3 | - | Accumulator |
| | 4 | 0x004 | R4 | - | Status register |
| | 5 | 0x005 | R5 or BM | - | BM base register |
| | 6 | 0x006 | R6 or BH | - | BH base register |
| | 7 | 0x007 | R7 | - | Status register |
| 01 | 0 | 0x008 | R8 | M0,H0 | General purpose registers |
| | 1 | 0x009 | R9 | M1,H1 | |
| | 2 | 0x00A | RA | M2,H2 | |
| | 3 | 0x00B | RB | M3,H3 | |
| | 4 | 0x00C | RC | M4,H4 | |
| | 5 | 0x00D | RD | M5,H5 | |
| | 6 | 0x00E | RE | M6,H6 | |
| | 7 | 0x00F | RF | M7,H7 | |
| 02 | 0 | 0x010 | - | M0,H0 | Register RAM |
| | 1 | 0x011 | - | M1,H1 | |
| | 2 | 0x012 | - | M2,H2 | |
| | 3 | 0x013 | - | M3,H3 | |
| | 4 | 0x014 | - | M4,H4 | |
| | 5 | 0x015 | - | M5,H5 | |
| | 6 | 0x016 | - | M6,H6 | |
| | 7 | 0x017 | - | M7,H7 | |
| 03 | 0 | 0x018 | - | M0,H0 | Register RAM |
| | 1 | 0x019 | - | M1,H1 | |
| | 2 | 0x01A | - | M2,H2 | |
| | 3 | 0x01B | - | M3,H3 | |
| | 4 | 0x01C | - | M4,H4 | |
| | 5 | 0x01D | - | M5,H5 | |
| | 6 | 0x01E | - | M6,H6 | |
| | 7 | 0x01F | - | M7,H7 | |
| 04 | 0 | 0x020 | - | M0,H0 | Register RAM |
| | 1 | 0x021 | - | M1,H1 | |
| | 2 | 0x022 | - | M2,H2 | |
| | 3 | 0x023 | - | M3,H3 | |
| | 4 | 0x024 | - | M4,H4 | |
| | 5 | 0x025 | - | M5,H5 | |
| | 6 | 0x026 | - | M6,H6 | |
| | 7 | 0x027 | - | M7,H7 | |
| 05 | 0 | 0x028 | - | M0,H0 | Register RAM |
| | 1 | 0x029 | - | M1,H1 | |
| | 2 | 0x02A | - | M2,H2 | |
| | 3 | 0x02B | - | M3,H3 | |
| | 4 | 0x02C | - | M4,H4 | |
| | 5 | 0x02D | - | M5,H5 | |
| | 6 | 0x02E | - | M6,H6 | |
| | 7 | 0x02F | - | M7,H7 | |

Table 8 Continued

| Bank | Register Number in Bank | Address | Name in Direct Addressing | Name in Index Addressing | Purpose |
|---|---|---|---|---|---|
| 06 | 0 | 0x030 | - | M0,H0 | Register RAM |
| | 1 | 0x031 | - | M1,H1 | |
| | 2 | 0x032 | - | M2,H2 | |
| | 3 | 0x033 | - | M3,H3 | |
| | 4 | 0x034 | - | M4,H4 | |
| | 5 | 0x035 | - | M5,H5 | |
| | 6 | 0x036 | - | M6,H6 | |
| | 7 | 0x037 | - | M7,H7 | |
| 07 | 0 | 0x038 | - | M0,H0 | Register RAM |
| | 1 | 0x039 | - | M1,H1 | |
| | 2 | 0x03A | - | M2,H2 | |
| | 3 | 0x03B | - | M3,H3 | |
| | 4 | 0x03C | - | M4,H4 | |
| | 5 | 0x03D | - | M5,H5 | |
| | 6 | 0x03E | - | M6,H6 | |
| | 7 | 0x03F | - | M7,H7 | |
| 08 | 0 | 0x040 | - | M0,H0 | Register RAM |
| | 1 | 0x041 | - | M1,H1 | |
| | 2 | 0x042 | - | M2,H2 | |
| | 3 | 0x043 | - | M3,H3 | |
| | 4 | 0x044 | - | M4,H4 | |
| | 5 | 0x045 | - | M5,H5 | |
| | 6 | 0x046 | - | M6,H6 | |
| | 7 | 0x047 | - | M7,H7 | |
| 09 | 0 | 0x048 | - | M0,H0 | Register RAM |
| | 1 | 0x049 | - | M1,H1 | |
| | 2 | 0x04A | - | M2,H2 | |
| | 3 | 0x04B | - | M3,H3 | |
| | 4 | 0x04C | - | M4,H4 | |
| | 5 | 0x04D | - | M5,H5 | |
| | 6 | 0x04E | - | M6,H6 | |
| | 7 | 0x04F | - | M7,H7 | |
| 0A | 0 | 0x050 | - | M0,H0 | Register RAM |
| | 1 | 0x051 | - | M1,H1 | |
| | 2 | 0x052 | - | M2,H2 | |
| | 3 | 0x053 | - | M3,H3 | |
| | 4 | 0x054 | - | M4,H4 | |
| | 5 | 0x055 | - | M5,H5 | |
| | 6 | 0x056 | - | M6,H6 | |
| | 7 | 0x057 | - | M7,H7 | |
| 0B | 0 | 0x058 | - | M0,H0 | Register RAM |
| | 1 | 0x059 | - | M1,H1 | |
| | 2 | 0x05A | - | M2,H2 | |
| | 3 | 0x05B | - | M3,H3 | |
| | 4 | 0x05C | - | M4,H4 | |
| | 5 | 0x05D | - | M5,H5 | |
| | 6 | 0x05E | - | M6,H6 | |
| | 7 | 0x05F | - | M7,H7 | |

**Table 8 Continued**

| Bank | Register Number in Bank | Address | Name in Direct Addressing | Name in Index Addressing | Purpose |
|---|---|---|---|---|---|
| 0C | 0 | 0x060 | - | M0,H0 | Register RAM |
| | 1 | 0x061 | - | M1,H1 | |
| | 2 | 0x062 | - | M2,H2 | |
| | 3 | 0x063 | - | M3,H3 | |
| | 4 | 0x064 | - | M4,H4 | |
| | 5 | 0x065 | - | M5,H5 | |
| | 6 | 0x066 | - | M6,H6 | |
| | 7 | 0x067 | - | M7,H7 | |
| 0D | 0 | 0x068 | - | M0,H0 | Register RAM |
| | 1 | 0x069 | - | M1,H1 | |
| | 2 | 0x06A | - | M2,H2 | |
| | 3 | 0x06B | - | M3,H3 | |
| | 4 | 0x06C | - | M4,H4 | |
| | 5 | 0x06D | - | M5,H5 | |
| | 6 | 0x06E | - | M6,H6 | |
| | 7 | 0x06F | - | M7,H7 | |
| 0E | 0 | 0x070 | - | M0,H0 | Register RAM |
| | 1 | 0x071 | - | M1,H1 | |
| | 2 | 0x072 | - | M2,H2 | |
| | 3 | 0x073 | - | M3,H3 | |
| | 4 | 0x074 | - | M4,H4 | |
| | 5 | 0x075 | - | M5,H5 | |
| | 6 | 0x076 | - | M6,H6 | |
| | 7 | 0x077 | - | M7,H7 | |
| 0F | 0 | 0x078 | - | M0,H0 | Register RAM |
| | 1 | 0x079 | - | M1,H1 | |
| | 2 | 0x07A | - | M2,H2 | |
| | 3 | 0x07B | - | M3,H3 | |
| | 4 | 0x07C | - | M4,H4 | |
| | 5 | 0x07D | - | M5,H5 | |
| | 6 | 0x07E | - | M6,H6 | |
| | 7 | 0x07F | - | M7,H7 | |
| 10 | 0 | 0x078 | - | M0,H0 | Register RAM |
| | 1 | 0x079 | - | M1,H1 | |
| | 2 | 0x07A | - | M2,H2 | |
| | 3 | 0x07B | - | M3,H3 | |
| | 4 | 0x07C | - | M4,H4 | |
| | 5 | 0x07D | - | M5,H5 | |
| | 6 | 0x07E | - | M6,H6 | |
| | 7 | 0x07F | - | M7,H7 | |

**RAM Registers Addressing**

R0 – R4, R5 (or BM), R6 (or BH), R8 – RF – names of RAM registers in commands during the direct addressing. For the registers R0 – R7 the direct addressing is possible only. For the registers
R8 – RF the direct or index addressing is possible, for the remaining registers – the index addressing only.

BM, BH – base index registers (R5, R6 appropriately). During the index addressing the RAM registers the contents of the base register determines the data bank number.

M0-M7, H0-H7 – names of the RAM registers in the commands during the index addressing. For the names of the registers M0-M7 the data bank number is determined by the contents of the base register R5 (BM), for the names of the registers H0-H7 the data bank number is determined by the contents of the base register R6 (BH). For computation of the physical address the contents of the indicated in the command of the base register should be multiplied by 8 with addition of the number from 0 to 7 appropriately. For instance: during writing in the command «M5» the physical address is equal to ((BM)∗8+5). When turning on the power supply on the base index registers R5, R6 are set by the software means.

**Status Register R7**

**Table 9 –Status register R7 bits description**

| Bit | Symbol | Purpose and performed action | Status at power on switching |
|---|---|---|---|
| R7_7 | MFR1 | 1 – Masking (denial) of setting to 1 of the request flag for interruption of FR1 from the timer | 1 |
| R7_6 | FR3 | Interruption request flag from the timer (set to 1 by «overfilling» of bits CNT[7:0] of the event counter at the control input IN8 at RFC0_3=1 or (at RFC0_3=0) by «overfilling» of bits T[9:0] after each 1024 periods of the timer input signal at R7_1=0, or by «overfilling» of bits T[11:0] after each 4096 periods of the timer input signal at R7_1=1) | 0 |
| R7_5 | FR2 | Interruption request flag from the timer (set to 1 after one period of the timer input signal after achieving the expected status of the timer bits T[11:4], concuriding with the code in the register RFB3) | 0 |
| R7_4 | FR1 | Interruption request flag from the timer (set to 1 after one period of the timer input signal after achieving the expected status of the timer bits T[7:0], concuring with the code in the register RFB0) | 0 |
| R7_3 | MFR3 | 1 – masking (denial) of setting to 1 of the interruption request flag from the timer or from the event counter at the control input IN8 | 1 |
| R7_2 | MFR2 | 1 – masking (denial) of setting to 1 of the FR2 interruption request flag from the timer | 1 |
| R7_1 | 8HZFR3 | 1–interruption request from the timer by «overfilling» of bits T[11:0] of the timer.<br>0– interruption request from the timer by «overfilling» of the T[9:0] timer bits or the interruption request from the eight bit counter by the control input IN8 by «overfilling» of bits CNT[7:0] of the counter | 0 |
| R7_0 | SVD_ON | 0 – turn-off of the supply voltage sensor and connection to the comparators at the inputs IN1- IN4 as the reference level of the divider output of supply voltage by two.<br>1 – turn-on of the supply voltage sensor and connection tothe comparators at the inputs IN1- IN4 as the reference level of the reference voltage source output (1,25 ± 0,15) V.<br>Time of setting the reference level of not over 1 ms | 0 |

**Status Register R4**

At the status «0» in the bits RFC0_7, RFC0_6, RFC0_5 RFC0_4 of the special register RFC0 are switched appropriately the microcircuit outputs OUT4, OUT3, OUT2, OUT1 (status Z instead of L and the status Z instead of H). When turning on the power supply, the register RFC0 is cleared (status «0x00»).

H – high level status ( 1 ).
L – low level status ( 0 ).
Z – high impedance status.

**Table 10 –Status register R4 bits description**

| Bit | Symbol | Purpose and performed action | Status at power on switching |
|---|---|---|---|
| R4_7 | DOUT4 | Status of the microcircuit pin OUT4 at RFC0_7=1 | 1 |
| R4_6 | DOUT3 | Status of the microcircuit pin OUT3 at RFC0_6=1 | 1 |
| R4_5 | DOUT2 | Status of the microcircuit pin OUT2 at RFC0_5=1 | 1 |
| R4_4 | DOUT1 | Status of the microcircuit pin OUT1 at RFC0_4=1 | 1 |
| R4_3 | SVD | 1 – at the supply voltage of less than 2,5 V | 0 |
| R4_2 | ELEN | 1 – turn-on of the electroluminescent backlight driver (outputs IND, EL).<br>0 – turn-off of the electroluminescent backlight driver (outputs IND, EL) | 0 |
| R4_1 | ALEN | 0 – sound denial (microcircuit pins AL=0, NAL=1).<br>1 – sound permission (microcircuit pins AL=1, NAL=0), if R4_0=0 or the timer bit T_2=0 | 0 |
| R4_0 | EN4096 | 1 – with sound permission, i. e. at R4_1=1, pins AL=1, NAL=0, if the timer bit T_2=0, otherwise the microcircuit pins AL=0, NAL=1, if the timer bit T_2=1.<br>0 – with sound permission, i. e. at R4_1=1, pins AL=1, NAL=0 irrespective of the timer bit T_2 | 1 |

**LCD Driver Memory**

At RFC0_1=0 and RFC0_0=0 the multiplex level is selected to be 1/4.
At RFC0_1=0 and RFC0_0=1 the multiplex level is selected to be 1/3.
At RFC0_1=1 the multiplex level is selected to be 1/2.

**Table 11 – Purpose of LCD Driver Memory Bits**

| Configuration of LCD Driver Memory at Multiplex Level 1/4 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank | Register Number in Bank | Address | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | COM |
| FD | 0 | 0x7E8 | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM1 |
| | 1 | 0x7E9 | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM2 |
| | 2 | 0x7EA | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM3 |
| | 3 | 0x7EB | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM4 |
| | 4 | 0x7EC | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM1 |
| | 5 | 0x7ED | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM2 |
| | 6 | 0x7EE | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM3 |
| | 7 | 0x7EF | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM4 |
| FE | 0 | 0x7E0 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM1 |
| | 1 | 0x7E1 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM2 |
| | 2 | 0x7E2 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM3 |
| | 3 | 0x7E3 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM4 |
| | 4 | 0x7E4 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM1 |
| | 5 | 0x7E5 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM2 |
| | 6 | 0x7E6 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM3 |
| | 7 | 0x7E7 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM4 |
| FB | 4 | 0x7DC | SEG02 COM1 | SEG02 COM2 | SEG02 COM3 | SEG02 COM4 | SEG01 COM1 | SEG01 COM2 | SEG01 COM3 | SEG01 COM4 | – |

**Table 11 Continued**

| Configuration of LCD Driver Memory at Multiplex Level 1/3 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank | Register Number in Bank | Address | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | COM |
| FD | 0 | 0x7E8 | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM1 |
| | 1 | 0x7E9 | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM2 |
| | 2 | 0x7EA | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM |
| | 3 | 0x7EB | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 4 | 0x7EC | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM1 |
| | 5 | 0x7ED | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM2 |
| | 6 | 0x7EE | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM3 |
| | 7 | 0x7EF | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| FE | 0 | 0x7E0 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM1 |
| | 1 | 0x7E1 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM2 |
| | 2 | 0x7E2 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM3 |
| | 3 | 0x7E3 | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 4 | 0x7E4 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM1 |
| | 5 | 0x7E5 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM2 |
| | 6 | 0x7E6 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM3 |
| | 7 | 0x7E7 | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| FB | 4 | 0x7DC | SEG02 COM1 | SEG02 COM2 | SEG02 COM3 | SEG02 RAM | SEG01 COM1 | SEG01 COM2 | SEG01 COM3 | SEG01 RAM | – |

**Table 11 Continued**

| Configuration of LCD Driver Memory at Multiplex level 1/2 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank | Register Number in Bank | Address | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | COM |
| FD | 0 | 0x7E8 | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM1 |
| | 1 | 0x7E9 | SEG04 | SEG06 | SEG08 | SEG10 | SEG12 | SEG14 | SEG16 | SEG18 | COM2 |
| | 2 | 0x7EA | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 3 | 0x7EB | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 4 | 0x7EC | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM1 |
| | 5 | 0x7ED | SEG03 | SEG05 | SEG07 | SEG09 | SEG11 | SEG13 | SEG15 | SEG17 | COM2 |
| | 6 | 0x7EE | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 7 | 0x7EF | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| FE | 0 | 0x7E0 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM1 |
| | 1 | 0x7E1 | SEG33 | SEG31 | SEG29 | SEG27 | SEG25 | SEG23 | SEG21 | SEG19 | COM2 |
| | 2 | 0x7E2 | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 3 | 0x7E3 | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 4 | 0x7E4 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM1 |
| | 5 | 0x7E5 | SEG34 | SEG32 | SEG30 | SEG28 | SEG26 | SEG24 | SEG22 | SEG20 | COM2 |
| | 6 | 0x7E6 | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| | 7 | 0x7E7 | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | RAM |
| FB | 4 | 0x7DC | SEG02 COM1 | SEG02 COM2 | SEG02 RAM | SEG02 RAM | SEG01 COM1 | SEG01 COM2 | SEG01 RAM | SEG01 RAM | – |

Data memory, directly indicated on the LCD segments, whose maximum volume is used for LCD control at multiplex 1/4, constitutes 17 bytes or 136 bits and is located at the addresses from 0x7E8 to 0x7F7 (banks FD, FE) and at the address 0x7DC (register RFB4 in bank FB). For the LCD memory the index addressing is possible only.

When switching on the power supply the multiplex level is 1/4, the LCD memory is set by the software means.

**Table 12 – Sequence of signals alteration at pins COM1, COM2, COM3, COM4 at the multiplex level 1/4**

| T_7 | COM1 | COM2 | COM4 | COM3 |
|---|---|---|---|---|
| 0 | 1 | M | M | M |
| 1 | M | 1 | M | M |
| 0 | M | M | 1 | M |
| 1 | M | M | M | 1 |
| 0 | 0 | M | M | M |
| 1 | M | 0 | M | M |
| 0 | M | M | 0 | M |
| 1 | M | M | M | 0 |

Notes

1 «1» - output level complies with $U_{CC}$;

2 «0» - output level complies with GND;

3 «M» - output level complies with $U_{CC}/2$

Signals at pins COM1, COM2, COM3, COM4 at the multiplex level 1/4 alter with the period 8/256 s each 1/256 s (with the period of the output signal of the T_6 timer bit).

**Table 13 – Sequence of signals alteration at pins COM1, COM2, COM3, COM4 at the multiplex level 1/3**

| T_7 | COM1 | COM2 | COM4 | COM3 |
|---|---|---|---|---|
| 0 | 1 | M | M | M |
| 1 | M | 1 | M | M |
| 0 | M | M | M | 1 |
| 1 | 0 | M | M | M |
| 0 | M | 0 | M | M |
| 1 | M | M | M | 0 |

Signals at pins COM1, COM2, COM3, COM4 at the multiplex level 1/3 alter with the period of 6/256 s with each 1/256 s (with the period of the output signal of the T_6 timer bit).

**Table 14 – Sequence of the signals alteration at the pins COM1, COM2, COM3, COM4 with the multiplex level 1/2**

| T_7 | COM1 | COM2 | COM4 | COM3 |
|---|---|---|---|---|
| 0 | 1 | M | M | M |
| 1 | 1 | M | M | M |
| 0 | M | 1 | M | M |
| 1 | M | 1 | M | M |
| 0 | 0 | M | M | M |
| 1 | 0 | M | M | M |
| 0 | M | 0 | M | M |
| 1 | M | 0 | M | M |

Signals at the pins COM1, COM2, COM3, COM4 at the multiplex level 1/2 alter with the period 8/256 s.

During execution of the command HLT for the time prior to stop by interruption from the input port and for the time of the initial set-up when switching on power supply the signals at the pins COM1, COM2, COM3, COM4 are set to be equal to $U_{CC}$, and after this they are transferred to the initial status.

**Table 15 – Initial status of the signals at the pins COM1, COM2, COM3, COM4 during switching on power supply**

| T_7 | COM1 | COM2 | COM4 | COM3 |
|---|---|---|---|---|
| 0 | 1 | M | M | M |

**Special Registers and Interruptions**

Controller's special registers have the addresses from 0x7D0 to 0x7E4 (banks FA, FB, FC). Bank FC contains six registers only from RFC_0 to RFC_5.

Special registers of the bank FB (except the register RFB_4, in which the data are located, directly indicated on LCD) are intended for the interruptions control from the timer, eight bit event counter at the control input IN8 by «overfilling» of the CNT[7:0] counter bits and from the input port.

Special registers of the 12-bit timer T[11:0] block have the addresses 0x7D8 – 0x7DB (bank FB), of the input port block have the addresses 0x7DE and 0x7DF (bank FB).

For the special registers, the index addressing is possible only.

**Table 16 – Special registers of Bank FB**

| Bank | Register Number in Bank | Address | Purpose | Bit_7 | Bit_6 | Bit_5 | Bit_4 | Bit_3 | Bit_2 | Bit_1 | Bit_0 | Address |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FB | 0 | 0x7D8 | Comparison code register with the timer junior byte T[7:0] | KT_7 | KT_6 | KT_5 | KT_4 | KT_3 | KT_2 | KT_1 | KT_0 | Writing/ read-out |
| | 1 | 0x7D9 | Timer junior byte read-out address T[7:0] | T_7 | T_6 | T_5 | T_4 | T_3 | T_2 | T_1 | T_0 | Read-out |
| | 2 | 0x7DA | Timer senior byte read-out address T[11:4] | T_11 | T_10 | T_9 | T_8 | T_7 | T_6 | T_5 | T_4 | Read-out |
| | 3 | 0x7DB | Comparison code register with the timer senior byte T[11:4] | KT_11 | KT_10 | KT_9 | KT_8 | KT_7 | KT_6 | KT_5 | KT_4 | Writing/ read-out |
| | 5 | 0x7DD | Eight bit event counter read-out address at the control input IN8 of bits CNT[7:0] | CNT_7 | CNT_6 | CNT_5 | CNT_4 | CNT_3 | CNT_2 | CNT_1 | CNT_0 | Read-out |
| | 6 | 0x7DE | Register EN_IR for interruptions permission from the control inputs IN8, IN7, IN6, IN5, IN4, IN3, IN2, IN1.<br>1-interruption permission from control input.<br>0-interruption request reset from control input | EN_8 | EN_7 | EN_6 | EN_5 | EN_4 | EN_3 | EN_2 | EN_1 | Writing/ read-out |
| | 7 | 0x7DF | Register read-out address of IR requests for interruption from the control inputs IN8, IN7, IN6, IN5, IN4, IN3, IN2, IN1 | IR_8 | IR_7 | IR_6 | IR_5 | IR_4 | IR_3 | IR_2 | IR_1 | Read-out |

When turning on power supply the registers RFB1, RFB2, RFB6, RFB7 and the counter CNT[7:0] are reset to 0x00, and the registers RFB0, RFB3 are set by the software means.

Interruptions may be initiated:

- by the interruption requests from the control inputs IN8, IN7, IN6, IN5, IN4, IN3, IN2, IN1;
- by the interruption requests from the timer FR1, FR2, FR3, by the interruption request FR3 from the eight bit event counter at the control input IN8 by «overfilling» of bits CNT[7:0]of the counter.

Interruptions are performed after completion of the main program command execution at arrival of the request. Interruptions are denied after the transfer commands: JMP, JMI and JC, JNC, JZ, JNZ during execution of the transfer conditions, command JSR of return from the subprogram.

Interruptions from the port bits can be initiated, if by the software means the appropriate bit of the interruption permission fags register is set to 1 in the register RFB6.

Meanwhile, read-out of the register RFB7 (access for read-out only) makes it possible to indicate, from which bits of the input port the requests were called for interruption. Request for interruption from any port bit can be reset after completion of the interruption service program by means of writing 0 into the appropriate bit in the register RFB6 with the subsequent setting of the given bit to 1 for permission of the subsequent interruption request.

Each port bit may be individually set by means of setting the similar named bits RFC2_i, RFC1_i in the registers RFC2 и RFC1.

**Table 17** – **Possible options of internal statuses adjustment**

| Bit | | Internal Status of IN_i Port i-st Bit | Remark |
|---|---|---|---|
| RFC2_i | RFC1_i | | |
| 1 | 0 | IN_OUT Z at RFB6_i=0 (high impedance).<br>This status is set when turning on power supply.<br><br>IN_OUT ZL at RFB6_i=1 (high impedance 0).<br>At RFB6_i=1 the internal current source is connected of 110 nA , supporting the level ZL | Interruption from internal influences are possible |
| 0 | 0 | IN_OUT L ( «strong» 0 ).<br>Output resistance of less than 200 Ohm | |
| 0 | 1 | IN RL (resistive 0).<br>Input resistance of over 100 kOhm | |
| 1 | 1 | IN_OUT RH (resistive 1).<br>Input resistance of over 50 kOhm | |

External influences can be as follows:

- H -«strong» 1;
-HR -«weak» 1;
- L -«strong» 0;
- LR -«weak» 0;
- Z -high impedance status.

**Table 18 – Status of the port bits at all possible combinations of the external influences and the internal statuses**

| Internal status | External Influence | | | | |
|---|---|---|---|---|---|
| | H | HR | L | LR | Z |
| IN RH | 1 | 1 | 0 | 0 | 1 |
| IN RL | 1 | 1 | 0 | 0 | 0 |
| OUT L | 1 | 0 | 0 | 0 | 0 |
| OUT ZL | 1 | 1 | 0 | 0 | 0 |

Irrespective of alignment of the input port the requests for interruption from the i-st port bit can be initiated at the input influence above the internal reference level when setting in the register RFC3 of the similar named bits RFC3_i=1 (the same status is set also when turning on power supply) or during the input influence below the reference level at RFC3_i=0. The reference level is determined by the bit R7_0 (SVD_ON) of the status register.

**Mode registers and Addresses of Programmed ROM RFC4 and RFC5, Bank Registers FA**

Special registers of the bank FA are used as the buffer data memory during programming of the programmed ROM. Register RFC4 is used as the mode control of the programmed ROM operation, and the register RFC5 is used as the address one when programming the programmed ROM. Contents of the register RFC5 sets the number from 0 to 255 of the programmable bank of the programmed ROM with the volume of 4 commands (64 bits), which corresponds to the volume of the bank FA of the buffer data memory. Registers of the bank FA and the registers RFC4, RFC5 are cleared when turning on power supply (status «0»).

Programming of the programmed ROM is allowed only by banks of 64 bits.

**Table 19 – Bits description or Mode Register RFC4 of programmed ROM**

| Bit | Identification | Purpose and Performed Action | Status when Turning on Power Supply |
|---|---|---|---|
| RFC4_7 | Uref_add1 | 1 – increase of the output level of the reference voltage source (1,25 ± 0,15) V by 0,33 V.<br>Time of setting the output level is not over 1 ms | 0 |
| RFC4_6 | Uref_add0 | 1 – rise of output level of the reference voltage source (1,25 ± 0,15) V by 0,17 V.<br>Time of setting the output level is not over 1 ms | 0 |
| RFC4_5 | PUMP_Uhigh | 1 – turning on the RC-oscillator and the supply voltage multiplier.<br>Rise time of the output level Uhigh of the supply voltage multiplier to the voltage of programming the programmed ROM not over 1 ms.<br>Discharge time of voltage Uhigh to supply voltage at RFC4_5=0 is not over 15 μs | 0 |
| RFC4_4 | FLAG | Program flag | 0 |
| RFC4_3 | PROGR | 1 – turn-on of the data writing mode from the bank FA to the addressed bank of the programmed ROM.<br>Write time is not over 10 ms | 0 |
| RFC4_2 | ERASE | 1 – turn-on of the data erasure mode in the addressed bank of the programmed ROM.<br>Erasure time is not over 10 ms | 0 |
| RFC4_1 | READ | 0 – read-out mode of the programmed ROM at the address from the program counter.<br>1– read-out mode denial of the programmed ROM, programming mode of the programmed ROM at the address from the register RFC5 | 0 |
| RFC4_0 | FLAG | Program flag | 0 |

**Table 20 – Compliance of the Address Register Bits of the Programmed ROM with the Command Address Bits**

| Bit | Command Address Bit | Status during Turn-on of Power Supply |
|---|---|---|
| RFC5_7 | A9 | 0 |
| RFC5_6 | A8 | 0 |
| RFC5_5 | A7 | 0 |
| RFC5_4 | A6 | 0 |
| RFC5_3 | A5 | 0 |
| RFC5_2 | A4 | 0 |
| RFC5_1 | A3 | 0 |
| RFC5_0 | A2 | 0 |

**Table 21 – Compliance of the Command Address Codes and Register Contents of Bank FA**

| Bits Code of Command Address A1A0 | Command Code, Written from FA Bank Registers | Status FA Bank Registers Status during Turn-on of Power Supply |
|---|---|---|
| 00 | (RFA1.RFA0) | 0x0000 |
| 01 | (RFA3.RFA2) | 0x0000 |
| 10 | (RFA5.RFA4) | 0x0000 |
| 11 | (RFA7.RFA6) | 0x0000 |

**Timer**

Controller has in its composition the block of 12-bit timer T[11:0]. The timer is essentially the binary twelve bit counter with the division ratio of 4096 with the weights of bits [2048, 1024, 512, 256, 128, 64, 32, 16, 8, 4, 2, 1].

The counter status alters during change of the status «0» at the counter input (the low level voltage at the pin of the microcircuit OSCI, i. e., the potential of the level GND) to the status «1» (the high level voltage at the pin of the microcircuit OSCI, i.e. the level potential $U_{CC}$). To the counter input the frequency is applied of the quartz oscillator of 32768 Hz.

The status of the T[7:0] timer junior byte is accessible at the read-out address 0x7D9 (RFB1).

**Table 22 - Information, read out to the data bus, of the T[7:0] Timer Junior Byte**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| T_7 | T_6 | T_5 | T_4 | T_3 | T_2 | T_1 | T_0 |
| 128 Hz | 256 Hz | 512 Hz | 1024 Hz | 2048 Hz | 4096 Hz | 8192 Hz | 16384 Hz |

Status of the T[11:4] timer senior byte is accessible at the read-out address 0x7DA (RFB2).

**Table 23 - Information, read-out to the data bus, of the T[11:4] Timer Senior Byte**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| T_11 | T_10 | T_9 | T_8 | T_7 | T_6 | T_5 | T_4 |
| 8 Hz | 16 Hz | 32 Hz | 64 Hz | 128 Hz | 256 Hz | 512 Hz | 1024 Hz |

When reading the timer there may arise the problems, pertaining to the possibility of reading out the variable data. For the correct reading it is possible, for instance, to perform the data read-out several times in succession with the subsequent comparison of the results. When turning on power supply the timer T[11:0] is reset to the status of 0x000.

After execution of the command HLT the timer T[11:0] is rest to the status of 0x000 and is fixed in this status (under the status «0» the microcircuit OSCI input is also fixed) prior to the program start-up from the external influences on the input port, by which interruption is permitted.

### Microcircuit Commands

**Table 24 – Microcircuit Commands**

| Mnemonics | Command Code | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | | | | | | | | | | | | | | | |
| 1 MV | 1 | 0 | 1 | 1 | 1 | 0 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 2 MVI | 1 | 0 | 0 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 3 ORI | 1 | 0 | 1 | 0 | 0 | 1 | 0<br>1 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 4 AN | 1 | 0 | 1 | 1 | 0 | 0 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 5 ANI | 1 | 0 | 1 | 1 | 1 | 1 | 0<br>1 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 6 ANI/ | 1 | 0 | 1 | 1 | 0 | 1 | 0<br>1 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 7 XR | 1 | 0 | 1 | 0 | 0 | 0 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 8 XR/ | 1 | 0 | 1 | 0 | 1 | 0 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 9 XRI | 1 | 0 | 1 | 0 | 1 | 1 | 0<br>1 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 10 A | 1 | 1 | 1 | 0 | 0 | 0 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 11 S/ | 1 | 1 | 1 | 0 | 1 | 0 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 12 AC | 1 | 1 | 1 | 0 | 0 | 1 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 13 SC/ | 1 | 1 | 1 | 0 | 1 | 1 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 14 S | 1 | 1 | 1 | 1 | 1 | 0 | S4 | S3 | S2 | S1 | S0 | D4 | D3 | D2 | D1 | D0 |
| 15 AI | 0 | 0 | 1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 16 SI/ | 1 | 1 | 0 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 17 AIC | 0 | 1 | 1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | D4 | D3 | D2 | D1 | D0 |
| 18 MVB | 0 | 0 | 0 | 1 | R3/R2 | SB2 | SB1 | SB0 | DB2 | DB1 | DB0 | D4 | D3 | D2 | D1 | D0 |
| 19 TBL | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20 JMI | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| 21 JMP | 0 | 0 | 0 | 0 | X11 | X10 | X9 | X8 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| 22 JZ | 0 | 1 | 0 | 0 | 1 | X10 | X9 | X8 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| 23 JNZ | 0 | 1 | 0 | 0 | 0 | X10 | X9 | X8 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| 24 JC | 0 | 1 | 0 | 1 | 1 | X10 | X9 | X8 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| 25 JNC | 0 | 1 | 0 | 1 | 0 | X10 | X9 | X8 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| 26 JSR | 1 | 1 | 1 | 1 | 1 | 1 | X9 | X8 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| 27 RTI | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28 RTN | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 29 WT | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 30 HLT | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 24 Continued**

| Mnemonics | Performed Operations | Operation Results Flags to be Set | |
|---|---|---|---|
| 1 | 3 | 4 | |
| 1 MV | (Rd) <= (Rs) | - | Z |
| 2 MVI | (Rd) <= C7-0 | - | Z |
| 3 ORI | (Rd) <= (Rd) OR C3C2C1C0 0000 ( writing 1 )<br>(Rd) <= (Rd) OR 0000 C3C2C1C0 | - | Z |
| 4 AN | (Rd) <= (Rd) AND (Rs) | - | Z |
| 5 ANI | (Rd) <= (Rd) AND C3C2C1C0 1111 (writing 0)<br>(Rd) <= (Rd) AND 1111 C3C2C1C0 | - | Z |
| 6 ANI/ | <= (Rd) AND C3C2C1C0 0000 ( analysis<br><= (Rd) AND 0000 C3C2C1C0 of bit ) | - | Z |
| 7 XR | (Rd) <= (Rd) XR (Rs) | - | Z |
| 8 XR/ | <= (Rd) XR (Rs) ( comparison of registers) | - | Z |
| 9 XRI | (Rd) <= (Rd) XR C3C2C1C0 0000 ( inversion<br>(Rd) <= (Rd) XR 0000 C3C2C1C0 of bit ) | - | Z |
| 10 A | (Rd) <= (Rd) + (Rs) | CF | Z |
| 11 S/ | <= (Rd) + N(Rs) + 1 | CF | Z |
| 12 AC | (Rd) <= (Rd) + (Rs) + CF | CF | RZ |
| 13 SC/ | <= (Rd) + N(Rs) + CF | CF | RZ |
| 14 S | (Rd) <= (Rd) + N(Rs) + 1 | CF | Z |
| 15 AI | (Rd) <= (Rd) + C7-0 | CF | Z |
| 16 SI/ | <= (Rd) + NC7-0 + 1 | CF | Z |
| 17 AIC | (Rd) <= (Rd) + C7-0 +CF | CF | RZ |
| 18 MVB | (Rd) <= MV bit from (R3) or ( R2) | - | - |
| 19 TBL | (Adr.ROM ) <= (R1, R0)<br>(R2) <= ROM 7 –0<br>(R3) <= ROM 15 –8<br>(PC) <= (PC)+1 | - | - |
| 20 JMI | (PC7-0) <= (R0)<br>(PC15-8) <= X 7-0 | - | - |
| 21 JMP | (PC11-0) <= X 11-0<br>(PC15-12) STORED | - | - |
| 22 JZ | (PC10-0) <= X 10-0 if Z=1<br>(PC15-11) STORED if Z=1 | - | - |
| | (PC) <= (PC)+1 if Z=0 | | |
| 23 JNZ | (PC10-0) X 10-0 if Z=0 | - | - |
| | (PC15-11) STORED if Z=0 | | |
| | (PC) (PC)+1 if Z=1 | | |
| 24 JC | (PC10-0) <= X 10-0 if CF=1 | - | - |
| | (PC15-11) STORED if CF=1 | | |
| | (PC) <= (PC)+1 if CF=0 | | |
| 25 JNC | (PC10-0) <= X 10-0 if CF=0 | - | - |
| | (PC15-11) STORED if CF=0 | | |
| | (PC) <= (PC)+1 if CF=1 | | |
| 26 JSR | (STACK) <= (PC)+1 SP=SP+1<br>(PC1-0) <= 00<br>(PC11-2) <= X 9-0 | - | - |
| | (PC15-12) STORED | - | - |
| 27 RTI | (PC) <= (STACK) SP=SP-1 | - | - |
| 28 RTN | (PC) <= (STACK) SP=SP-1 | - | - |
| 29 WT | Program stop, stand-by | - | - |
| 30 HLT | Program stop, reset of the timer and the oscillator stop | - | - |

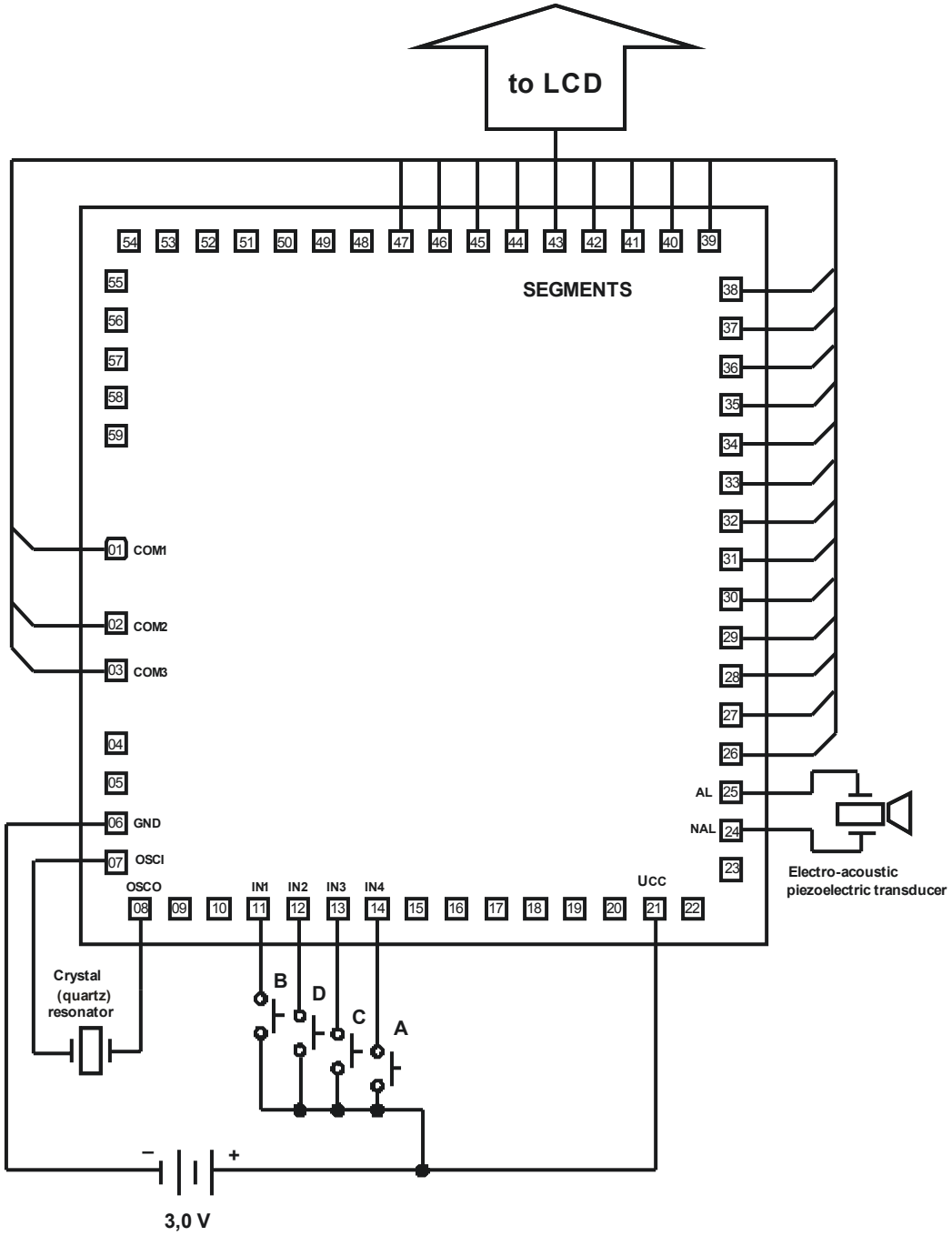
**Table 24 Continued**

Notes

1 PC – program counter.
2 STACK – seven level stack.
3 SP – stack indicator.
4 CF – transfer flag.
5 Z – zero result flag.
6 RZ – indicates, that in the given commands the flag Z can be reset only with the different from zero result (if it was set in the preceding commands to 1)

**Table 25 – Operands Address Field Codes D4D3/S4S3 and Types of Addressing**

| Address Field Code of Operands D4D3 / S4S3 | Type of Addressing |
|---|---|
| 00 | Direct addressing, bank 00 |
| 01 | Direct addressing, bank 01 |
| 10 | Index addressing, index from register R5 |
| 11 | Index addressing, index from register R6 |

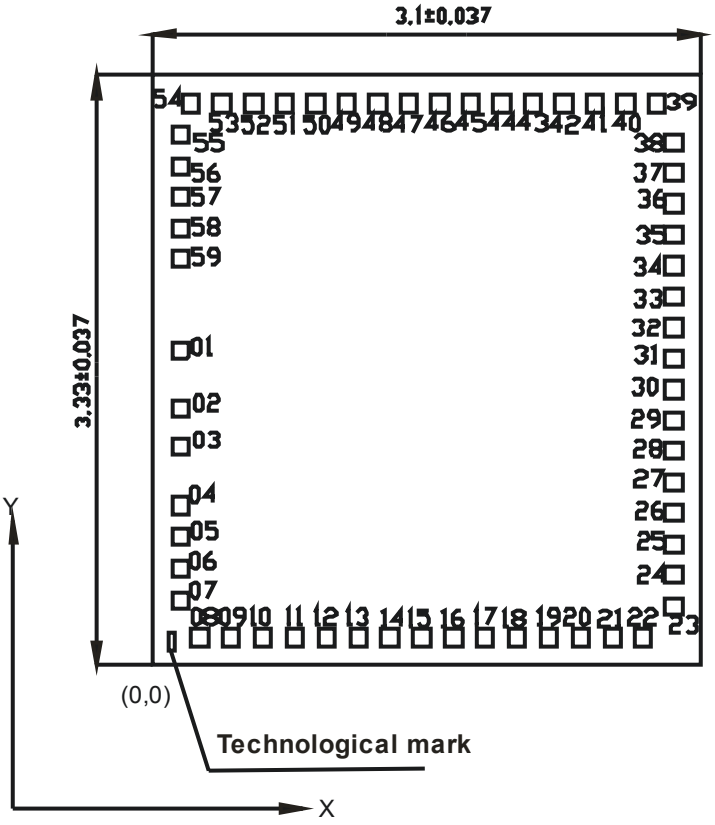



The crystal resonator applied with a microcircuit should have following characteristics:
- Frequency of a resonance $f_P$ = 32768 Hz at load capacity $C_L$ = 6 pF;
- Dynamic resistance $R_S$ ≤35 kOhm;
- Q-factor Q ≥35000;
- Static capacity $C_O$≤2,5 pF;
- Dynamic capacity $C_I$ 0,≤004 pF.

**Figure 2 – Application diagram**
**(ROM coding with the functions of the watch, stopwatch with the possibility of fixation of the intermediate values and writing of thirty results into the memory).**

**Contact pads layout diagram**

Microcircuits are delivered on the common wafer, undiced.
Mass of the microcircuits is not over 0,01 g.




Chip thickness (0,46 ± 0,02) mm.
Technological marking on the chip 7012-1 with the coordinates, mm: x=0,120, y=0,130.

**Figure 3 – Location diagram of the contact pads.**

**Table 26 – Coordinates and sizes of the contact pads**

| Number of contact pad | Coordinates (left bottom corner), μm | |
|---|---|---|
| | X | Y |
| 01 | 0,112 | 1,736 |
| 02 | 0,112 | 1,401 |
| 03 | 0,112 | 1,192 |
| 04 | 0,112 | 0,857 |
| 05 | 0,112 | 0,679 |
| 06 | 0,112 | 0,500 |
| 07 | 0,112 | 0,322 |
| 08 | 0,223 | 0,112 |
| 09 | 0,402 | 0,112 |
| 10 | 0,579 | 0,112 |
| 11 | 0,758 | 0,112 |
| 12 | 0,937 | 0,112 |
| 13 | 1,116 | 0,112 |
| 14 | 1,295 | 0,112 |
| 15 | 1,474 | 0,112 |
| 16 | 1,655 | 0,112 |
| 17 | 1,834 | 0,112 |
| 18 | 2,013 | 0,112 |
| 19 | 2,192 | 0,112 |
| 20 | 2,371 | 0,112 |
| 21 | 2,550 | 0,112 |
| 22 | 2,724 | 0,112 |
| 23 | 2,896 | 0,289 |
| 24 | 2,896 | 0,464 |
| 25 | 2,896 | 0,639 |
| 26 | 2,896 | 0,813 |
| 27 | 2,896 | 0,988 |
| 28 | 2,896 | 1,163 |
| 29 | 2,896 | 1,338 |
| 30 | 2,896 | 1,512 |
| 31 | 2,896 | 1,687 |
| 32 | 2,896 | 1,862 |
| 33 | 2,896 | 2,037 |
| 34 | 2,896 | 2,212 |
| 35 | 2,896 | 2,386 |
| 36 | 2,896 | 2,561 |

**Table 26 Continued**

| Number of contact pad | Coordinates (left bottom corner), μm | |
|---|---|---|
| | X | Y |
| 37 | 2,896 | 2,736 |
| 38 | 2,896 | 2,911 |
| 39 | 2,800 | 3,127 |
| 40 | 2,626 | 3,127 |
| 41 | 2,451 | 3,127 |
| 42 | 2,276 | 3,127 |
| 43 | 2,101 | 3,127 |
| 44 | 1,926 | 3,127 |
| 45 | 1,752 | 3,127 |
| 46 | 1,577 | 3,127 |
| 47 | 1,402 | 3,127 |
| 48 | 1,227 | 3,127 |
| 49 | 1,052 | 3,127 |
| 50 | 0,878 | 3,127 |
| 51 | 0,703 | 3,127 |
| 52 | 0,528 | 3,127 |
| 53 | 0,347 | 3,127 |
| 54 | 0,173 | 3,127 |
| 55 | 0,112 | 2,947 |
| 56 | 0,112 | 2,772 |
| 57 | 0,112 | 2,598 |
| 58 | 0,112 | 2,423 |
| 59 | 0,112 | 2,248 |
| Note – Coordinates and size of the contact pads 0,092 x 0,092 mm are given by the layer «Passivation» | | |