8-BIT CONTROLLER WITH MASK PROGRAMMING

Microcircuit IZ7013 – 8-bit controller with the mask programming (ROM test coding with the functions of the electronic wrist watch with the five program alarm, stopwatch and timer).
The microcircuit is intended for receipt, processing and indication of data on the liquid crystal indicator The microcircuit is applicable in the electronic household appliance devices (counters, electronic watches, electronic thermometers, pedometers).

Main Features:

- ROM capacity, Q_{ROM}, bits……2560x16;
- RAM capacity, Q_{RAM}, bits……..……..72x8;
- Number of bits of ALU, bits……..……8;
- Sources of interruptions…….……from 8 inputs,
  from event counter at input IN8,
  from three timers;
- Maximum number of controlled…….136 (34 LCD control drivers
  LCD segments…….....at multiplex levels 1/2,1/3,1/4);
- RISC-system of instructions……..…30 types of instructions;
- Stack……7 levels;
- Accepted value of potential
  of static electricity, V ……..…...1500
  (for pins IN1-IN4, OSCI, OSCO)……..…..(1000)
- Operating temperature range ……- 40 … +85 °C.

Table 1 –Contact pads description

Number of contact pad	Symbol	Purpose
01	COM1	Control output of LCD common electrode
02	COM2	Control output of LCD common electrode
03	COM3	Control output of LCD common electrode
04	COM4	Control output of LCD common electrode
05	U_{TEST}	Supply voltage test pin / LCD supply voltage pin
06	GND	Common pin
07	OSCI	Input for connection of quartz resonator
08	OSCO	Output for connection of quartz resonator
09	OUT1	Control output
10	OUT2	Control output
11	IN1	Temperature sensor input, comparator input or control input
12	IN2	Comparator input or control input
13	IN3	Comparator input or control input
14	IN4	Comparator input or control input
15	IN5 / OUT3	Control input / Control output
16	IN6 / OUT4	Control input / Control output
17	IN7	Control input
18	U_{CC}	Supply voltage pin from voltage source
19	IN8 / NAL	Control input or event counter input / Inverse alarm control output
20	AL	Alarm control output
21	SEG1 / IND	Output of LCD symbol (segment) control / Electro-luminescent backlight control output
22	SEG2 / EL	Output of LCD symbol (segment) control / Electro-luminescent backlight control output
23	SEG3	Output of LCD symbol (segment) control
24	SEG4	Output of LCD symbol (segment) control
25	SEG5	Output of LCD symbol (segment) control
26	SEG6	Output of LCD symbol (segment) control
27	SEG7	Output of LCD symbol (segment) control
28	SEG8	Output of LCD symbol (segment) control
29	SEG9	Output of LCD symbol (segment) control
30	SEG10	Output of LCD symbol (segment) control
31	SEG11	Output of LCD symbol (segment) control
32	SEG12	Output of LCD symbol (segment) control
33	SEG13	Output of LCD symbol (segment) control
34	SEG14	Output of LCD symbol (segment) control
35	SEG15	Output of LCD symbol (segment) control
36	SEG16	Output of LCD symbol (segment) control
37	SEG17	Output of LCD symbol (segment) control
38	SEG18	Output of LCD symbol (segment) control
39	SEG19	Output of LCD symbol (segment) control
40	SEG20	Output of LCD symbol (segment) control

Table 1 Continued

Number of contact pad	Symbol	Purpose
41	SEG21	Output of LCD symbol (segment) control
42	SEG22	Output of LCD symbol (segment) control
43	SEG23	Output of LCD symbol (segment) control
44	SEG24	Output of LCD symbol (segment) control
45	SEG25	Output of LCD symbol (segment) control
46	SEG26	Output of LCD symbol (segment) control
47	SEG27	Output of LCD symbol (segment) control
48	SEG28	Output of LCD symbol (segment) control
49	SEG29	Output of LCD symbol (segment) control
50	SEG30	Output of LCD symbol (segment) control
51	SEG31	Output of LCD symbol (segment) control
52	SEG32	Output of LCD symbol (segment) control
53	SEG33	Output of LCD symbol (segment) control
54	SEG34	Output of LCD symbol (segment) control

Notes:
1 LCD – liquid crystal display.
2 Purpose of contact pads 11-16, 19, 21, 22 is determined by coding

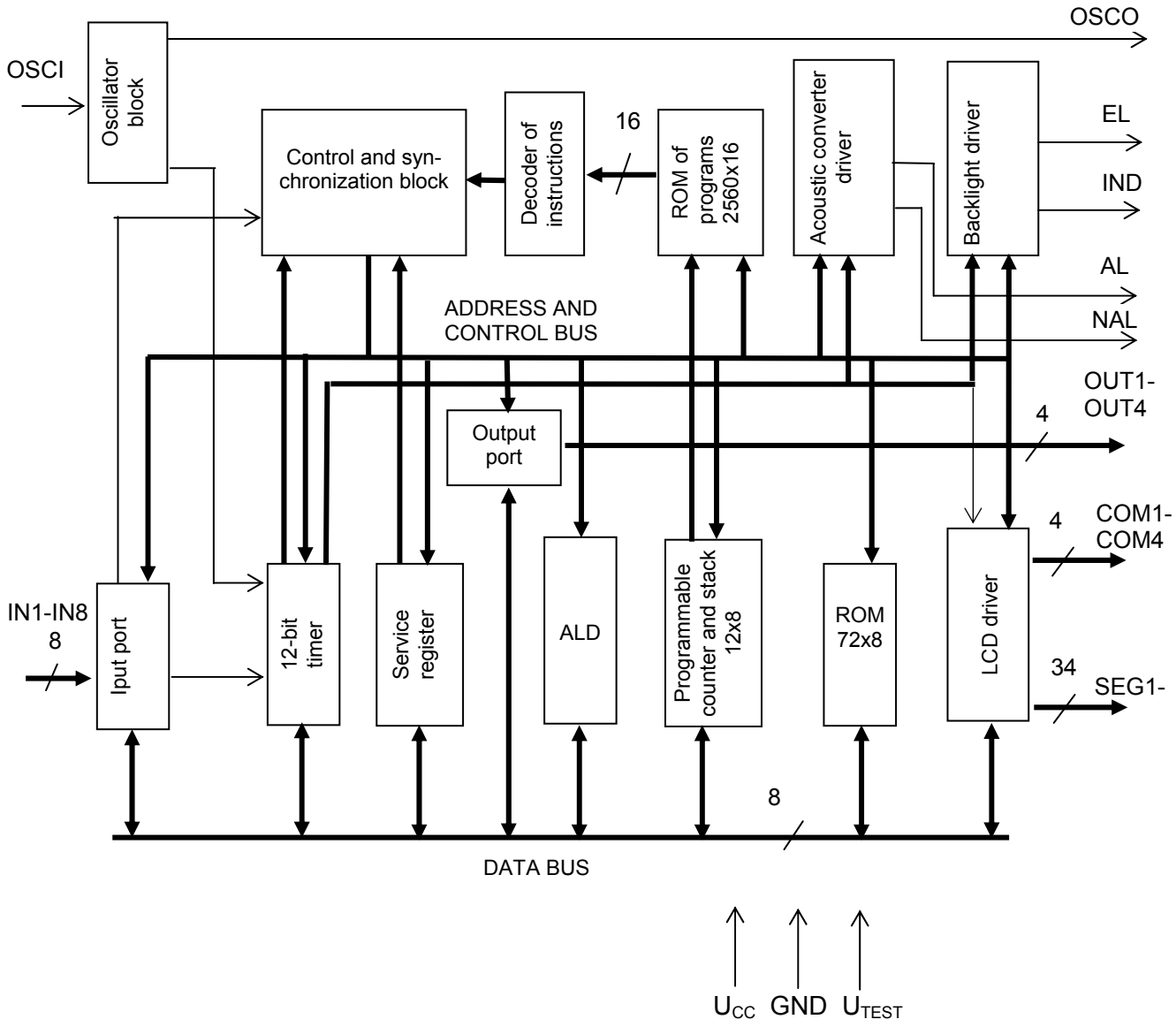


Figure 1 – Layout Diagram

Table 2 –Recommended Operation Electric Modes

Symbol	Parameter Description	Norm		Unit
		Min	Max	
U_{CC}	Supply voltage	2,4	5,5	V
U_{IL}	Low level input voltage	0	0,3	V
U_{IH}	High level input voltage	U_{CC}-0,3	U_{CC}	V
C_{OSCI}	Oscillator input stray capacitance	-	8	pF
C_{OSCO}	Oscillator output stray capacitance	-	5	pF

Table 3 – Maximum rating

Symbol	Parameter Description	Norm		Unit
		Min	Max	
U_{CC}	Supply voltage	-0,3	6,0	V
U_{IL}	Low level input voltage	-0,3	-	V
U_{IH}	High level input voltage	-	U_{CC}+0,3	V

Table 4 – Electric Parameters of Microcircuits (Test Coding)

Symbol	Parameter	Measurement Mode	Norm		Ambient Temperature, °C	Unit
			Min	Max		
I_{OCC}	Dynamic consumption current in the stand-by mode	U_{CC}=5,5 V (without load)	-	2,0 3,0	25±10 85 -40	μA
I_{CC}	Consumption current	U_{CC}=5,5 V	-	1,5 2,0		μA
I_{IL}	Low level input current - at inputs IN1-IN7	U_{CC}=5,5 V U_{IL}= 0,3 V	-	20 28		μA
I_{OH1}	High level output current - at outputs AL, NAL	U_{CC}=2,4 V U_{OH} = U_{CC}-0,2 V	|-0,2| |-0,14|	-		μA
I_{OH2}	- at output IND	U_{CC}=2,4 V U_{OH} = U_{CC}-0,8 V	|-0,15| |-0,1|	|-1,2| |-1,56|		mA
I_{OH3}	- at output EL	U_{CC}=2,4 V U_{OH} = U_{CC}-0,8 V	|-0,1 | |-0,07 |	|-0,9| |-1,17|		mA
I_{OL1}	Low level output current - at outputs AL, NAL	U_{CC}=2,4 V U_{OL} = 0,2 V	0,2 0,14	-		mA
I_{OL2}	- at output IND	U_{CC}=2,4 V U_{OL} = 0,8 V	3,0 2,1	-		mA
I_{OL3}	- at output EL	U_{CC}=2,4 V U_{OL} = 0,8 V	1,0 0,7	-		mA
U_{OSC}	Start-up voltage of the quartz oscillator	t≤3 s 31 Hz ≤ f_C ≤ 34 Hz C_{OSCI} ≤ 8 pF C_{OSCO} ≤ 5 pF	-	2,4 2,5		V

Operation Description

1.1.Read Only Memory (ROM)

ROM contains 2560 instructions (16 - bit instructions) at the addresses from 0x000 to 0x9FF. ROM area within the address range from 0x000 to 0x0FF (256 instructions) is reserved for processing interruptions and testing the controller. ROM areas with the addresses of 0x7e, 0x7f and addresses from 0x7FE to 0x801 (4 instructions) are reserved for the control ROM total and the stack registers test, to be checked while testing the controller.

Table 5 – Subprogram Initial Addresses for Processing Interruptions (In the Order of Priority Reduction)

Address	Interruption Source	Remark
0x000	Power switch on	-
0x08F	Timers 1, 2 and 3 simultaneously	Simultaneously with the timers it is possible to initiate interruption from the input port, which is required to be taken into consideration in the program of servicing interruptions
0x09F	Timers 2 and 3 simultaneously	
0x0AF	Timers 1 and 3 simultaneously	
0x0CF	Timers 1 and 2 simultaneously	
0x0BF	Timer 3	
0x0DF	Timer 2	
0x0EF	Timer 1	
0x0FF	Input port	-

1.2.Random Access Memory (RAM)

RAM is arranged as the banks of 8 registers each and contains the internal function registers with the direct addressing, the general purpose registers with the direct or index addressing R8, R9, RA, RB, RC, RD, RE, RF, the RAM data area with the index addressing, special registers and the data memory, directly indicated on LCD, with the index addressing.

The controller service registers are located in the address space from 0x000 to 0x007 (bank 00) and have the following purpose:

- R0, R1, R2, R3 - accumulators;
- R5, R6 - base index registers BM, BH for storage of the addressed bank number;
- R4, R7- controller status registers.

RAM data area with the capacity of 72 bytes is located in the address space from 0x008 to 0x04F (banks 01, 02, 03, 04, 05, 06, 07, 08, 09).

Table 6 –Data RAM Area

Bank	Register Number in Bank	Address	Name during Direct Addressing	Name during Index Addressing	Purpose
00	0	0x000	R0	-	Accumulator
	1	0x001	R1	-	Accumulator
	2	0x002	R2	-	Accumulator
	3	0x003	R3	-	Accumulator
	4	0x004	R4	-	Status register
	5	0x005	R5 or BM	-	Base register BM
	6	0x006	R6 or BH	-	Base register BH
	7	0x007	R7	-	Status register
01	0	0x008	R8	M0,H0	Common purpose registers
	1	0x009	R9	M1,H1	
	2	0x00A	RA	M2,H2	
	3	0x00B	RB	M3,H3	
	4	0x00C	RC	M4,H4	
	5	0x00D	RD	M5,H5	
	6	0x00E	RE	M6,H6	
	7	0x00F	RF	M7,H7	
02	0	0x010	-	M0,H0	Register RAM
	1	0x011	-	M1,H1	
	2	0x012	-	M2,H2	
	3	0x013	-	M3,H3	
	4	0x014	-	M4,H4	
	5	0x015	-	M5,H5	
	6	0x016	-	M6,H6	
	7	0x017	-	M7,H7	
03	0	0x018	-	M0,H0	Register RAM
	1	0x019	-	M1,H1	
	2	0x01A	-	M2,H2	
	3	0x01B	-	M3,H3	
	4	0x01C	-	M4,H4	
	5	0x01D	-	M5,H5	
	6	0x01E	-	M6,H6	
	7	0x01F	-	M7,H7	
04	0	0x020	-	M0,H0	Register RAM
	1	0x021	-	M1,H1	
	2	0x022	-	M2,H2	
	3	0x023	-	M3,H3	
	4	0x024	-	M4,H4	
	5	0x025	-	M5,H5	
	6	0x026	-	M6,H6	
	7	0x027	-	M7,H7	
05	0	0x028	-	M0,H0	Register RAM
	1	0x029	-	M1,H1	
	2	0x02A	-	M2,H2	
	3	0x02B	-	M3,H3	
	4	0x02C	-	M4,H4	
	5	0x02D	-	M5,H5	
	6	0x02E	-	M6,H6	
	7	0x02F	-	M7,H7	

Table 6 Continued

Bank	Register Number in Bank	Address	Name during Direct Addressing	Name during Index Addressing	Purpose
06	0	0x030	-	M0,H0	Register RAM
	1	0x031	-	M1,H1	
	2	0x032	-	M2,H2	
	3	0x033	-	M3,H3	
	4	0x034	-	M4,H4	
	5	0x035	-	M5,H5	
	6	0x036	-	M6,H6	
	7	0x037	-	M7,H7	
07	0	0x038	-	M0,H0	Register RAM
	1	0x039	-	M1,H1	
	2	0x03A	-	M2,H2	
	3	0x03B	-	M3,H3	
	4	0x03C	-	M4,H4	
	5	0x03D	-	M5,H5	
	6	0x03E	-	M6,H6	
	7	0x03F	-	M7,H7	
08	0	0x040	-	M0,H0	Register RAM
	1	0x041	-	M1,H1	
	2	0x042	-	M2,H2	
	3	0x043	-	M3,H3	
	4	0x044	-	M4,H4	
	5	0x045	-	M5,H5	
	6	0x046	-	M6,H6	
	7	0x047	-	M7,H7	
09	0	0x048	-	M0,H0	Register RAM
	1	0x049	-	M1,H1	
	2	0x04A	-	M2,H2	
	3	0x04B	-	M3,H3	
	4	0x04C	-	M4,H4	
	5	0x04D	-	M5,H5	
	6	0x04E	-	M6,H6	
	7	0x04F	-	M7,H7	

Addressing RAM Registers

R0 – R4, R5 (or BM), R6 (or BH), R8 – RF – names of RAM registers in commands during the direct addressing. For registers R0 – R7 the direct addressing only is possible. For registers
R8 – RF the direct addressing or index addressing is possible. For the remaining registers – the index addressing only.

BM, BH – base index registers (R5, R6 appropriately). During the index addressing of RAM registers the contents of the base registers determines the data bank number.

M0-M7, H0-H7 – names of RAM registers in commands during the index addressing. For names of the registers M0-M7 the data bank number is determined by the contents of the base register R5 (BM), for names of the registers H0-H7 the data bank number is determined by the contents of the base register R6 (BH). For computation of the physical address the contents of the indicated in the command base register should be multiplied by 8 with addition of a number from 0 to 7 appropriately. For instance, during writing in the command «M5» the physical address is equal to ((BM)∗8+5).

When switching on power supply, the base index registers R5, R6 are preset by the software means.

Status Register R7

Table 7 – Status register R7 bits description

Bit	Symbol	Purpose and performed action	Status at power on switching
R7_7	MFR1	1 – masking (denial) of setting to 1 of interruption request flag FR1 from timer	1
R7_6	FR3	Interruption reqwuest flag from timer (set to 1 by «event» at control input IN8 or (selection by coding) by «overflow» of bits T[9:0] after each 1024 periods of the timer input signal at R7_1=0, or by «overflow» of bits T[11:0] after each 4096 periods of the timer input signal at R7_1=1)	0
R7_5	FR2	Interruption request flag from timer (set to 1 after one period of the timer input signal after one period of the timer input signal after attaining the expected status of the timer bits T[11:4], coinciding with the code in the register RFB3)	0
R7_4	FR1	Interruption request flag from the timer (set to 1 after one period of the timer input signal after attaining the expected status of the timer bits T[7:0], coinciding with the code in the register RFB0)	0
R7_3	MFR3	1 – masking (denial) of setting to 1 of the interruption request flag FR3 from the timer or (selection by coding) from the event at the control input IN8	1
R7_2	MFR2	1 – masking (denial) of setting to 1 of the interruption request flag FR2 from timer	1
R7_1	8HZFR3	1 – interruption request from the timer by «overflow» of bits T[11:0] of the timer. 0 – interruption request from the timer by «overflow» of the bits T[9:0] of the timer or the interruption request from the event by the control input IN8	0
R7_0	FLAG	Program flag	0

Status register R4

The mask «programming» may switch off the output level (Z instead of L or (and) Z instead of H) with their possible replacement with the external resistors.

H – high level status (1);
L – low level status (0);
Z – high impedance status.

Table 8 –Status register R4 bits description

Bit	Symbol	Purpose and performed action	Status at power on switching
R4_7	DOUT4	Status of pin OUT4	1
R4_6	DOUT3	Status of pin OUT3	1
R4_5	DOUT2	Status of pin OUT2	1
R4_4	DOUT1	Status of pin OUT1	1
R4_3	FLAG	Program flag	0
R4_2	ELEN	1 – switching on the driver of the electroluminescent backlight (outputs IND, EL). 0 – switching off the driver of the electroluminescent backlight (pins IND, EL)	0
R4_1	ALEN	0 – sound denial (microcircuit pins AL=0, NAL=1). 1 – sound permission (microcircuit pins AL=1, NAL=0), if R4_0=0 or timer bitt T_2=0	0
R4_0	EN4096	1 – with sound permission, i. e. at R4_1=1, pins AL=1, NAL=0, if the timer bit T_2=0, otherwise the microcircuit pins AL=0, NAL=1, if the timer bit T_2=1. 0 – with sound permission, i. e. at R4_1=1, pins AL = 1, NAL = 0 independently on the timer bit T_2	1

LCD Driver Memory

Data, directly indicated on LCD, are located in the banks FD and FE and in the register RFB_4 of bank FB.
The multiplex level is selected by coding.

Table 9 –LCD Driver memory bits description

Memory Configuration of LCD Driver at Multiplex Level 1/4											
Bank	Register Number in Bank	Address	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	COM
FD	0	0x7E8	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM1
	1	0x7E9	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM2
	2	0x7EA	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM3
	3	0x7EB	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM4
	4	0x7EC	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM1
	5	0x7ED	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM2
	6	0x7EE	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM3
	7	0x7EF	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM4
FE	0	0x7E0	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM1
	1	0x7E1	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM2
	2	0x7E2	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM3
	3	0x7E3	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM4
	4	0x7E4	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM1
	5	0x7E5	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM2
	6	0x7E6	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM3
	7	0x7E7	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM4
FB	4	0x7DC	SEG02 COM1	SEG02 COM2	SEG02 COM3	SEG02 COM4	SEG01 COM1	SEG01 COM2	SEG01 COM3	SEG01 COM4	-

Table 9 Continued

Memory Configuration of LCD Driver at Multiplex Level 1/3											
Bank	Register Number in Bank	Address	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	COM
FD	0	0x7E8	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM1
	1	0x7E9	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM2
	2	0x7EA	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM3
	3	0x7EB	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	4	0x7EC	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM1
	5	0x7ED	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM2
	6	0x7EE	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM3
	7	0x7EF	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
FE	0	0x7E0	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM1
	1	0x7E1	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM2
	2	0x7E2	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM3
	3	0x7E3	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	4	0x7E4	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM1
	5	0x7E5	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM2
	6	0x7E6	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM3
	7	0x7E7	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
FB	4	0x7DC	SEG02 COM1	SEG02 COM2	SEG02 COM3	SEG02 RAM	SEG01 COM1	SEG01 COM2	SEG01 COM3	SEG01 RAM	-

Table 9 Continued

Memory Configuration of LCD Driver at Multiplex Level 1/2											
Bank	Register Number in Bank	Address	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	COM
FD	0	0x7E8	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM1
	1	0x7E9	SEG04	SEG06	SEG08	SEG10	SEG12	SEG14	SEG16	SEG18	COM2
	2	0x7EA	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	3	0x7EB	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	4	0x7EC	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM1
	5	0x7ED	SEG03	SEG05	SEG07	SEG09	SEG11	SEG13	SEG15	SEG17	COM2
	6	0x7EE	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	7	0x7EF	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
FE	0	0x7E0	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM1
	1	0x7E1	SEG33	SEG31	SEG29	SEG27	SEG25	SEG23	SEG21	SEG19	COM2
	2	0x7E2	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	3	0x7E3	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	4	0x7E4	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM1
	5	0x7E5	SEG34	SEG32	SEG30	SEG28	SEG26	SEG24	SEG22	SEG20	COM2
	6	0x7E6	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
	7	0x7E7	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	RAM
FB	4	0x7DC	SEG02 COM1	SEG02 COM2	SEG02 RAM	SEG02 RAM	SEG01 COM1	SEG01 COM2	SEG01 RAM	SEG01 RAM	-

Data memory, directly indicated on the LCD segments, whose maximum volume is used for LCD control at multiplex 1/4, constitutes 17 bytes or 136 bits and is located at the addresses from 0x7E8 to 0x7F7 (banks FD, FE) and by the address 0x7DC (register RFB4 in the bank FB). For LCD memory the index addressing only is possible.

Table 10 – Sequence of the signals alteration at the pins COM1, COM2, COM3, COM4 at the multiplex level 1/4

T_7	COM1	COM2	COM4	COM3
0	1	M	M	M
1	M	1	M	M
0	M	M	1	M
1	M	M	M	1
0	0	M	M	M
1	M	0	M	M
0	M	M	0	M
1	M	M	M	0

Notes
1 «1» - output level complies with U_{CC};
2 «0» - output level complies with GND;
3 «M» - output level complies with $U_{CC}/2$

Signals at the pins COM1, COM2, COM3, COM4 at the multiplex level 1/4 vary with the period of 8/256 s with each 1/256 s (with the output signal period of the timer bit T_6).

Table 11 – Sequence of the signals variation at the pins COM1, COM2, COM3, COM4 at the multiplex level 1/3

T_7	COM1	COM2	COM4	COM3
0	1	M	M	M
1	M	1	M	M
0	M	M	M	1
1	0	M	M	M
0	M	0	M	M
1	M	M	M	0

Signals at the pins COM1, COM2, COM3, COM4 at the multiplex level 1/3 vary with the period of 6/256 s with each 1/256 s (with the output signal period of the timer bit T_6).

Table 12 – Sequence of the signals variation at the pins COM1, COM2, COM3, COM4 at the multiplex level 1/2

T_7	COM1	COM2	COM4	COM3
0	1	M	M	M
1	1	M	M	M
0	M	1	M	M
1	M	1	M	M
0	0	M	M	M
1	0	M	M	M
0	M	0	M	M
1	M	0	M	M

Signals at the pins COM1, COM2, COM3, COM4 at the multiplex level of 1/2 vary with the period of 8/256 s.

When executing the command HLT for the time prior to exiting stop by interruption from the input port and for the time of the initial setting when switching on power supply, the signals at the pins COM1, COM2, COM3, COM4 are set by the equal U_{CC}, and then proceed to the initial status.

Table 13 – Initial status at the pins COM1, COM2, COM3, COM4 when switching on power supply

T_7	COM1	COM2	COM4	COM3
0	1	M	M	M

Special Registers and Interruptions

Special bank registers FB (except the register RFB_4, in which the data are located, directly indicated on LCD) are intended for interruptions control from the timer, events by the control input IN8 and from the input port.

Special block registers of the 12-bit timer T[11:0] have the addresses 0x7D8 – 0x7DB (bank FB), the input port block have the addresses 0x7DE and 0x7DF (bank FB). For the special registers the index addressing only is possible.

Table 14 – Special bank registers FB

Bank	Register Number in Bank	Address	Purpose	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0	Access
FB	0	0x7D8	Register of code comparison with the junior byte of the timer T[7:0]	KT_7	KT_6	KT_5	KT_4	KT_3	KT_2	KT_1	KT_0	Write/ read-out
	1	0x7D9	Read-out address of the timer junior byte T[7:0]	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	Read-out
	2	0x7DA	Read-out address of the timer senior byte T[11:4]	T_11	T_10	T_9	T_8	T_7	T_6	T_5	T_4	Read-out
	3	0x7DB	Register of code comparison with the timer senior byte T[11:4]	KT_11	KT_10	KT_9	KT_8	KT_7	KT_6	KT_5	KT_4	Write / read-out
	6	0x7DE	Register of EN_IR permission of interruptions from the control inputs IN8, IN7, IN6, IN5, IN4, IN3, IN2, IN1. 1 - interruption permission from control input. 0 – reset of interruption request from control input	EN_8	EN_7	EN_6	EN_5	EN_4	EN_3	EN_2	EN_1	Write / read-out
	7	0x7DF	Register read-out address of IR requests for interruption from control inputs IN8, IN7, IN6, IN5, IN4, IN3, IN2, IN1	IR_8	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	Read-out

When switchin on the power supply, the registers RFB1, RFB2, RFB6, RFB7 are reset to 0x00, and the registers RFB0, RFB3 are set by means of software.

The interruptions can be initiated by:

- interruption requests from the control inputs IN8, IN7, IN6, IN5, IN4, IN3, IN2, IN1;
- interruption requests from the timer FR1, FR2, FR3, by the interruption request FR3 from events by the control input IN8.

Interruptions are performed after completion of the command execution of the base program on arrival of the request. Interruptions are denied after the transition commands: JMP, JMI and JC, JNC, JZ, JNZ during fulfillment of the transition conditions, command of JSR return from the subprogram.

Interruptions from the port bits can be initiated, if one sets by the software means to one the appropriate bit of the interruption permission flags register in the register RFB6.

Meanwhile, read-out of the register RFB7 (access by read-out only) makes it possible to indicate, from which bits of the input port the requests are called for interruption. Request for interruption from any port bit may be reset after execution of the interruption service program by means of writing 0 to the appropriate bit in the register RFB6 with the subsequent setting of the given bit to 1 for permission of the subsequent interruption request.

As per the input type, each bit of the input port may be individually adjusted (selection by coding), as «IN RL» (resistive 0), «IN RH» (resistive 1), «IN ZL» (high impedance 0).

Irrespective of the preset by coding input port type, the requests for interruption from any port bit by the coding selection may be initiated under the external influence of the high level signal or under the external influence of the low level signal on input.

Mask «metal 1» may switch off the internal level (ZL, RL) with the possible their replacement with the external resistors.

Table 15 – Possible options of the Internal Statuses Alignment

Internal status of i-st bit of the port IN_ i	Remark
IN Z (high impedance). IN_1 ZL (high impedance 0). Internal current source 110 nA, supporting the level ZL is to be connected	Interruptions from the external influences are possible
IN RL (resistive 0). Input resistance of over 100 kOhm	

External influences can be as follows:

- H – «strong» 1;
- HR – «weak» 1;
- L – «strong» 0;
- LR – «weak» 0;
- Z – high impedance status.

Table 16 – Statuses of the port bits under all possible combinations of the external influences and the internal statuses

Internal status	External status				
	H	HR	L	LR	Z
IN RH	1	1	0	0	1
IN RL	1	1	0	0	0
OUT ZL	1	1	0	0	0

Timer

Controller has in its composition the 12-bit timer block T[11:0]. Timer is essentially the binary twelve bit counter with the division ratio 4096 with the bit weights [2048, 1024, 512, 256, 128, 64, 32, 16, 8, 4, 2, 1].

The counter status varies at the status change «0» at the counter input (low level voltage at the OSCI microcircuit pin, i. e. the GND level potential) for the status «1» (the high level voltage at the OSCI microcircuit pin, i. e. the U_{CC} level potential). The quartz clock frequency of 32768 Hz is applied to the counter input.

Status of the T[7:0] timer junior byte is accessible at the read-out address 0x7D9 (RFB1).

Table 17 - Information, read out to the data bus of the T[7:0] timer junior byte

D7	D6	D5	D4	D3	D2	D1	D0
T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0
128 Hz	256 Hz	512 Hz	1024 Hz	2048 Hz	4096 Hz	8192 Hz	16384 Hz

Status of the T[11:4] timer senior byte is accessible at the read-out address 0x7DA (RFB2).

Table 18 - Information, read out to the data bus of the T[11:4] timer senior byte

D7	D6	D5	D4	D3	D2	D1	D0
T_11	T_10	T_9	T_8	T_7	T_6	T_5	T_4
8 Hz	16 Hz	32 Hz	64 Hz	128 Hz	256 Hz	512 Hz	1024 Hz

When reading the timer there may arise the problems, related to the possibility of reading the variable data. For the correct reading it is possible, for instance, to perform the reading several times in sequence with the subsequent comparison of the results. With power supply turned on, the T[11:0] timer is reset to the status 0x000.

When executing the command HLT the T[11:0] timer is reset to the status 0x000 and is fixed in this status (under the «0» status, the OSCI input is also fixed) prior to the program start from the exetrnal influences on the input port, at which interruption is permitted.

Microcircuit commands

Table 19 – Microcircuit commands

Mnemonics	Command code															
1	2															
1 MV	1	0	1	1	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
2 MVI	1	0	0	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0
3 ORI	1	0	1	0	0	1	0 1	C3	C2	C1	C0	D4	D3	D2	D1	D0
4 AN	1	0	1	1	0	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
5 ANI	1	0	1	1	1	1	0 1	C3	C2	C1	C0	D4	D3	D2	D1	D0
6 ANI/	1	0	1	1	0	1	0 1	C3	C2	C1	C0	D4	D3	D2	D1	D0
7 XR	1	0	1	0	0	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
8 XR/	1	0	1	0	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
9 XRI	1	0	1	0	1	1	0 1	C3	C2	C1	C0	D4	D3	D2	D1	D0
10 A	1	1	1	0	0	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
11 S/	1	1	1	0	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
12 AC	1	1	1	0	0	1	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
13 SC/	1	1	1	0	1	1	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
14 S	1	1	1	1	1	0	S4	S3	S2	S1	S0	D4	D3	D2	D1	D0
15 AI	0	0	1	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0
16 SI/	1	1	0	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0
17 AIC	0	1	1	C7	C6	C5	C4	C3	C2	C1	C0	D4	D3	D2	D1	D0
18 MVB	0	0	0	1	R3/R2	SB2	SB1	SB0	DB2	DB1	DB0	D4	D3	D2	D1	D0
19 TBL	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0
20 JMI	1	1	1	1	0	1	0	0	X7	X6	X5	X4	X3	X2	X1	X0
21 JMP	0	0	0	0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
22 JZ	0	1	0	0	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
23 JNZ	0	1	0	0	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
24 JC	0	1	0	1	1	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
25 JNC	0	1	0	1	0	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
26 JSR	1	1	1	1	1	1	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
27 RTI	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
28 RTN	1	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0
29 WT	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
30 HLT	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Table 19 Continued

Mnemonics	Executed operations	Preset flags of operation result	
3	4	5	
1 MV	(Rd) <= (Rs)	-	Z
2 MVI	(Rd) <= C7-0	-	Z
3 ORI	(Rd) <= (Rd) OR C3C2C1C0 0000 (writing 1) (Rd) <= (Rd) OR 0000 C3C2C1C0	-	Z
4 AN	(Rd) <= (Rd) AND (Rs)	-	Z
5 ANI	(Rd) <= (Rd) AND C3C2C1C0 1111 (writing 0) (Rd) <= (Rd) AND 1111 C3C2C1C0	-	Z
6 ANI/	<= (Rd) AND C3C2C1C0 0000 (analysis <= (Rd) AND 0000 C3C2C1C0 bit)	-	Z
7 XR	(Rd) <= (Rd) XR (Rs)	-	Z
8 XR/	<= (Rd) XR (Rs) (comparison of registers)	-	Z
9 XRI	(Rd) <= (Rd) XR C3C2C1C0 0000 (inversion (Rd) <= (Rd) XR 0000 C3C2C1C0 bit)	-	Z
10 A	(Rd) <= (Rd) + (Rs)	CF	Z
11 S/	<= (Rd) + N(Rs) + 1	CF	Z
12 AC	(Rd) <= (Rd) + (Rs) + CF	CF	RZ
13 SC/	<= (Rd) + N(Rs) + CF	CF	RZ
14 S	(Rd) <= (Rd) + N(Rs) + 1	CF	Z
15 AI	(Rd) <= (Rd) + C7-0	CF	Z
16 SI/	<= (Rd) + NC7-0 + 1	CF	Z
17 AIC	(Rd) <= (Rd) + C7-0 +CF	CF	RZ
18 MVB	(Rd) <= MV bit from (R3) or (R2)	-	-
19 TBL	(Adr.ROM) <= (R1, R0) (R2) <= ROM 7 –0 (R3) <= ROM 15 –8 (PC) <= (PC)+1	-	-
20 JMI	(PC7-0) <= (R0) (PC15-8) <= X 7-0	-	-
21 JMP	(PC11-0) <= X 11-0 (PC15-12) IS MAINTAINED	-	-
22 JZ	(PC10-0) <= X 10-0 if Z=1 (PC15-11) MAINTAINED if Z=1 (PC) <= (PC)+1 if Z=0	-	-
23 JNZ	(PC10-0) X 10-0 if Z=0 (PC15-11) MAINTAINED if Z=0 (PC) (PC)+1 if Z=1	-	-
24 JC	(PC10-0) <= X 10-0 if CF=1 (PC15-11) MAINTAINED if CF=1 (PC) <= (PC)+1 if CF=0	-	-
25 JNC	(PC10-0) <= X 10-0 if CF=0 (PC15-11) MAINTAINED if CF=0 (PC) <= (PC)+1 if CF=1	-	-
26 JSR	(STACK) <= (PC)+1 SP=SP+1 (PC1-0) <= 00 (PC11-2) <= X 9-0	-	-
	(PC15-12) MAINTAINED	-	-
27 RTI	(PC) <= (STACK) SP=SP-1	-	-
28 RTN	(PC) <= (STACK) SP=SP-1	-	-
29 WT	Program stop, stand-by	-	-
30 HLT	Program stop, timer reset and oscillator stop	-	-

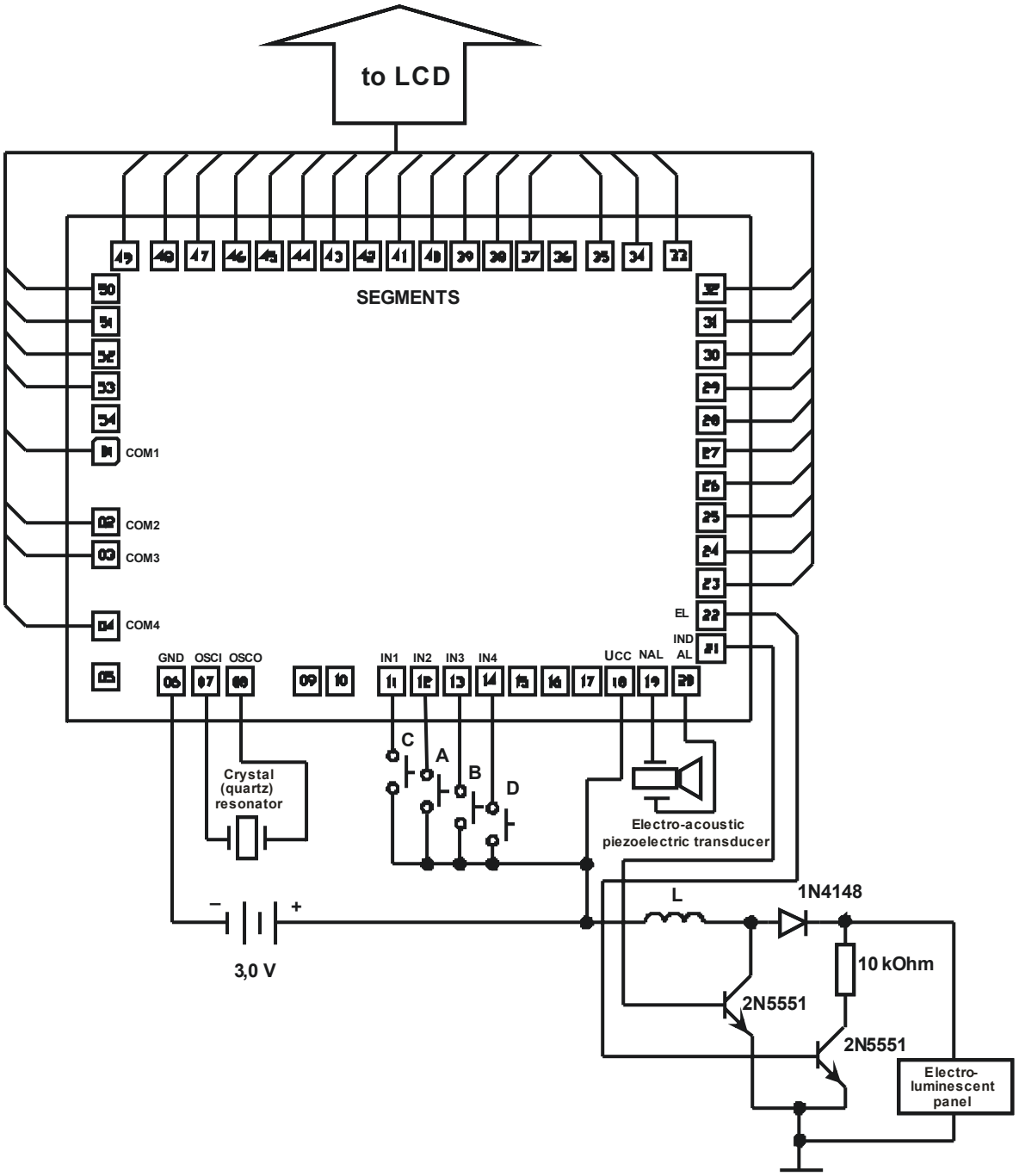
Table 19 Continued

Notes

1 PC – programmable counter.
2 STACK – seven level stack.
3 SP – stack indicator.
4 CF – transfer flag.
5 Z – zero result flag.
6 RZ – indicates, that in the given commands the flag Z can be reset only with the different from zero result (if it had been set in the previous commands to 1)

Table 20 – Address field codes of operands (D4D3)/(S4S3) addressing types

Address field code of operands D4D3 / S4S3	Type of addressing
00	Direct addressing, bank 00
01	Direct addressing, bank 01
10	Index addressing, index from register R5
11	Index addressing, index from register R6

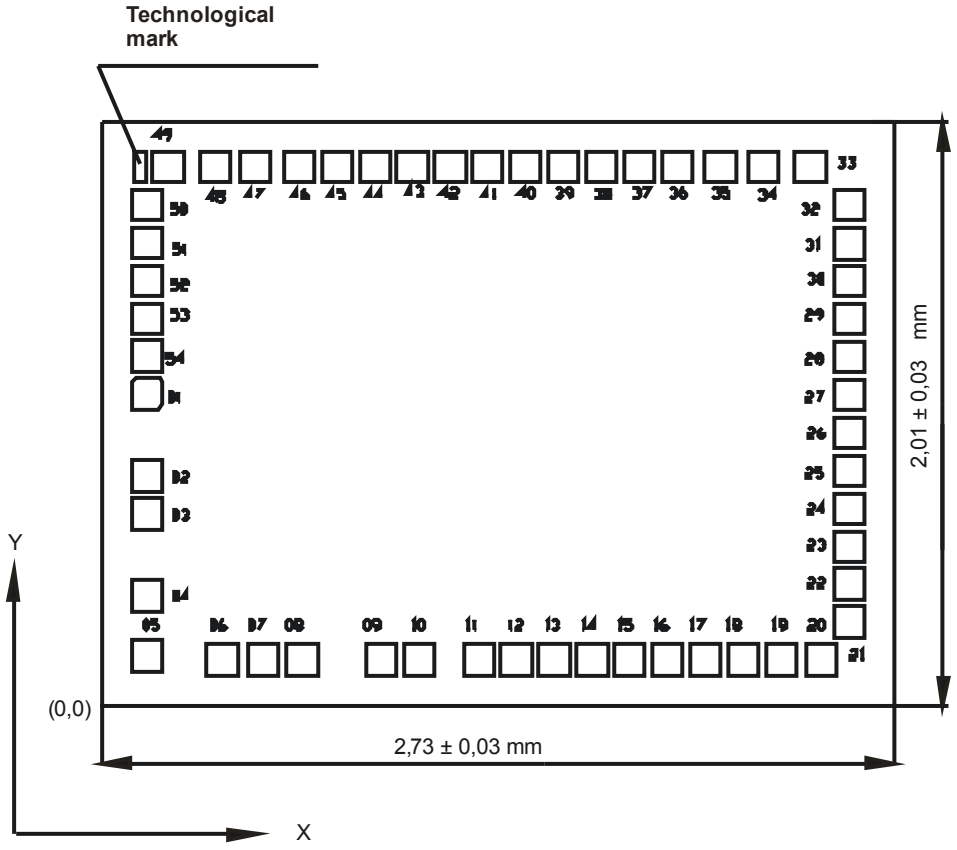


The crystal resonator applied with a microcircuit should have following characteristics:
- Frequency of a resonance f_P = 32768 Hz at load capacity C_L = 6 pF;
- Dynamic resistance $R_S \leq$35 kOhm;
- Q-factor Q ≥35000;
- Static capacity $C_O \leq$2,5 pF;
- Dynamic capacity C_I 0,≤004 pF.

Figure 2 –Application diagram
(ROM coding with the functions of the electronic wrist watch with the five program alarm, stopwatch and timer)

Location diagram of contact pads

Delivery of microcircuits is performed on the common wafer, undiced.
Mass of microcircuits is not over 0,01 g.



Chip thickness (0,46 ± 0,02) mm.
Process marking on the chip 7013 with the coordinates, mm: x=0,157, y=1,830.

Figure 3 – Location diagram of contact pads

Table 21 – Coordinates and sizes of contact pads

Number of contact pad	Coordinates (left bottm corner), μm	
	X	Y
01	0,105	1,020
02	0,105	0,738
03	0,105	0,608
04	0,105	0,325
05	0,105	0,119
06	0,363	0,105
07	0,503	0,105
08	0,638	0,105
09	0,909	0,105
10	1,039	0,105
11	1,246	0,105
12	1,376	0,105
13	1,506	0,105
14	1,636	0,105
15	1,766	0,105
16	1,896	0,105
17	2,026	0,105
18	2,156	0,105
19	2,286	0,105
20	2,423	0,105
21	2,520	0,236
22	2,520	0,366
23	2,520	0,496
24	2,520	0,626
25	2,520	0,756
26	2,520	0,886
27	2,520	1,026
28	2,520	1,146
29	2,520	1,276
30	2,520	1,406
31	2,520	1,536
32	2,520	1,671
33	2,387	1,800
34	2,227	1,800
35	2,077	1,800
36	1,927	1,800

Table 21 Continued

Number of contact pad	Coordinates (left bottom corner), μm	
	X	Y
37	1,797	1,800
38	1,667	1,800
39	1,537	1,800
40	1,407	1,800
41	1,277	1,800
42	1,147	1,800
43	1,017	1,800
44	0,887	1,800
45	0,757	1,800
46	0,627	1,800
47	0,477	1,800
48	0,337	1,800
49	0,177	1,800
50	0,105	1,670
51	0,105	1,540
52	0,105	1,410
53	0,105	1,280
54	0,105	1,150
Note – Coordinates and size of contact pads 0,092 x 0,092 mm are given by the layer «Passivation»		