40CH Segment/Common Driver for DOT MATRIX LCD

IZ7065

Features

- Display driving bias: static -1/5
- Power supply voltage: +5V ± 10%,
  +3V ± 10%
- Supply voltage for display: 0 ~ -5V(V_{EE})
- Interface

Driver (cascade connection)	Controller
Other IZ7065	IZ7066 KS0066 HD44780 SED1278

- CMOS Process
- Bare chip available

Functions

- Dot matrix LCD driver with 40 channel output.
- Selectable function to use common/segment drivers simultaneously.
- Input/Output signal
- output: 20 × 2 channel waveform for LCD driving
- input: - Serial display data and control pulse from the controller LSI.
- Bias voltage (V1-V6)

Introduction

The IZ7065 is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 20 × 2 bit bidirectional shift register, 20 × 2 bit data latch and 20 × 2 bit driver (refer to Fig 1). This LSI can be used a common or segment driver.

Block Diagram

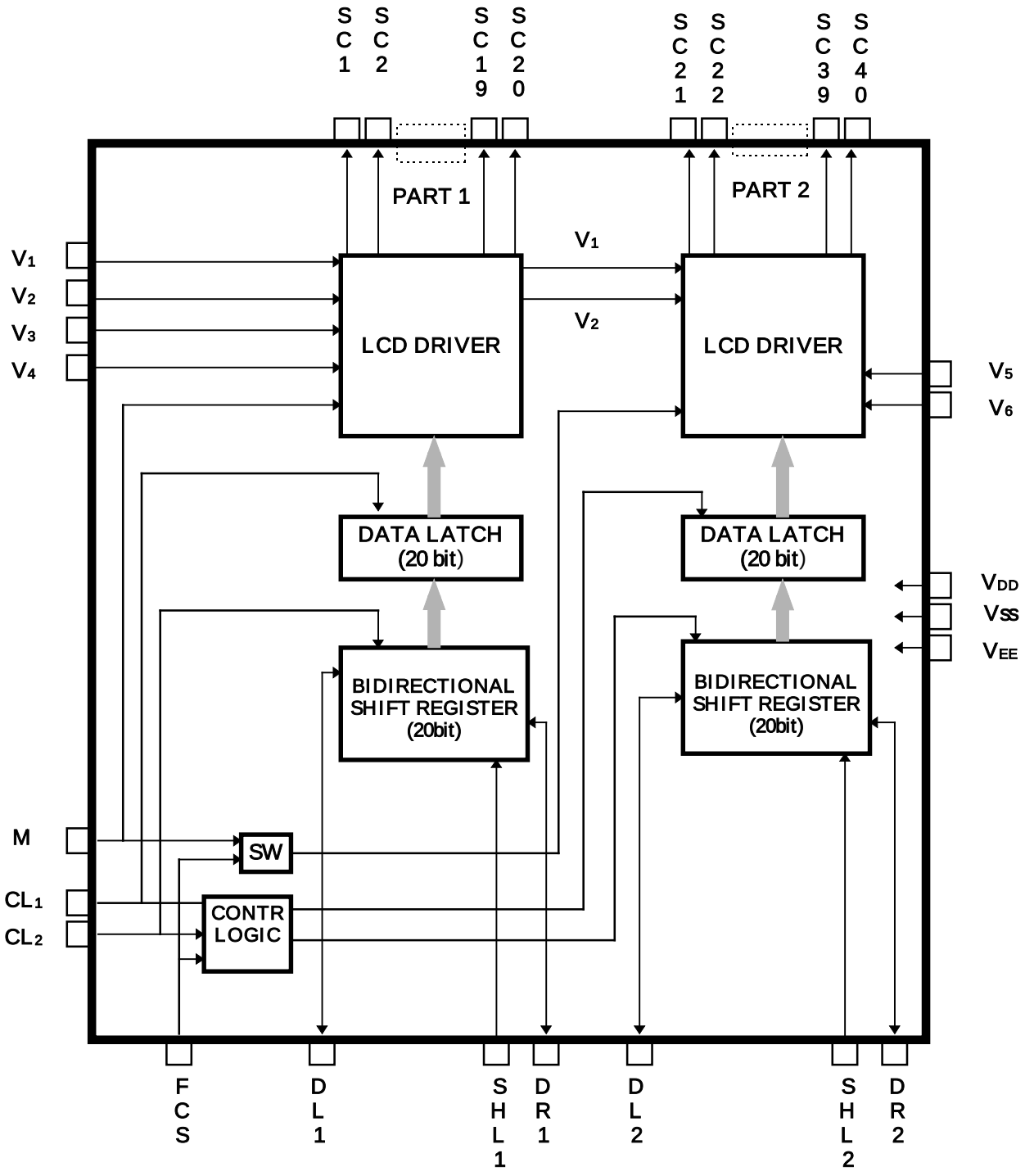


Figure 1. IZ7065 functional block diagram.

Pin Description

<table>
<tr><th>PIN(NO.)</th><th>INPUT/
OUTPUT</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTER-
FACE</th></tr>
<tr><td>V_{DD} (24)</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (+5 V ± 10%, +3 V ± 10%)</td><td rowspan="3">Power
Supply</td></tr>
<tr><td>GND (34)</td><td>0 V (GND)</td></tr>
<tr><td>V_{EE} (31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit (-5 V)</td></tr>
<tr><td>V_1 V_2
(44,45)</td><td>Input</td><td colspan="2">Bias Voltage</td><td>Bias voltage level for LCD drive (select level)</td><td>Power</td></tr>
<tr><td>SC_1÷SC_{20}</td><td>Output</td><td rowspan="4">PART 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V_3 V_4
(46,47)</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (nonselect level)</td><td>Power</td></tr>
<tr><td>SHL1
(41)</td><td>Input</td><td>Data interface</td><td>Selection of the shift direction of Part 1 shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD}
or
V_{SS}</td></tr>
<tr><td>DL1,DR1
(35,36)</td><td>Input/Output</td><td>Data input/output of Part 1 shift register</td><td>Controller
or
IZ7065</td></tr>
<tr><td>SC_{21}÷SC_{40}</td><td>Output</td><td rowspan="4">PART 2</td><td>LCD driver</td><td>LCD driver output</td><td></td></tr>
<tr><td>V_5 V_6
(48,49)</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (nonselect level)</td><td>Power</td></tr>
<tr><td>SHL2
(42)</td><td>Input</td><td>Data interface</td><td>Selection of the shift direction of Part 2 shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD}
or
V_{SS}</td></tr>
<tr><td>DL2,DR2
(37,38)</td><td>Input/Output</td><td>Data input/output of Part 2 shift register</td><td>Controller
or
IZ7065B</td></tr>
<tr><td>M
(40)</td><td>Input</td><td colspan="2">Alternated
signal for LCD

driver output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M
polarity</th></tr><tr><td>1</td><td>V_{SS}</td><td rowspan="2">latch
clock
(⎍‾)</td><td rowspan="2">shift clock
(⎍‾)</td><td rowspan="2">M</td></tr><tr><td>V_{DD}</td></tr><tr><td>2</td><td>V_{SS}</td><td rowspan="2">shift clock
(‾⎍)</td><td rowspan="2">latch clock
(‾⎍)</td><td rowspan="2">$\overline{M}$</td></tr><tr><td>V_{DD}</td></tr></table>Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level , user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.</td><td>Controller</td></tr>
<tr><td>CL1,CL2
(32,33)</td><td>Input</td><td colspan="2">Data shift / latch clock</td><td>Controller</td></tr>
<tr><td>FCS
(43)</td><td>Input</td><td colspan="2">Mode selection</td><td>Controller</td></tr>
<tr><td>NC(39)</td><td></td><td colspan="2"></td><td>No connection pin</td><td>N.C</td></tr>
</table>

Maximum Absolute Limit (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3 ~ **7**.0	V
Driver Supply Voltage	V_{LCD}	V_{DD} - 13.5 ~ V_{DD} + 0.3	V
Input Voltage 1	V_{IN1}	- 0.3 ~ V_{DD} + 0.3	V
Input Voltage 2 (V_1-V_6)	V_{IN2}	V_{DD} + 0.3 ~ V_{EE} - 0.3	V
Operating Temperature	T_{OPR}	-30 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +125	°C

Voltage greater than above may damage to then circuit.
V_{EE}: connect protection resistor (220Ω ± 5%)
* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Electrical Characteristics

DC characteristics (V_{DD}=2.7~5.5V, V_{DD} - V_{EE} =3~13V, V_{SS}=0V, Ta=-30 ~ +85°C)

Characteristic	Symbol	Test Condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	f_{CL2}=400KHz	-	1	mA	-
Supply Current *	I_{EE}	f_{CL1}=1KHz	-	10	μA	
Input High Voltage	V_{IH}	-	0.7V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2,
Input Low Voltage	V_{IL}		0	0.3V_{DD}		DR1, DR2,
Input Leakage Current	I_{LKG}	V_{IN} =0-V_{DD}	-5	5	μA	SHL1, SHL2, M, FCS
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	V_{DD}-0.4	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	I_{OL} = +0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON}=0.1mA for one of SC1-SC40	-	1.1		V(V_1-V_6), SC(SC_1-SC_{40})
	V_{D2}	I_{ON}=0.5mA for each SC1-SC40	-	1.5		
Leakage Current	I_V	V_{IH}= V_{DD}~ V_{EE} (Output SC1-SC40:floating)	-10	10	μA	V_1-V_6

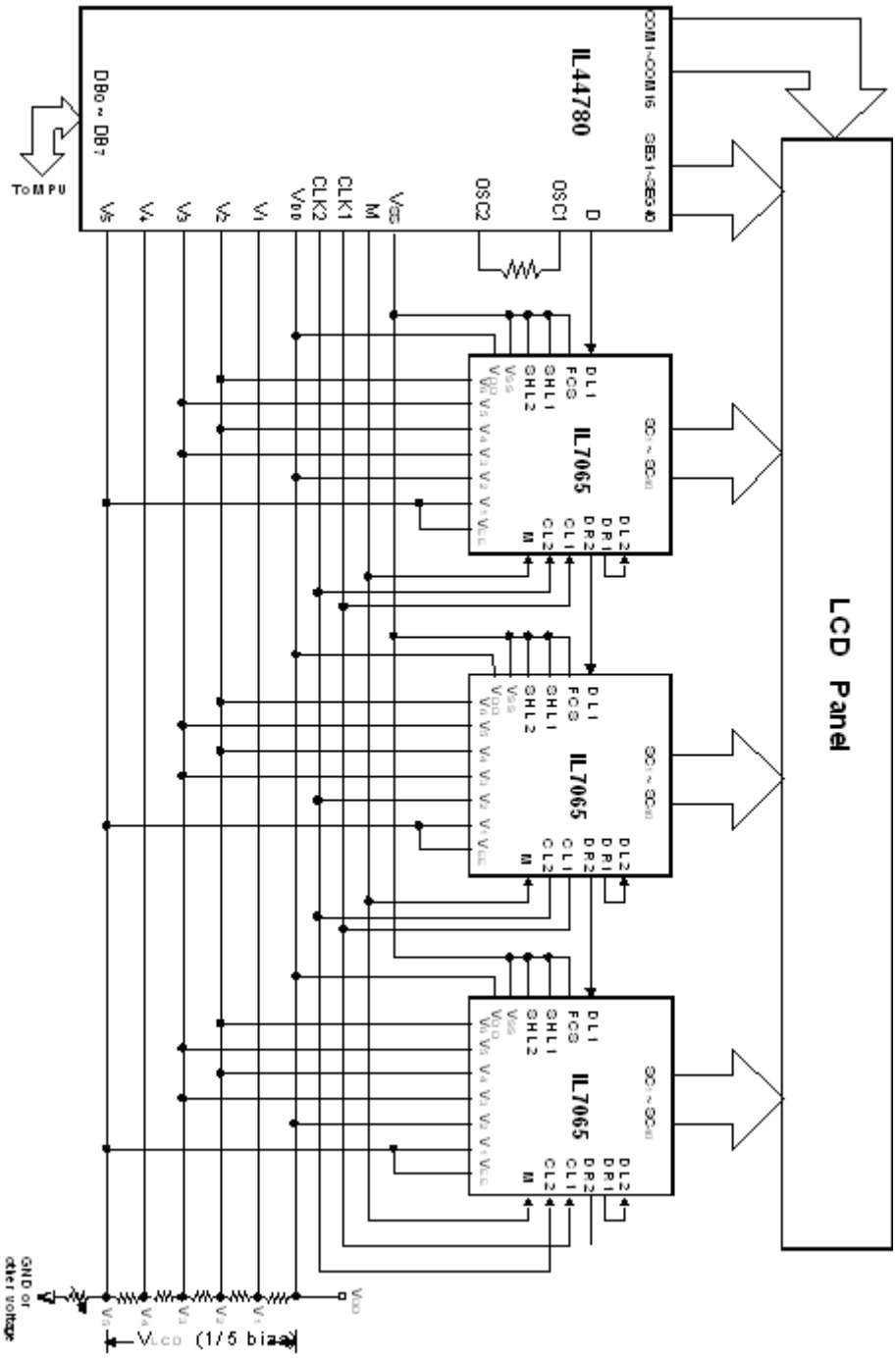
* V_{DD}-V_{EE}=4V

AC characteristics (V_{DD}=2.7~5.5V, V_{DD} - V_{EE} =3~13V, V_{SS}=0V, Ta=-30 ~ +85°C)

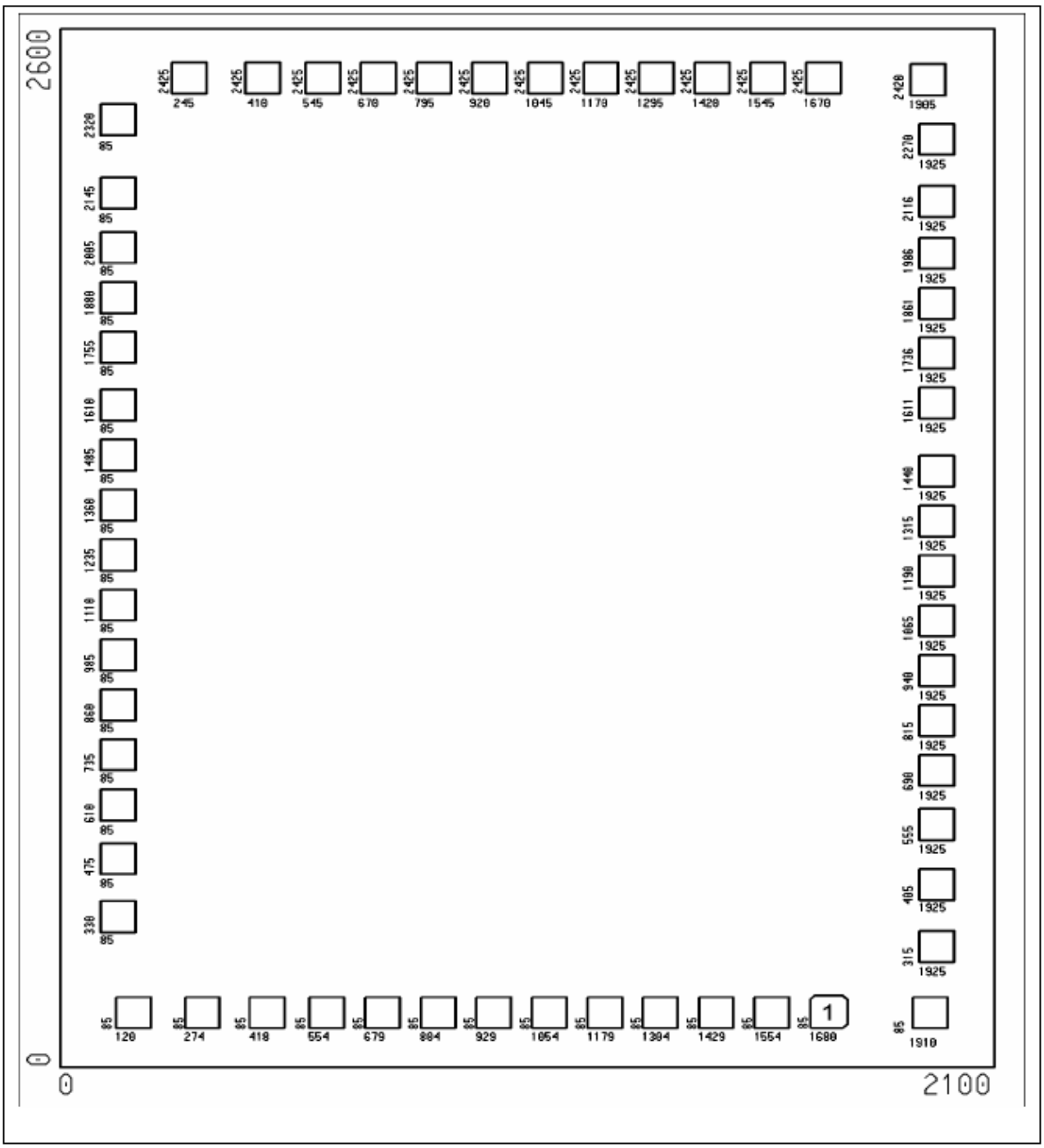
Characteristic	Symbol	Test Condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	KHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{LS}	from CL2 to CL1	500	-		CL1, CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DL1, DL2, DR1, DR2,
Data Hold Time	t_{DH}	-	300	-		FLM
Data Delay Time	t_D	CL=15pF	-	500		DL1, DL2, DR1, DR2

Input/Output current excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at “H” or “L”.

Application Circuit



Pad Diagram



Chip size: 2100 x 2600 µm
Pad size : 92 x 92 µm

Pad Location

Unit (um)

PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y
1	V_{EE}	1680	85	31	SC_{28}	245	2425
2	CL_1	1910	85	32	SC_{27}	85	2320
3	CL_2	1925	315	33	SC_{26}	85	2145
4	V_{SS}	1925	405	34	SC_{25}	85	2005
5	DL_1	1925	555	35	SC_{24}	85	1880
6	DR_1	1925	690	36	SC_{23}	85	1755
7	DL_2	1925	815	37	SC_{22}	85	1610
8	DR_2	1925	940	38	SC_{21}	85	1485
9	M	1925	1065	39	SC_{20}	85	1360
10	SHL_1	1925	1190	40	SC_{19}	85	1235
11	SHL_2	1925	1315	41	SC_{18}	85	1110
12	FCS	1925	1440	42	SC_{17}	85	985
13	V_1	1925	1611	43	SC_{16}	85	860
14	V_2	1925	1736	44	SC_{15}	85	735
15	V_3	1925	1861	45	SC_{14}	85	610
16	V_4	1925	1986	46	SC_{13}	85	475
17	V_5	1925	2116	47	SC_{12}	85	330
18	V_6	1925	2270	48	SC_9	120	85
19	SC_{40}	1905	2420	49	SC_{10}	274	85
20	SC_{39}	1670	2425	50	SC_{11}	418	85
21	SC_{38}	1545	2425	51	SC_8	554	85
22	SC_{37}	1420	2425	52	SC_7	679	85
23	SC_{36}	1295	2425	53	V_{DD}	804	85
24	SC_{35}	1170	2425	54	SC_6	929	85
25	SC_{30}	1045	2425	55	SC_5	1054	85
26	SC_{31}	920	2425	56	SC_4	1179	85
27	SC_{32}	795	2425	57	SC_3	1304	85
28	SC_{33}	670	2425	58	SC_2	1429	85
29	SC_{34}	545	2425	59	SC_1	1554	85
30	SC_{29}	410	2425				