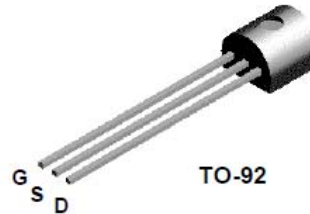


J105 / J106 / J107 N-Channel Switch

Description

This device is designed for analog or digital switching applications where very low on resistance is mandatory. Sourced from Process 59.



Ordering Informations

| Part Number | Marking | Package | Packing Method |
|-------------|---------|----------|----------------|
| J105 | J105 | TO-92 3L | Bulk |
| J106 | J106 | | |
| J107 | J107 | | |

Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Value | Units |
|----------------|--|-------------|------------------|
| V_{DG} | Drain-Gate Voltage | 25 | V |
| V_{GS} | Gate-Source Voltage | -25 | V |
| I_{GF} | Forward Gate Current | 10 | mA |
| T_J, T_{stg} | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ\text{C}$ |

Notes:

1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. These ratings are based on a maximum junction temperature of 150°C .
3. These are steady-state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics⁽⁴⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Maximum | Units |
|-----------------|---|---------|---------------------------|
| P_D | Power Dissipation | 625 | mW |
| | Derate above 25°C | 5.0 | mW/ $^\circ\text{C}$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 125 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 357 | $^\circ\text{C}/\text{W}$ |

Note:

4. PCB board size FR-4 76 x 114 x 0.6T mm³ (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Max | Units | |
|-------------------------------------|--|---|------|------|-------|----------|
| OFF CHARACTERISTICS | | | | | | |
| $V_{(BR)GSS}$ | Gate-Source Breakdown Voltage | $I_G = -10 \mu\text{A}, V_{DS} = 0$ | -25 | | V | |
| I_{GSS} | Gate Reverse Current | $V_{GS} = -15 \text{ V}, V_{DS} = 0$ | | -3.0 | nA | |
| | | $V_{GS} = -15 \text{ V}, V_{DS} = 0, T_A = 100^\circ\text{C}$ | | -200 | | |
| $I_{D(off)}$ | Gate-Source Cut-Off Voltage | $V_{DS} = -5.0 \text{ V}, V_{GS} = -10 \text{ V}$ | | 3.0 | nA | |
| $V_{GS(off)}$ | Gate-Source Cut-Off Voltage | $V_{DS} = 5.0 \text{ V}, I_D = 1.0 \text{ mA}$ | J105 | -4.5 | -10.0 | V |
| | | | J106 | -2.0 | -6.0 | |
| | | | J107 | -0.5 | -4.5 | |
| ON CHARACTERISTICS | | | | | | |
| I_{DSS} | Zero-Gate Voltage Drain Current ⁽⁵⁾ | $V_{DS} = 15 \text{ V}, I_{GS} = 0$ | J105 | 500 | | mA |
| | | | J106 | 200 | | |
| | | | J107 | 100 | | |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0$ | J105 | | 3.0 | Ω |
| | | | J106 | | 6.0 | |
| | | | J107 | | 8.0 | |
| SMALL SIGNAL CHARACTERISTICS | | | | | | |
| $C_{dg(on)}$ | Drain-Gate On Capacitance | $V_{DS} = 0, V_{GS} = 10 \text{ V}, f = 1.0 \text{ MHz}$ | | 160 | pF | |
| $C_{sg(on)}$ | Source-Gate On Capacitance | | | | | |
| $C_{dg(off)}$ | Drain-Gate Off Capacitance | | | 35 | pF | |
| $C_{sg(off)}$ | Source-Gate Off Capacitance | | | | pF | |

Note:

5. Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2.0\%$.

Typical Performance Characteristic

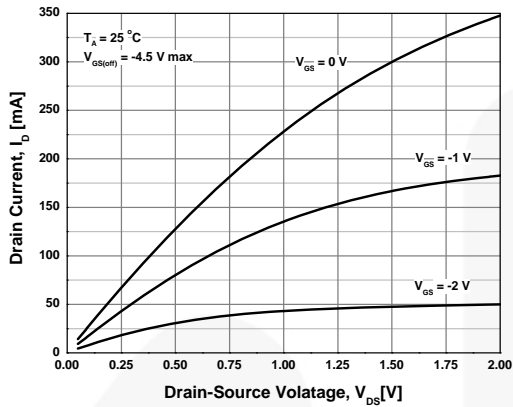


Figure 1. Common Drain-Source Characteristics

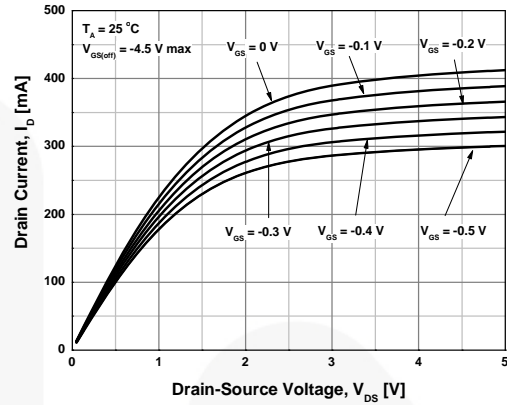


Figure 2. Common Drain-Source Characteristics

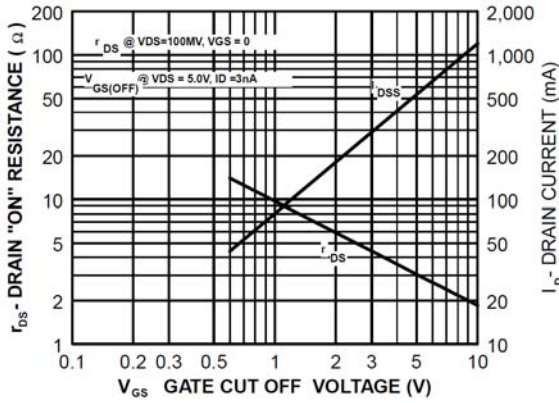


Figure 3. Parameter Interactions

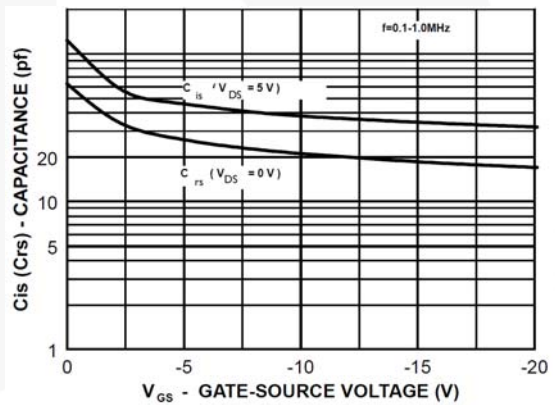


Figure 4. Capacitance vs. Voltage

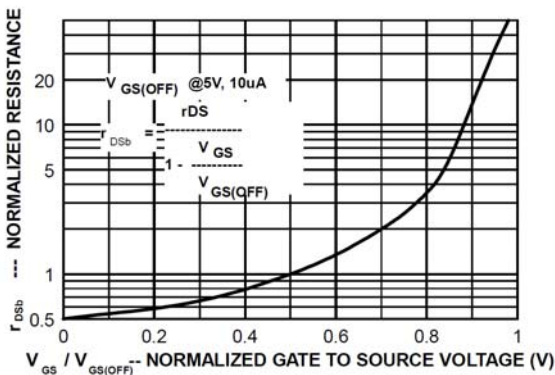


Figure 5. Normalized Drain Resistance vs. Bias Voltage

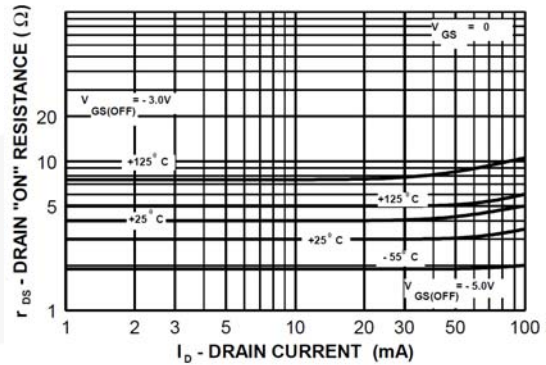


Figure 6. On Resistance vs. Drain Current

Typical Performance Characteristic (Continued)

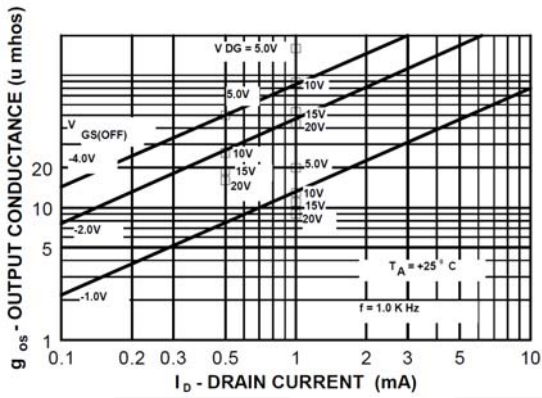


Figure 7. Output Conductance vs. Drain Current

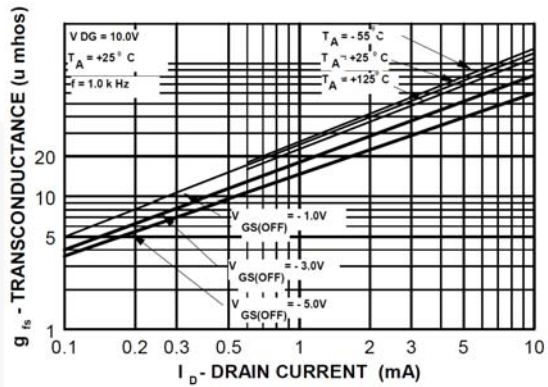


Figure 8. Transconductance vs. Drain Current

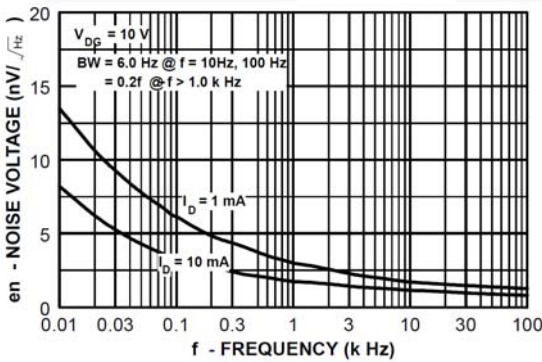


Figure 9. Noise Voltage vs. Frequency

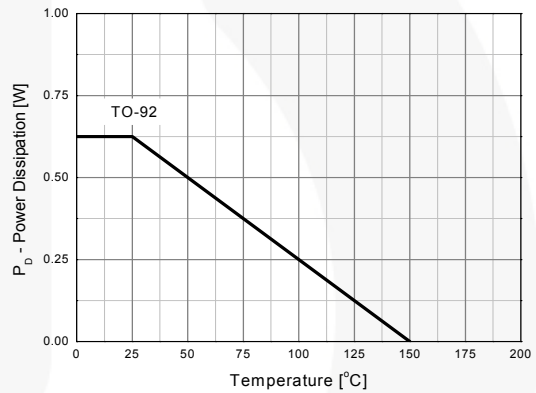
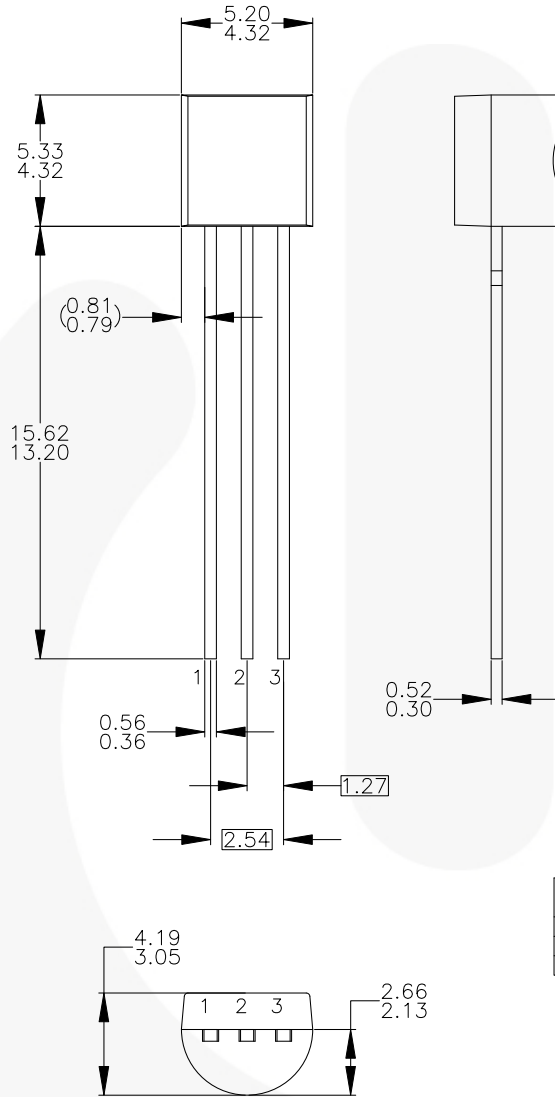


Figure 10. Power Dissipation vs. Ambient Temperature

Physical Dimensions

TO-92



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

| Pin | 92 | | | 94 | | | 96 | | | 97 | | | 98 | | |
|-----|----|---|---|----|---|---|----|---|---|----|---|---|----|---|---|
| | P | F | M | P | F | M | B | F | M | P | F | M | P | F | M |
| 1 | E | S | S | E | S | S | B | D | G | C | G | D | C | G | D |
| 2 | B | D | G | C | G | D | E | S | S | B | D | G | E | S | S |
| 3 | C | G | D | B | D | G | C | G | D | E | S | S | B | D | G |

LEGEND:
 P - BIPOLAR E - EMITTER D - DRAIN
 F - JFET B - BASE S - SOURCE
 M - DMOS C - COLLECTOR G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 11. 3-LEAD, TO-92, MOLDED, STD STRAIGHT LD (NO EOL CODE)






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