n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NIP See Section 4

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Low Noise Audio Amplifiers**

BENEFITS

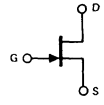
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $r_{DS(on)} < 8\ \Omega$ (J108)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{d(on)} + t_r = 5$ ns Typical
- Low Noise
  $\overline{e_n} = 6\ nV/\sqrt{Hz}$ at 10 Hz, Typ (J110)

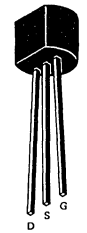
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25° C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . .300°C

Plastic

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J108 Min	J108 Typ	J108 Max	J109 Min	J109 Typ	J109 Max	J110 Min	J110 Typ	J110 Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–3'			–3			–3	nA	$V_{DS} = 0$ V, $V_{GS} = -15$ V
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–3		–10	–2		–6	–0 5		–4	V	$V_{DS} = 5$ V, $I_D = 1\ \mu$A
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	$V_{DS} = 0$ V, $I_G = -1\ \mu$A
4	STATIC	I_{DSS}	Drain Saturation Current (Note 2)	80			40			10			mA	$V_{DS} = 15$ V, $V_{GS} = 0$ V
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance J110A			8			12			18 25	Ω	$V_{DS} \leq 0\ 1$ V, $V_{GS} = 0$ V
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85	pF	$V_{DS} = V_{GS} = 0$; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn ON Delay Time		4			4			4		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		1			1			1		ns	J108 / J109 / J110
12	DYNAMIC	$t_{d(off)}$	Turn OFF Delay Time		6			6			6		ns	V_{DD} 1 5 V / 1.5 V / 1.5 V
13	DYNAMIC	t_f	Fall Time		30			30			30		ns	$V_{GS(off)}$ –12 V / –7 V / –5 V
														R_L 150 Ω / 150 Ω / 150 Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs, duty cycle ≤ 3%

NIP

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