

# quad-ring demodulator designed for . . .



**Performance Curves NZA**  
See Section 4

**BENEFITS**

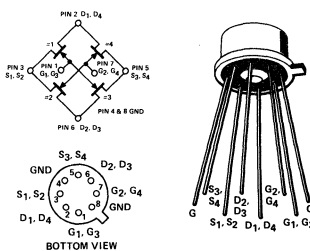
- Four Matched U310 FETs
- High IMD Intercept Point
- Low Turn-ON Resistance
- Conversion Gain
- High 1 dB Compression
- Suitable for PC Board Construction

- VHF Double-Balanced Mixers
- Analog Multipliers

TO-99  
See Section 5

**ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . -25 V  
 Gate Current . . . . . 25 mA  
 Total Continuous Power Dissipation  
 at (or Below) 25°C Free Air Temperature  
 (Derate 8.0 mW/°C to 150°C) . . . . . 1 W  
 Storage Temperature Range . . . . . -65 to +150°C  
 Lead Temperature  
 (1/16" from case for 10 seconds) . . . . . 300°C



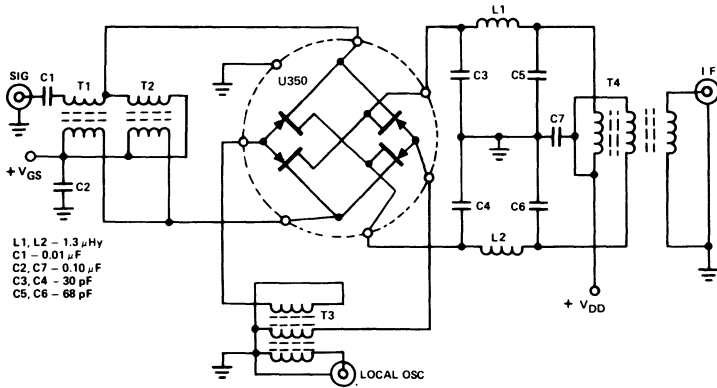
**ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic		U350			Unit	Test Conditions	
		Min	Typ	Max			
1 2 S	IGSS	Gate Reverse Current		-1	nA	VGS = -15 V, VDS = 0 (Note 1)	TA = +125°C
				-1	µA		
3 T A	BVGS	Gate-Source Breakdown Voltage		-25		IG = -1 µA, VDS = 0	
4 T I	VGS(off)	Gate-Source Cutoff Voltage		-2	-6	ID = 1 nA, VDS = 10 V (Note 1)	
5 C	VGS(f)	Gate-Source Forward Voltage			1	IG = 1 mA, VDS = 0 (Note 1)	
6	IDSS	Drain Saturation Current		24	60	mA	VDS = 15 V, VGS = 0 (Notes 1 and 2)
7 D Y	9fs	Common-Source Forward Transconductance		10	18	mΩ	VDS = 10 V, ID = 10 mA
8 N	9os	Common-Source Output Conductance			150	µΩ	
9 A	Cgs	Gate-Source Capacitance			5	pF	VGS = -10 V, ID = 0
10 M I	Cgd	Drain Gate Capacitance			2.5	pF	VGD = -10 V, IS = 0
11 C	Rds(on)	Drain-Source ON Resistance		50	90	Ω	VGS = 0, ID = 0
12 H	Gc	(Conversion Gain)			4		VDS = 20 V, VGS = ½VGS(off), RD = 1,700 Ω
13 F	NF	Noise Figure			7		f = 100 MHz (Note 3)
14 M A T	IDSS/IDSS	Saturation Drain Current Ratio		0.9	1.0		VDS = 15 V, VGS = 0 (Note 2)
		VGS(off)/VGS(off)	Gate-Source Cutoff Voltage Ratio		0.9	1.0	
16 C H	9fs/9fs	Common-Source Forward Transconductance		0.9	1.0		VDS = 15 V, ID = 10 mA
		9os/9os	Differential Output Conductance		0.9	1.0	

**NOTES:**

1. Other gate terminal clamped to -8 V
2. Pulse test: PW 300 µsec DC ≤ 3 %.
3. See Figure 1.

**NZA**



Double-Balanced Mixer using U350\*  
 Figure 1

\*Reference Siliconix application note AN73-4