monolithic dual n-channel JFETs *designed for . . .*

- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NNR See Section 4

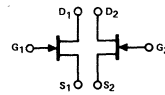
BENEFITS

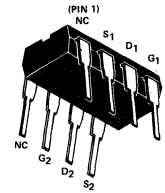
- Low Cost, Automated Insertion Package
- Minimum System Error and Calibration
  - 5 mV Offset Maximum (J401)
  - 95 dB Minimum CMRR (J401-04)
- Low Drift with Temperature
  - 10 μV/°C Maximum (J401, 02)
- Operates from Low Power Supply Voltages
  - $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  - Output Conductance < 2 μmho
- Low Noise
  - $\overline{e_n}$ = 6 nV/√Hz at 10 Hz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 50 V
Forward Gate Current . . . . . 10 mA
Device Dissipation (each side)
@ T_A = 85°C derate 7.5 mW/°C . . . . . 300 mW
Total Device Dissipation
@ T_A = 85°C derate 11 mW/°C . . . . . 500 mW
Storage Temperature Range . . . . . −55 to +150°C

8-Pin Mini DIP
See Section 5





ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

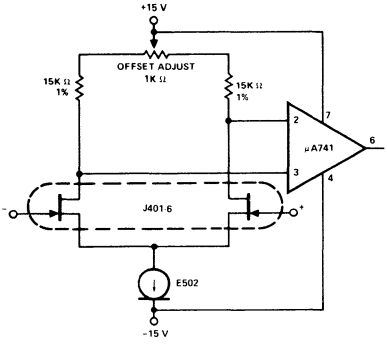
		Characteristic		J401 Min	J401 Max	J402 Min	J402 Max	J403 Min	J403 Max	J404 Min	J404 Max	J405 Min	J405 Max	J406 Min	J406 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
2		I_{GSS}	Gate Reverse Current (Note 1)		−100		−100		−100		−100		−100		−100	pA	V_{DS} = 0, V_{GS} = −30 V	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	V_{DS} = 15 V, I_D = 1 nA	
4		V_{GS}	Gate-Source Voltage (on)		−2.3		−2.3		−2.3		−2.3		−2.3		−2.3		V_{DG} = 15 V, I_D = 200 μA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6		I_G	Gate Current (Note 1)		−100		−100		−100		−100		−100		−100	pA	V_{DG} = 15 V,	
7					−60		−60		−60		−60		−60		−60	nA	I_D = 200 μA	T_A = 125°C
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 μA	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
11		g_{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600		V_{DG} = 15 V, I_D = 200 μA	
12		g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
13		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
15		$\overline{e_N}$	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA	
17		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA	
18		$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	μV/°C	V_{DG} = 10 V, I_D = 200 μA	T_A = −55°, T_B = +25°, T_C = +125°C

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.
4. Measured at end points, T_A, T_B and T_C.

NNR

APPLICATIONS

Inexpensive All-Epoxy
General Purpose FET Input Op Amp



For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

FET Input Instrumentation Amplifier

L144CJ
Instrumentation Amplifier