monolithic dual n-channel JFETs *designed for . . .*

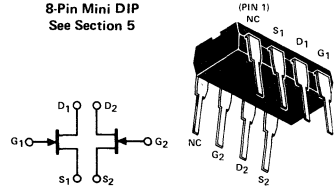
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NQP
See Section 4

BENEFITS

- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (J410)
  70 dB Minimum CMRR (J410)
- Low Drift with Temperature
  10 μV/°C Maximum (J410)
- Simplifies Amplifier Design
  Low Output Conductance
- Automatic Insertion Package

8-Pin Mini DIP
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage ..... ±40 V
Gate-Drain or Gate-Source Voltage ..... −40 V
Gate Current ..... 50 mA
Total Package Dissipation (25°C Free-Air) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... −55 to +125°C
Operating Temperature Range ..... −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) ... 260°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J410 Min	J410 Typ	J410 Max	J411 Min	J411 Typ	J411 Max	J412 Min	J412 Typ	J412 Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current (Note 1)			−250			−250			−250	pA	V_{DS} = 0 V_{GS} = −30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−3.5	−0.5		−3.5	−0.5		−3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40			−40			−40				V_{DS} = 0 I_G = −1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	0.5		6.0	0.5		6.0	0.5		6.0	mA	V_{DS} = 20 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)			−250			−250			−250	pA	V_{DG} = 20 V, I_D = 200 μA	
6		V_{GS}	Gate-Source Voltage	−0.2		−3.0	−0.2		−3.0	−0.2		−3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4 000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8				600		1,200	600		1,200	600		1,200		V_{DG} = 20 V, I_D = 200 μA	
9		g_{os}	Common-Source Output Conductance			20			20			20		V_{DS} = 20 V, V_{GS} = 0	
10						5			5			5		V_{DS} = 20 V, I_D = 200 μA	
11		C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2				
13		$\bar{e}_N$	Equivalent Short-Circuit Input Noise Voltage		13	50		13	50		13	50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			25			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16		CMRR	Common-Mode Rejection Ratio (Note 4)	70	80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP