# monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

**Performance Curves NQT See Section 4**

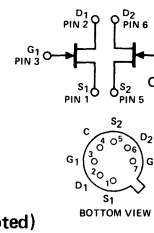
BENEFITS

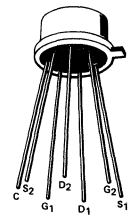
- High Input Impedance
  $I_G$ = 0.1 pA Maximum (U421-3)
- High Gain $g_{fs}$ = 140 μmho Minimum @ $I_D$ = 30 μA (U421-3)
- Low Power Supply Operation
  $V_{GS(off)}$ = 2 V Maximum (U421-3)
- Minimum System Error and Calibration
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

## ABSOLUTE MAXIMUM RATINGS (25°C)

| | |
|---|---|
| Gate-to-Gate Voltage | ±40 V |
| Gate-Drain or Gate-Source Voltage | −40 V |
| Gate Current | 10 mA |
| Device Dissipation (Each Side), $T_A$ = 25°C (Derate 3.2 mW/°C to 150°C) | 400 mW |
| Total Device Dissipation, $T_A$ = 25°C (Derate 6.0 mW/°C to 150°C) | 750 mW |
| Storage Temperature Range | −65 to +150°C |

TO-78
See Section 5




## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| | | Characteristic | | U421-3 Min | U421-3 Typ | U421-3 Max | U424-6 Min | U424-6 Typ | U424-6 Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | STATIC | $BV_{GSS}$ | Gate-Source Breakdown Voltage | −40 | −60 | | −40 | −60 | | V | $I_G$ = −1 μA, $V_{DS}$ = 0 | |
| 2 | STATIC | $BV_{G1G2}$ | Gate-Gate Breakdown Voltage | ±40 | | | ±40 | | | V | $I_G$ = −1 μA, $I_D$ = 0, $I_S$ = 0 | |
| 3 | STATIC | $I_{GSS}$ | Gate Reverse Current (Note 1) | | | 0.2 | | | 1.0 | pA | T = +25°C | $V_{GS}$ = −20 V, $V_{DS}$ = 0 |
| | | | | | | 0.5 | | | 1.0 | nA | T = +125°C | |
| 4 | STATIC | $I_G$ | Gate Operating Current (Note 1) | | | 0.1 | | | 0.5 | pA | T = +25°C | $V_{DG}$ = 10 V, $I_D$ = 30 μA |
| | | | | | | -100 | | | -500 | | T = +125°C | |
| 5 | STATIC | $V_{GS(off)}$ | Gate-Source Cutoff Voltage | −0.4 | | −2.0 | −0.4 | | −3.0 | V | $V_{DS}$ = 10 V, $I_D$ = 1 nA | |
| 6 | STATIC | $V_{GS}$ | Gate-Source Voltage | | | −1.8 | | | −2.9 | V | $V_{DG}$ = 10 V, $I_D$ = 30 μA | |
| 7 | STATIC | $I_{DSS}$ | Saturation Drain Current | 60 | | 1000 | 60 | | 1800 | μA | $V_{DS}$ = 10 V, $V_{GS}$ = 0 | |
| 8 | DYNAMIC | $g_{fs}$ | Common-Source Forward Transconductance | 300 | | 800 | 300 | | 1000 | μ℧ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 | f = 1 kHz |
| 9 | DYNAMIC | $g_{os}$ | Common-Source Output Conductance | | | 3.0 | | | 5.0 | μ℧ | | |
| 10 | DYNAMIC | $C_{iss}$ | Common-Source Input Capacitance | | | 3.0 | | | 3.0 | pF | | f = 1 MHz |
| 11 | DYNAMIC | $C_{rss}$ | Common-Source Reverse Transfer Capacitance | | | 1.5 | | | 1.5 | pF | | |
| 12 | DYNAMIC | $g_{fs}$ | Common-Source Forward Transconductance | 140 | | 250 | 135 | | 300 | μ℧ | $V_{DG}$ = 10 V, $I_D$ = 30 μA | f = 1 kHz |
| 13 | DYNAMIC | $g_{os}$ | Common-Source Output Conductance | | | 0.5 | | | 1.0 | μ℧ | | |
| 14 | DYNAMIC | $\bar{e}_n$ | Equivalent Short Circuit Input Noise Voltage | | 20 | 50 | | 20 | 70 | nV/√Hz | | f = 10 Hz |
| | | | | | 10 | | | 10 | 50 | nV/√Hz | | f = 1 kHz |
| 15 | DYNAMIC | NF | Noise Figure | | | 1.0 | | | 1.0 | dB | | f = 10 Hz, $R_G$ = 10M Ω |

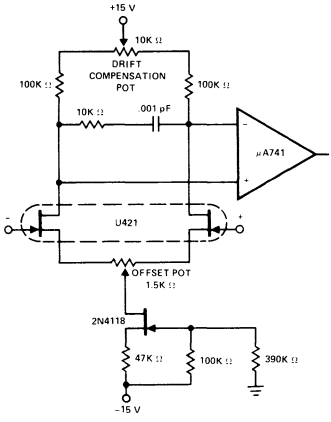
| | | Characteristic | | U421, 4 Min | U421, 4 Typ | U421, 4 Max | U422, 5 Min | U422, 5 Typ | U422, 5 Max | U423,6 Min | U423,6 Typ | U423,6 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 16 | MATCH | $\lvert V_{GS1} - V_{GS2}\rvert$ | Differential Gate-Source Voltage | | | 10 | | | 15 | | | 25 | mV | $V_{DG}$ = 10 V, $I_D$ = 30 μA |
| 17 | MATCH | $\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$ | Differential Gate-Source Voltage Change With Temperature (Note 2) | | | 10 | | | 25 | | | 40 | μV/°C | $V_{DG}$ = 10 V, $I_D$ = 30 μA, $T_A$ = −55°C, $T_B$ = 25°C, $T_C$ = 125°C |
| 18 | MATCH | CMRR | Common Mode Rejection Ratio (Note 3) | 90 | 95 | | 80 | 90 | | 80 | 90 | | dB | $I_D$ = 30 μA, $V_{DG}$ = 10 to 20 V |

NOTES.
1. Approximately doubles for every 10°C increase in $T_A$.
2. Measured at end points $T_A$, $T_B$ and $T_C$.
3. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$, $\Delta V_{DD}$ = 10 V.

NQT

## APPLICATIONS

### Very Low Leakage FET Input Op Amps




| | |
|---|---|
| $I_G$ | = 0.1 pA at $V_{cm}$ = 0 |
| Offset | = Can be nulled to 0 volts |
| Drift | = Can be nulled to 2 μV/°C |
| Slew Rate | = 0.5 V/μs |

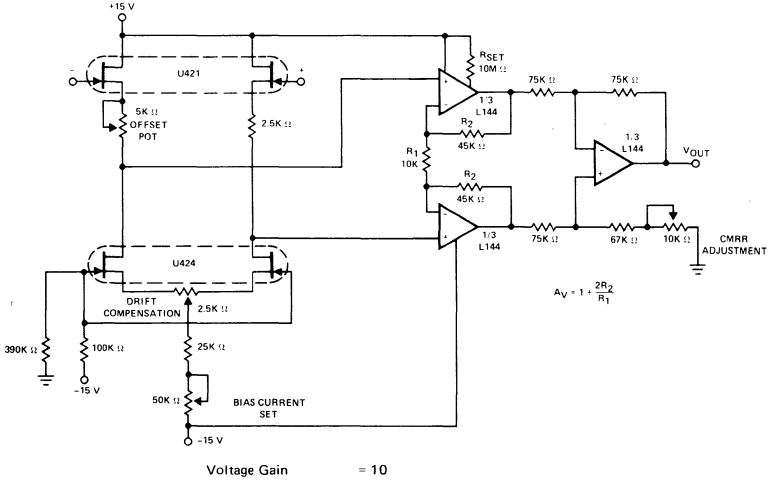
For more information see:

**DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)**

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

### Electrometer Amplifier

### L144CJ Instrumentation Amplifier




| | |
|---|---|
| Voltage Gain | = 10 |
| Input Current | = 0.1 pA |
| Compensated Drift | = 3 μV/°C |
| Nulled Offset | = 0 mV |
| CMRR | = 80 dB typical |
| Power Consumption | = Approx. 30 Volt x 120 μA = 3.6 mW |

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