

IG1NT052N10R (JANS G2N7697UFHC)

PD-98011B

Radiation Hardened GaN transistor
Surface Mount (PowIR-SMD)
100V, 52A, N-channel, Enhancement mode

Features

- Single event effect (SEE) hardened
up to LET (GAN)¹ = 70 MeV.cm²/mg (Au ion)
- Ultra low R_{DS(on)}
- Low total gate charge
- Zero reverse recovery charge
- Hermetically sealed ceramic package
- Surface mount
- Light weight
- ESD rating: Class 1C per MIL-STD-750, Method 1020

Potential Applications

- Isolated DC-DC converters
- Point-of-load (PoL) converters for FPGA, ASIC and DSP core rails
- Synchronous rectification
- Motor drives

Product Validation

Validated based on MIL-PRF-19500 for space applications

Description

IG1NT052N10R is part of the IR HiRel family of products. IR HiRel radiation hardened GaN transistor technology provides high performance power devices for space applications. These devices have been characterized for both Total Ionizing Dose (TID) and Single Event Effects (SEE). The combination of low R_{DS(on)}, low gate charge and zero reverse recovery charge reduces the power losses in switching applications such as DC-DC converters and motor control. These devices enable high-frequency operation of power management circuits resulting in high-power density and low payload mass.

Ordering Information

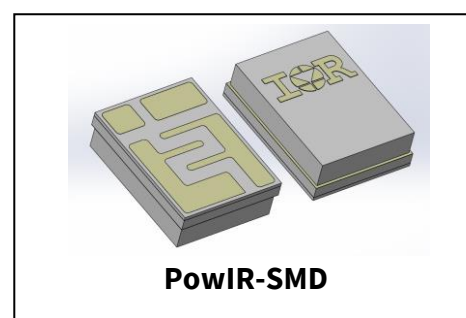
Table 1 **Ordering options**

Part number	Package	Screening Level	TID Level
IG1NT052N10R	PowIR-SMD	COTS	100 krad(Si)
IG1NT052N10G	PowIR-SMD	COTS	500 krad(Si)
JANS G2N7697UFHC	PowIR-SMD	JANS	500 krad(Si)

¹ LET Si equivalent = 86.5 MeV.cm²/mg

Product Summary

- V_{DS max}: 100V
- I_D: 52A
- R_{DS(on) max}: 6.0mΩ
- Q_{G max}: 13nC
- **Size**: 7.1mm x 5.3mm
- **REF**: MIL-PRF-19500 / 794



IG1NT052N10R (JANSG2N7697UFHC)

Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	100	V
$V_{DS (transient)}$	Drain-to-Source Voltage - transient ¹	120	V
$I_{D1} @ V_{GS} = 5V, T_C = 25^{\circ}C$	Continuous Drain Current	52	A
$I_{D2} @ V_{GS} = 5V, T_C = 100^{\circ}C$	Continuous Drain Current	33	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ²	208	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	30	W
	Linear Derating Factor	0.24	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage (Repetitive transients) ¹	± 5.5	V
	Gate-to-Source Voltage	± 5.0	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Package Mounting Surface Temperature	300 (for 5s)	
	Weight	0.23	g

¹ For $\leq 1\mu s$ ² Repetitive Rating; Pulse width limited by maximum junction temperature.

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$V_{DS\text{ max}}$	Drain-to-Source Voltage, continuous	—	—	100	V	$V_{GS} = 0\text{V}$, $I_D = 0\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	4.0	6.0	m Ω	$V_{GS} = 5\text{V}$, $I_D = 33\text{A}$ ¹
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.5	2.0	V	$V_{DS} = V_{GS}$, $I_D = 8.0\text{mA}$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.0	—	mV/ $^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current	—	0.1	10	μA	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$
		—	10	100		$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	0.03	0.5	mA	$V_{GS} = 5.0\text{V}$, $T_J = 25^\circ\text{C}$
		—	0.5	1		$V_{GS} = 5.0\text{V}$, $T_J = 125^\circ\text{C}$
	Gate-to-Source Leakage Reverse	—	0.2	1	μA	$V_{GS} = -5.0\text{V}$, $T_J = 25^\circ\text{C}$
		—	2.5	10		$V_{GS} = -5.0\text{V}$, $T_J = 125^\circ\text{C}$
R_G	Gate Resistance	—	1.5	—	Ω	$f = 1.0\text{MHz}$, open drain
Q_G	Total Gate Charge	—	8.8	13	nC	$I_D = 33\text{A}$ $V_{DS} = 50\text{V}$ $V_{GS} = 5.0\text{V}$
Q_{GS}	Gate-to-Source Charge	—	3.1	—		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	1.1	—		
Q_{OSS}	Output Charge	—	44	—	nC	$V_{DD} = 50\text{V}$, $V_{GS} = 0\text{V}$
C_{iss}	Input Capacitance	—	820	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 50\text{V}$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	510	—		
C_{rss}	Reverse Transfer Capacitance	—	7.7	—		

¹ Pulse width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Reverse Operation - Ratings and Characteristics (Pre-Irradiation)

Table 4 Reverse Operation Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current	—	—	52	A	$T_J = 25^\circ\text{C}$
I_{SM}	Pulsed Source Current ¹	—	—	208	A	$T_J = 25^\circ\text{C}$
V_{SD}	Forward Voltage	—	2.1	3.9	V	$T_J = 25^\circ\text{C}$, $I_S = 33\text{A}$, $V_{GS} = 0\text{V}$ ²
Q_{rr}	Reverse Recovery Charge	—	0	—	nC	$T_J = 25^\circ\text{C}$, $I_S = 33\text{A}$, $V_{DD} = 50\text{V}$ $di_S/dt = 100\text{A}/\mu\text{s}$

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	1.9	4.0	$^\circ\text{C}/\text{W}$
$R_{\theta J-PCB}$	Junction-to-Case-with Heat Sink	—	20	25	
$R_{\theta JA}$	Junction-to-Ambient - Devices on PCB (in free air)	—	45	70	

2.4 Radiation Characteristics

IR HiRel Radiation Hardened GaN transistors are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4.) Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics - Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	Up to 500 krad (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
$V_{DS\max}$	Drain-to-Source Breakdown Voltage	100	—	V	$V_{GS} = 0\text{V}$, $I_D = 0\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	V	$V_{DS} = V_{GS}$, $I_D = 8.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	0.5	mA	$V_{GS} = 5\text{V}$
	Gate-to-Source Leakage Reverse	—	1.0	μA	$V_{GS} = -5\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	10	μA	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (Package PowIR-SMD) ²	—	6.0	m Ω	$V_{GS} = 5\text{V}$, $I_D = 33\text{A}$
V_{SD}	Source-Drain Forward Voltage	—	3.9	V	$V_{GS} = 0\text{V}$, $I_S = 33\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature² Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$ ³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 5\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 80\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.⁵ Part numbers IG1NT052N10R (100 krad(Si)) and IG1NT052N10G (JANS G2N7697UFHC) 500 krad(Si)

IG1NT052N10R (JANS G2N7697UFHC)

Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

Device Characteristics

2.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened GaN transistors have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Figure 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

Ion	LET (GaN) ¹ (MeV.cm ² /mg)	Energy (GaN) (MeV)	Range (GaN) (μm)	V _{DS} (V)	
				V _{GS} = 0V	V _{GS} = -5V
Au	70 ± 5%	1713 ± 5%	48 ± 5%	100	100

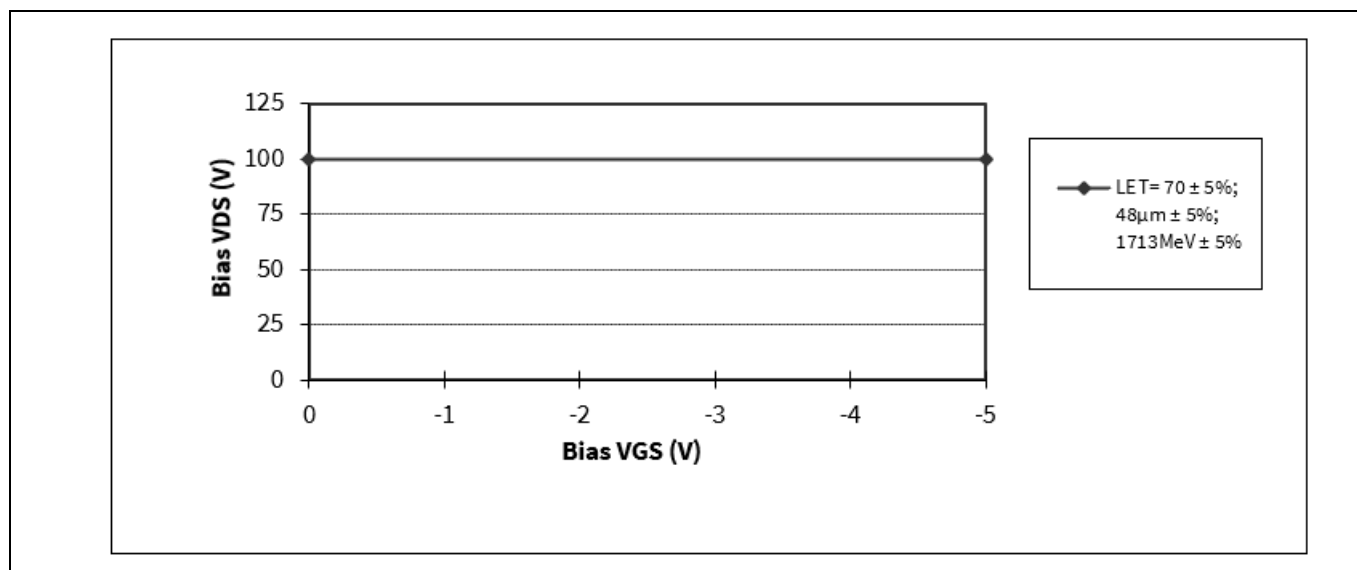


Figure 1 Typical Single Event Effect, Safe Operating Area

¹ LET Si equivalent = 86.5 MeV.cm²/mg

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Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

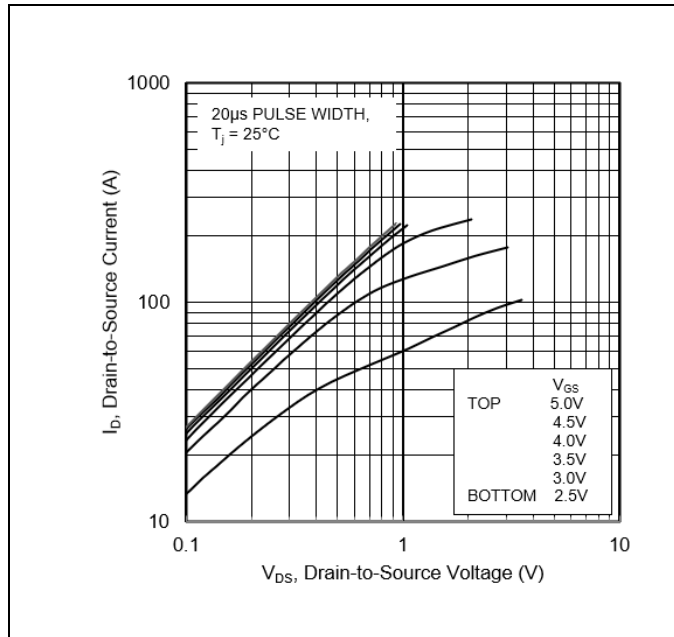


Figure 2 Typical Output Characteristics

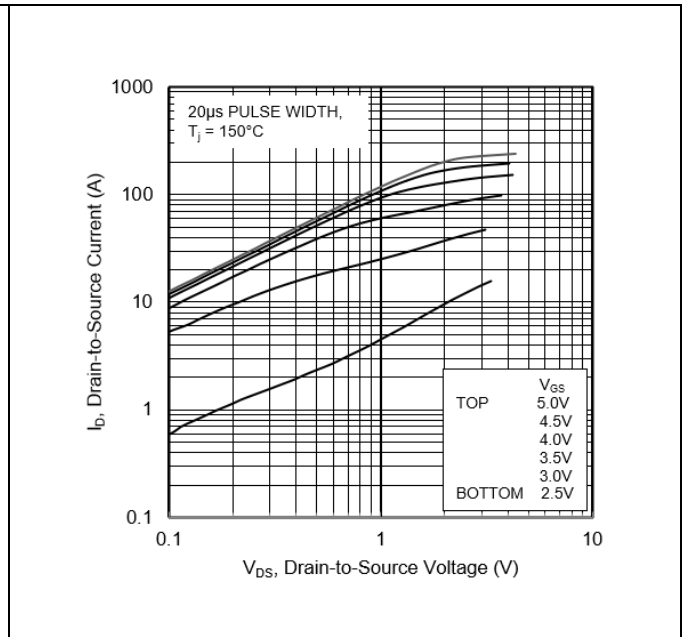


Figure 3 Typical Output Characteristics

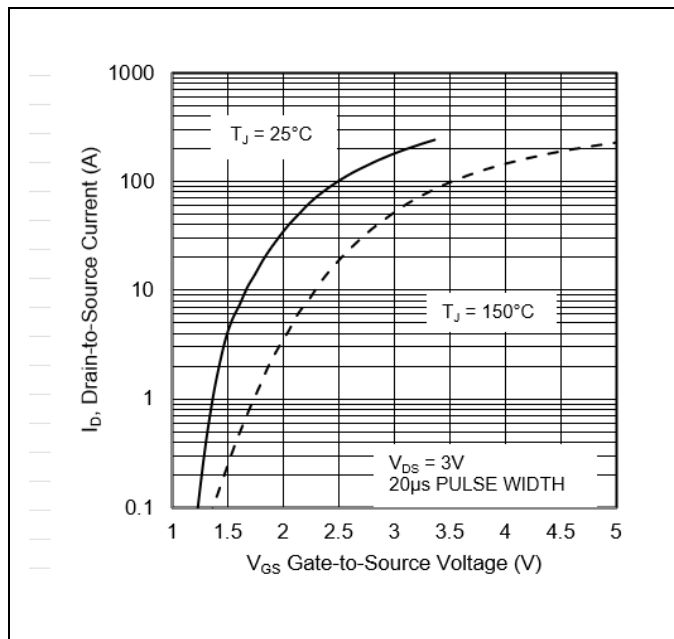


Figure 4 Typical Transfer Characteristics

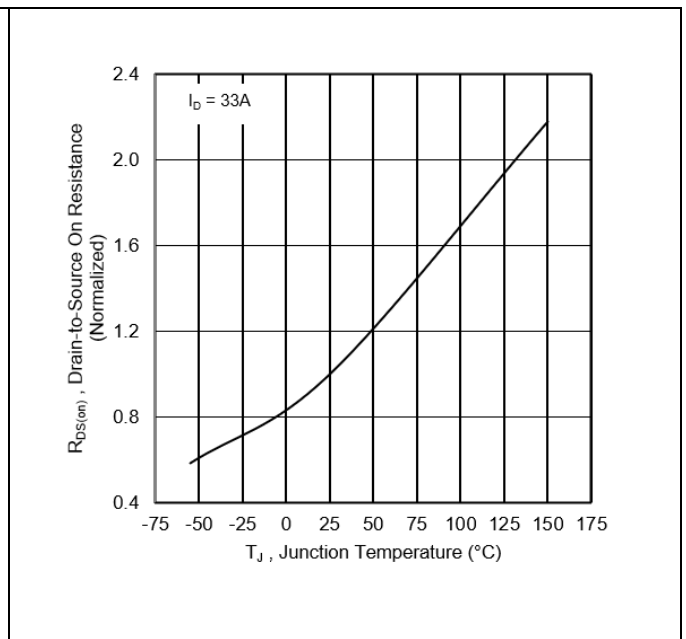


Figure 5 Normalized On-Resistance Vs. Temperature

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Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

Electrical Characteristics Curves (Pre-irradiation)

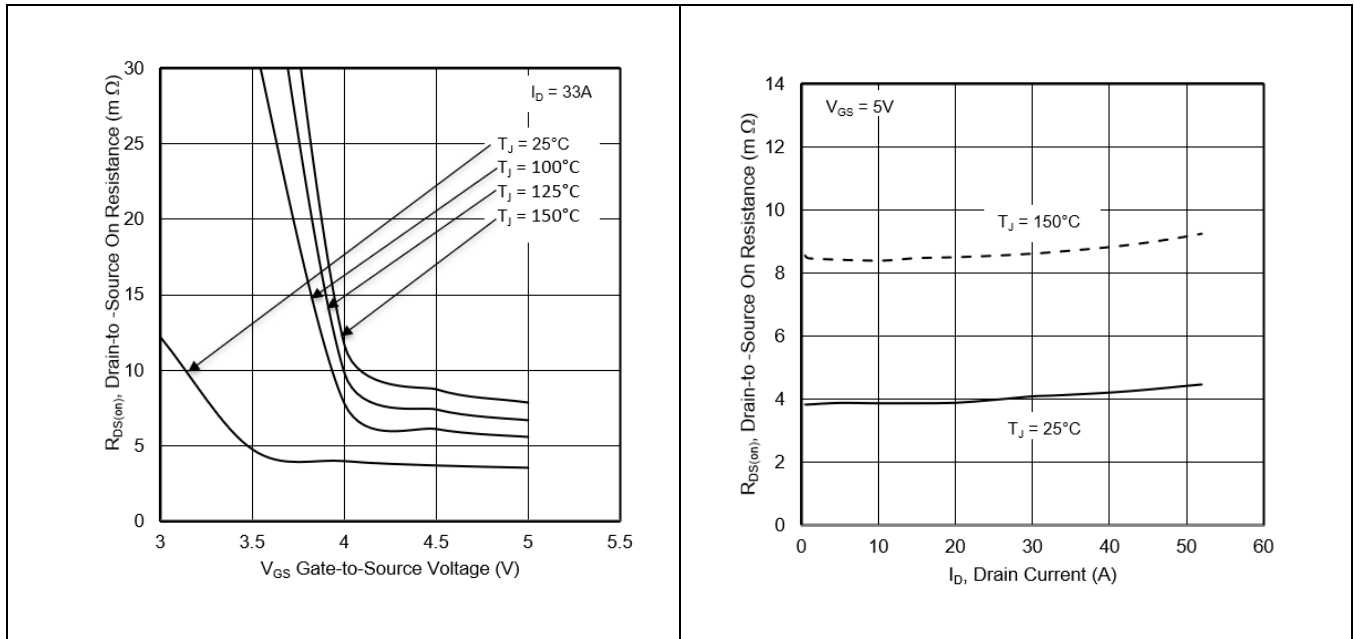


Figure 6 Typical On-Resistance Vs. Gate Voltage

Figure 7 Typical On-Resistance Vs. Drain Current

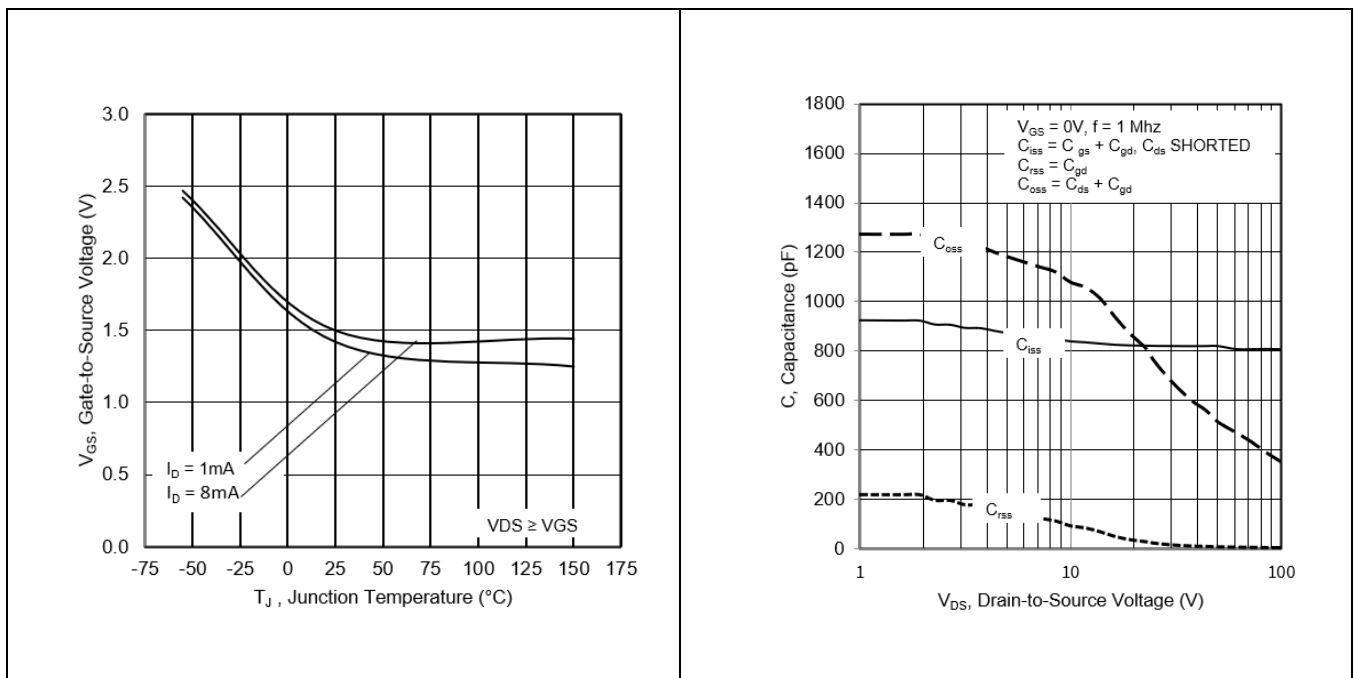


Figure 8 Typical Threshold Voltage Vs. Temperature

Figure 9 Typical Capacitance Vs. Drain-to-Source Voltage

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Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

Electrical Characteristics Curves (Pre-irradiation)

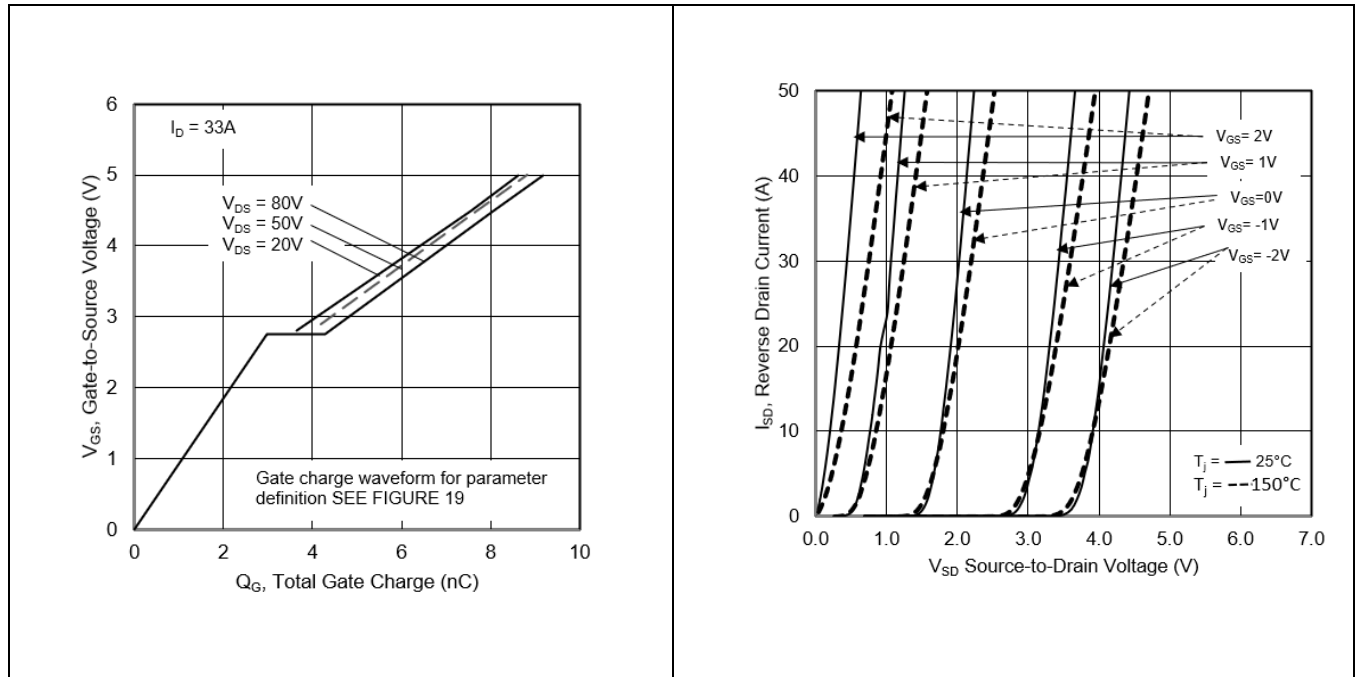


Figure 10 Typical Gate Charge Vs. Gate-to-Source Voltage

Figure 11 Typical Source-Drain Current Vs. Source-Drain Voltage (reverse output characteristics)

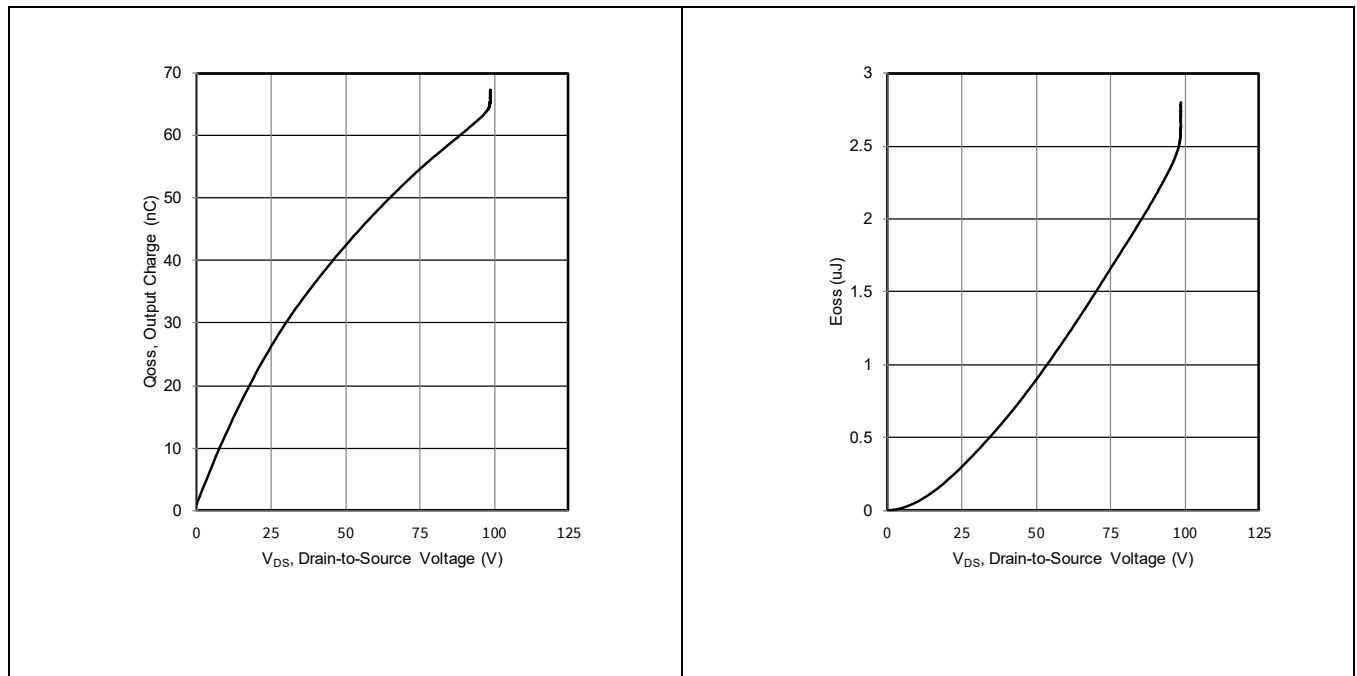


Figure 12 Typical Output Charge

Figure 13 Typical Output Energy

IG1NT052N10R (JANS G2N7697UFHC)

Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

Electrical Characteristics Curves (Pre-irradiation)

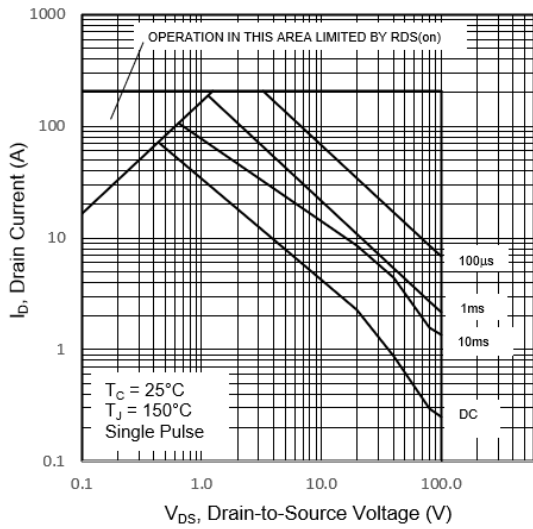


Figure 14 Maximum Safe Operating Area

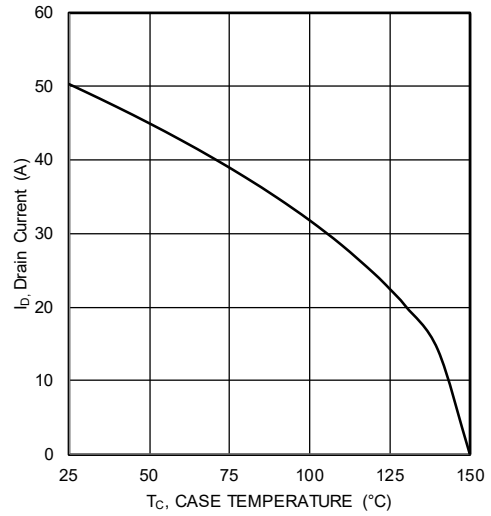


Figure 15 Maximum Drain Current Vs. Case Temperature

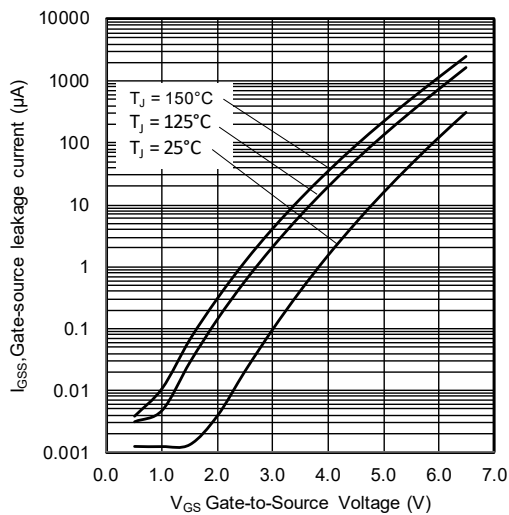


Figure 16 Typical Gate-Source Leakage Current Vs. Gate-Source Voltage (Positive voltage)

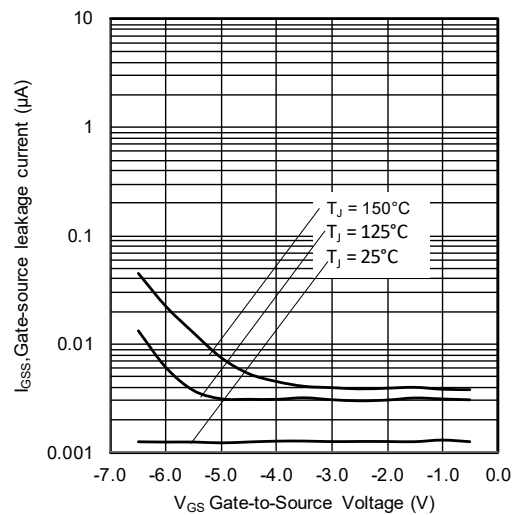


Figure 17 Typical Gate-Source Leakage Current Vs. Gate-Source Voltage (Negative Voltage)

IG1NT052N10R (JANS62N7697UFHC)

Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

Electrical Characteristics Curves (Pre-irradiation)

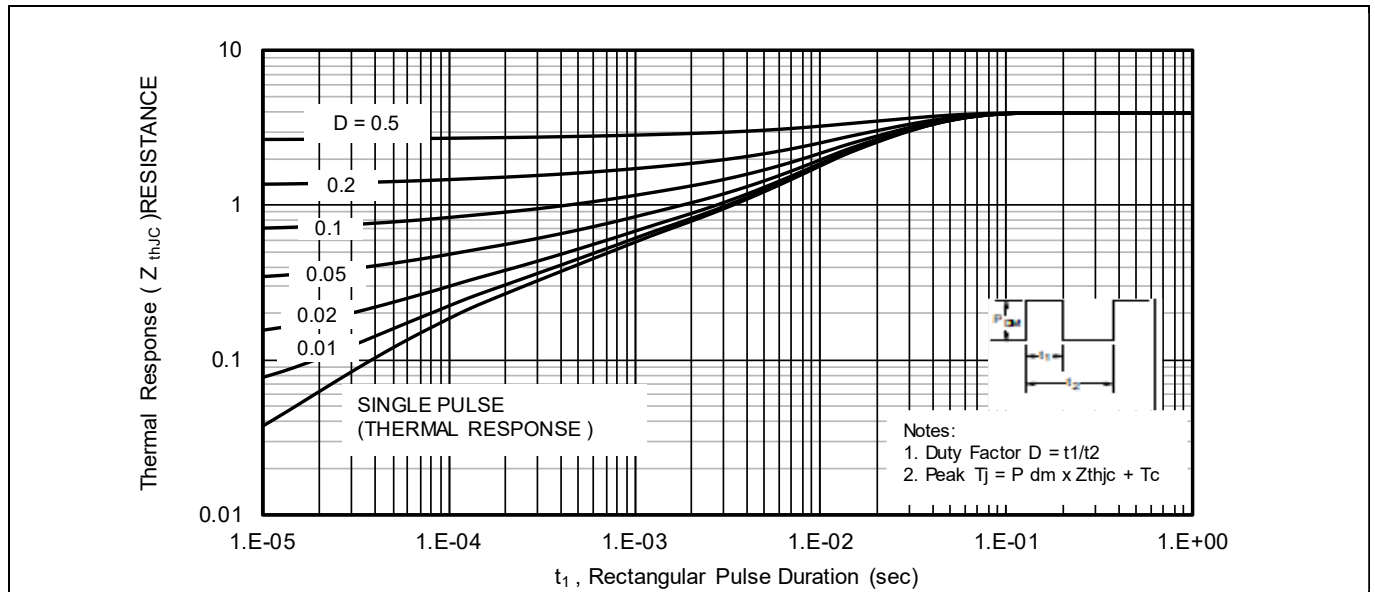


Figure 18 Maximum Effective Transient Thermal Impedance, Junction-to-Case

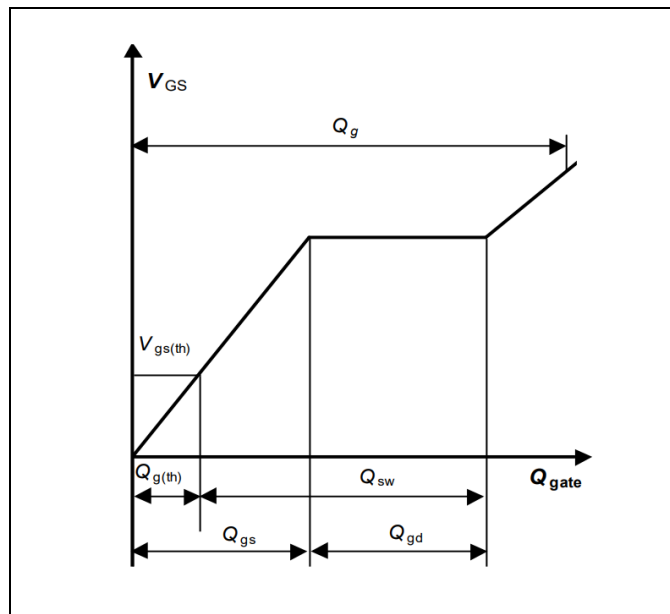


Figure 19 Gate Charge Waveform

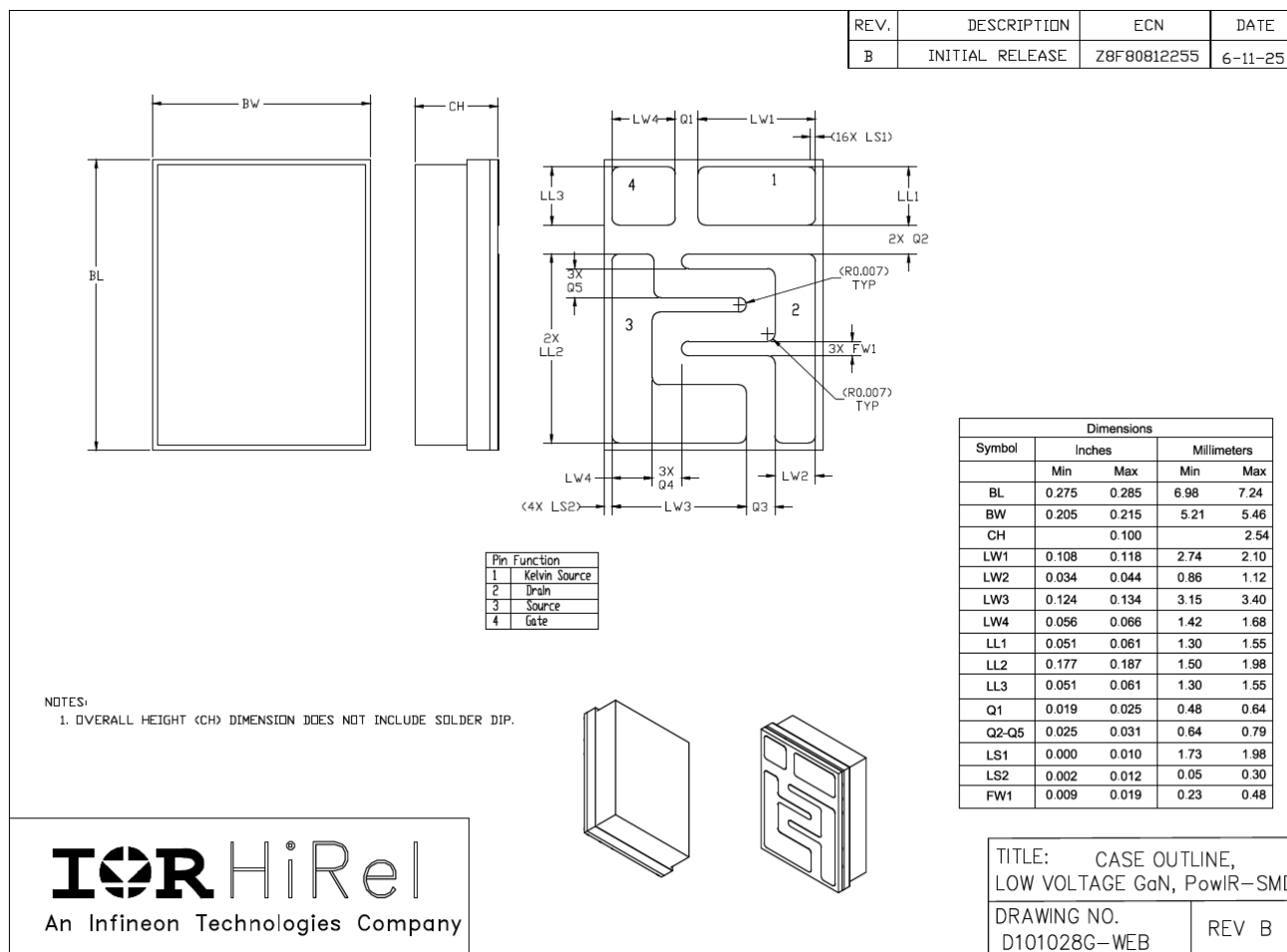
IG1NT052N10R (JANS G2N7697UFHC)

Radiation Hardened GaN transistor Surface Mount (PowIR-SMD)

Package Outline

4 Package Outline

Note: For the most updated package outline, please see the website: [PowIR-SMD](#)



Pin Description:

Pin 1: Kelvin Source: This pin can be used for the gate return. It is optimized to help the gate drive loop. **Pin 1 and Pin 3** are at the same potential.

Pin 2: Drain: This pin is optimized as a power pin to conduct current between drain and source.

Pin 3: Source: This pin is optimized as a power pin to conduct current between drain and source, it is at the same potential as **Pin 1**.

Pin 4: Gate: The control pin for the device.

Revision history**Revision history**

Document version	Date of release	Description of changes
	02/22/2024	Preliminary datasheet with PPD number (PPD-98011)
Rev A	05/30/2025	Final datasheet with PD number
Rev B	07/30/2025	Updated based on ECN-Z8F80816562

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