JANSR2N7294

Formerly FRF250R4

June 1998

23A, 200V, 0.115 Ohm, Rad Hard, N-Channel Power MOSFET

Features

- **23A, 200V, $r_{DS(ON)}$ = 0.115Ω**
- **Total Dose**
  - **Meets Pre-RAD Specifications to 100K RAD (Si)**
- **Dose Rate**
  - **Typically Survives 3E9 RAD (Si)/s at 80% BV_{DSS}**
  - **Typically Survives 2E12 if Current Limited to I_{DM}**
- **Photo Current**
  - **12nA Per-RAD(Si)/s Typically**
- **Neutron**
  - **Maintain Pre-RAD Specifications for 1E13 Neutrons/cm^2**
  - **Usable to 1E14 Neutrons/cm^2**

Ordering Information

PART NUMBER	PACKAGE	BRAND
JANSR2N7294	TO-254AA	JANSR2N7294

Die family TA17652.

MIL-PRF-19500/605.

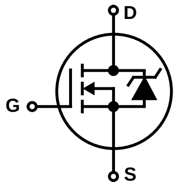
Description

The Intersil Corporation has designed a series of SECOND GENERATION hardened power MOSFETs of both N-Channel and P-Channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD (Si) and 1000K RAD (Si) with neutron hardness ranging from 1E13 for 500V product to 1E14 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^o) exposures. Design and processing efforts are also directed to enhance survival to dose rate (GAMMA DOT) exposure.

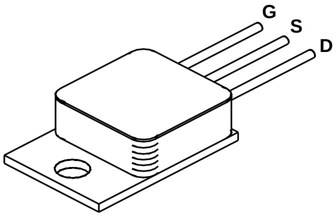
Also available at other radiation and screening levels. See us on the web, Intersil' home page: http://www.intersil.com. Contact your local Intersil Sales Office for additional information.

Symbol



Package

TO-254AA



CAUTION: Beryllia Warning per MIL-S-19500
refer to package specifications.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		JANSR2N7294	UNITS
Drain to Source Voltage	V_{DS}	200	V
Drain to Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200	V
Continuous Drain Current			
$T_C = 25^oC$	I_D	23	A
$T_C = 100^oC$	I_D	15	A
Pulsed Drain Current	I_{DM}	69	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
$T_C = 25^oC$	P_T	125	W
$T_C = 100^oC$	P_T	50	W
Linear Derating Factor		1.00	$W/^oC$
Single Pulsed Avalanche Current, L = 100μH, (See Test Figure)	I_{AS}	69	A
Continuous Source Current (Body Diode)	I_S	23	A
Pulsed Source Current (Body Diode)	I_{SM}	69	A
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Lead Temperature (During Soldering) (Distance >0.063in (1.6mm) from Case, 10s Max)	T_L	300	^oC
Weight (Typical)		9.3	g

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V		200	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA	$T_C = -55^oC$	-	-	5.0	V
			$T_C = 25^oC$	2.0	-	4.0	V
			$T_C = 125^oC$	1.0	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160V, V_{GS} = 0V	$T_C = 25^oC$	-	-	25	μA
			$T_C = 125^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	$T_C = 25^oC$	-	-	100	nA
			$T_C = 125^oC$	-	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	V_{GS} = 10V, I_D = 23A		-	-	2.78	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 15A, V_{GS} = 10V	$T_C = 25^oC$	-	-	0.115	Ω
			$T_C = 125^oC$	-	-	0.253	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 23A, R_L = 4.35Ω, V_{GS} = 10V, R_{GS} = 25Ω		-	-	156	ns
Rise Time	t_r			-	-	510	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	574	ns
Fall Time	t_f			-	-	280	ns
Total Gate Charge (Not on slash sheet)	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 100V, I_D = 23A	-	-	558	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	-	298	nC
Threshold Gate Charge (Not on slash sheet)	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	-	20	nC
Gate Charge Source	Q_{gs}			-	-	66	nC
Gate Charge Drain	Q_{gd}			-	-	144	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	48	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 25A	0.6	-	1.8	V
Reverse Recovery Time	t_{rr}	I_{SD} = 25A, dI_{SD}/dt = 100A/μs	-	-	1700	ns

Electrical Specifications up to 100K RAD $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts	(Note 3)	BV_{DSS}	$V_{GS} = 0$, $I_D = 1mA$	200	-	V
Gate to Source Threshold Volts	(Note 3)	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 1mA$	2.0	4.0	V
Gate to Body Leakage	(Notes 2, 3)	I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	100	nA
Zero Gate Leakage	(Note 3)	I_{DSS}	$V_{GS} = 0$, $V_{DS} = 160V$	-	25	μA
Drain to Source On-State Volts	(Notes 1, 3)	$V_{DS(ON)}$	$V_{GS} = 10V$, $I_D = 23A$	-	2.78	V
Drain to Source On Resistance	(Notes 1, 3)	$r_{DS(ON)}$	$V_{GS} = 10V$, $I_D = 15A$	-	0.115	Ω

NOTES:

1. Pulse test, 300μs Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both $V_{GS} = 10V$, $V_{DS} = 0V$ and $V_{GS} = 0V$, $V_{DS} = 80\%\ BV_{DSS}$.

Typical Performance Curves Unless Otherwise Specified

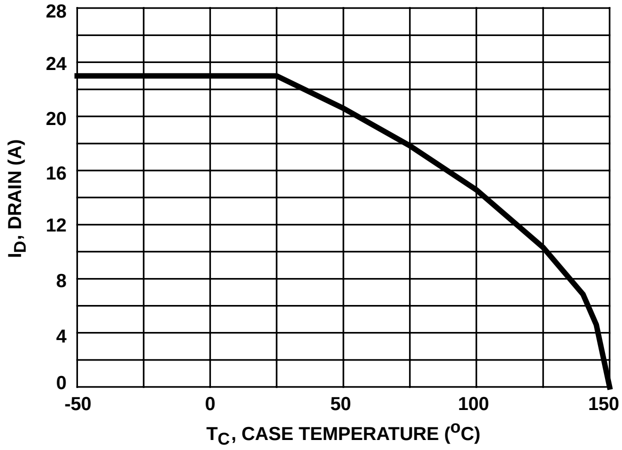


FIGURE 1. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

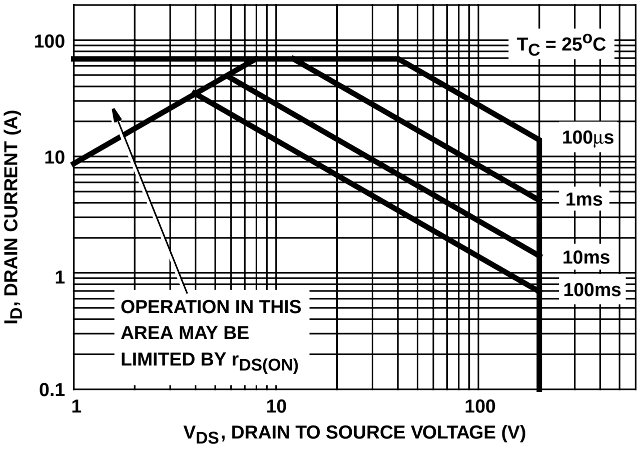


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

Typical Performance Curves Unless Otherwise Specified (Continued)

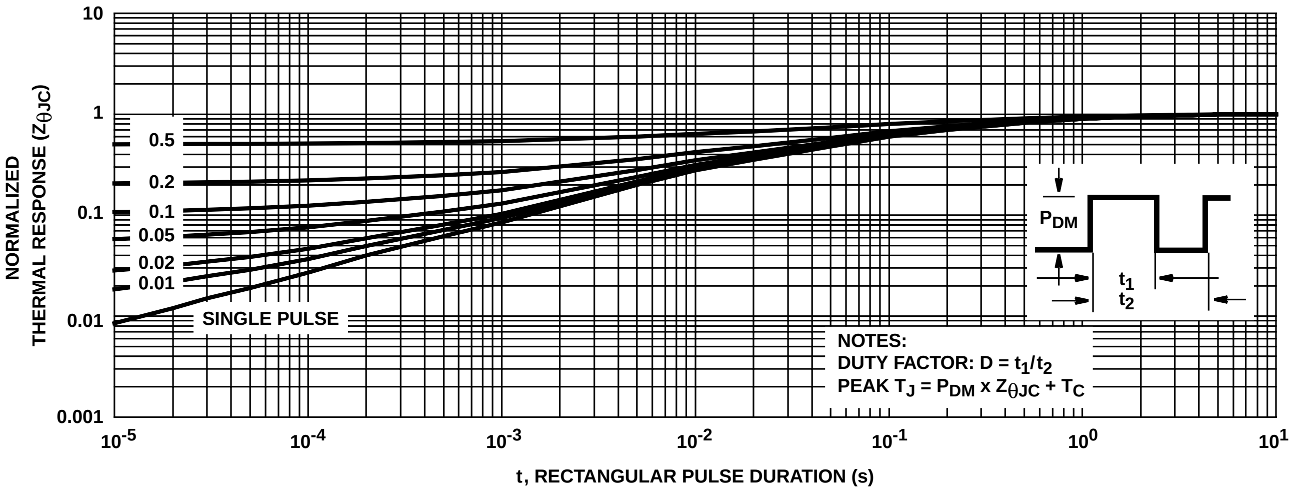


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

Test Circuits and Waveforms

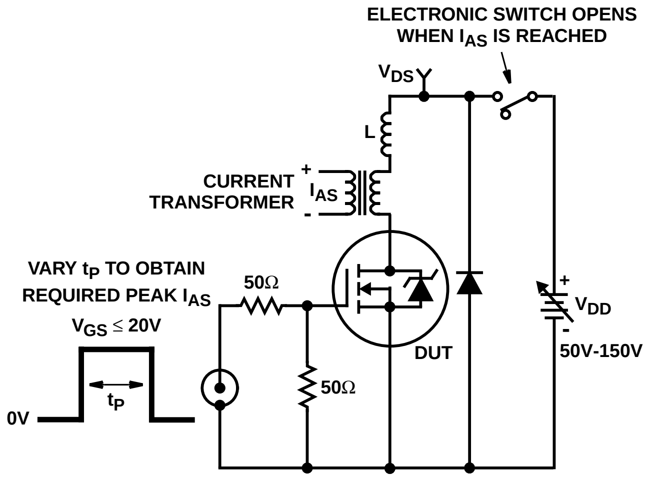


FIGURE 4. UNCLAMPED ENERGY TEST CIRCUIT

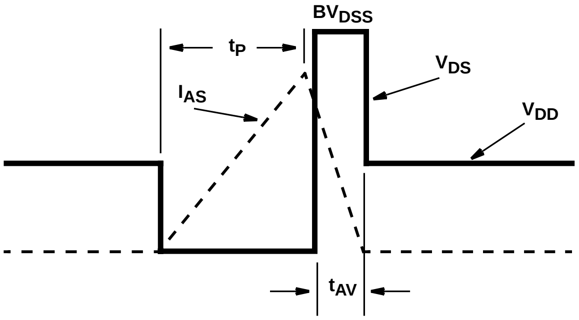


FIGURE 5. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms

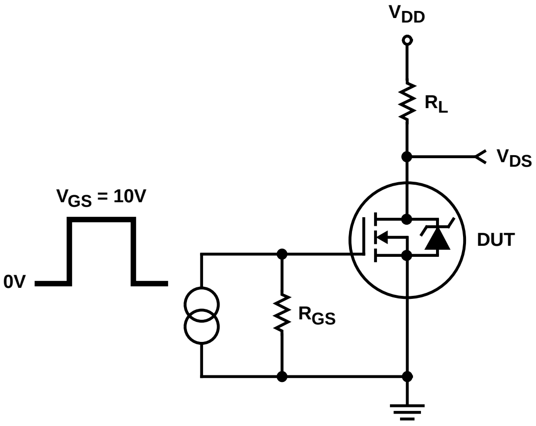


FIGURE 6. RESISTIVE SWITCHING TEST CIRCUIT

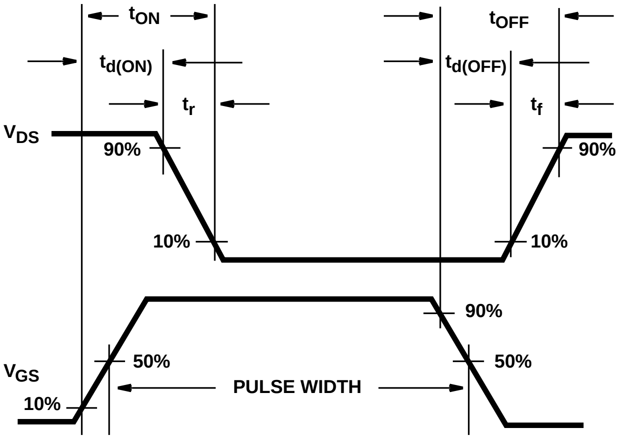


FIGURE 7. RESISTIVE SWITCHING WAVEFORMS

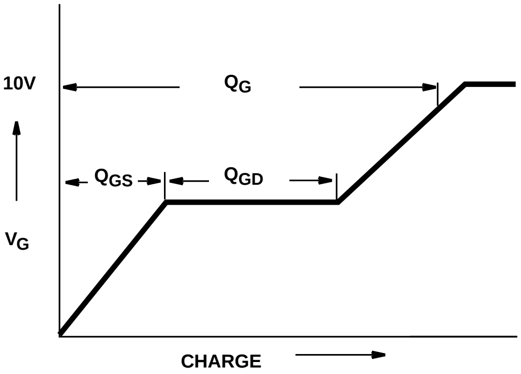


FIGURE 8. BASIC GATE CHARGE WAVEFORM

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table).

Delta Tests and Limits (JANS) T_C = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm20V$	±20 (Note 4)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value	±25 (Note 4)	µA
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 25^oC$ at Rated I_D	±20% (Note 5)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	I_D = 1.0mA	±20% (Note 5)	V

NOTES:

4. Or 100% of Initial Reading (whichever is greater).
5. Of Initial Reading.

Screening Information

TEST	JANS
Gate Stress	V_{GS} = 30V, t = 250µs
Pind	Required
Pre Burn-In Tests (Note 6)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, T_A = 150°C, Time = 48 hours
Interim Electrical Tests (Note 6)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, T_A = 150°C, Time = 240 hours
PDA	5%
Final Electrical Tests (Note 6)	MIL-S-19500, Group A, Subgroups 2 and 3

NOTE:

6. Test limits are identical pre and post burn-in.

Additional Screening Tests

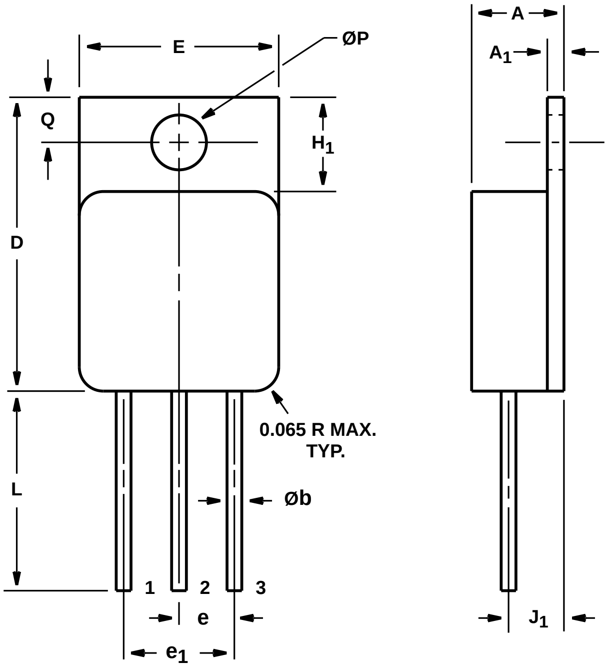
PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	V_{DS} = 160V, t = 10ms	1.6	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)}$ = 15V, L = 0.1mH	69	A
Thermal Response	ΔV_{SD}	t_H = 100ms; V_H = 25V; I_H = 4A	136	mV
Thermal Impedance	ΔV_{SD}	t_H = 500ms; V_H = 25V; I_H = 4A	187	mV

Rad Hard Data Packages - Intersil Power Transistors

1. **JANS Rad Hard - Standard Data Package**
   - A. Certificate of Compliance
   - B. Serialization Records
   - C. Assembly Flow Chart
   - D. SEM Photos and Report

TO-254AA

3 LEAD JEDEC TO-254AA HERMETIC METAL PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.249	0.260	6.33	6.60	-
A_1	0.040	0.050	1.02	1.27	-
Øb	0.035	0.045	0.89	1.14	2, 3
D	0.790	0.800	20.07	20.32	-
E	0.535	0.545	13.59	13.84	-
e	0.150 TYP		3.81 TYP		4
e_1	0.300 BSC		7.62 BSC		4
H_1	0.245	0.265	6.23	6.73	-
J_1	0.140	0.160	3.56	4.06	4
L	0.520	0.560	13.21	14.22	-
ØP	0.139	0.149	3.54	3.78	-
Q	0.110	0.130	2.80	3.30	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC outline TO-254AA dated 11-86.
2. Add typically 0.002 inches (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Die to base BeO isolated, terminals to case ceramic isolated.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

WARNING!

BERYLLIA WARNING PER MIL-S-19500

Packages containing beryllium oxide (BeO) shall not be ground, machined, sandblasted, or subject to any mechanical operation which will produce dust containing any beryllium compound. Packages containing any beryllium compound shall not be subjected to any chemical process (etching, etc.) which will produce fumes containing beryllium or its' compounds.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

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