

RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
SURFACE MOUNT (UB)
60V, P-CHANNEL
REF: MIL-PRF-19500/745
R₇ TECHNOLOGY
Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number
IRHLUB7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UB
IRHLUB7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UB

Refer to Page 10 for 3 Additional Part Numbers -
 IRHLUBN7970Z4, IRHLUBC7970Z4, IRHLUBCN7970Z4


Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Surface Mount
- Light Weight
- Complementary N-Channel Available-
 IRHLUB770Z4, IRHLUBN770Z4
 IRHLUBC770Z4, IRHLUBCN770Z4

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = -4.5V, T _C = 25°C	Continuous Drain Current	-0.53	A
I _{D2} @ V _{GS} = -4.5V, T _C = 100°C	Continuous Drain Current	-0.33	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	-2.12	
P _D @ T _C = 25°C	Maximum Power Dissipation	0.57	W
	Linear Derating Factor	0.0045	W/°C
V _{GS}	Gate-to-Source Voltage	± 10	V
E _{AS}	Single Pulse Avalanche Energy ②	33.5	mJ
I _{AR}	Avalanche Current ①	-0.53	A
E _{AR}	Repetitive Avalanche Energy ①	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-4.4	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	43 (Typical)	

Pre-Irradiation

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.055	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.40	Ω	V _{GS} = -4.5V, I _{D2} = -0.33A ④
V _{GS(th)}	Gate Threshold Voltage	-1.0	—	-2.0	V	V _{DS} = V _{GS} , I _D = -250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	3.1	—	mV/°C	
G _{fs}	Forward Transconductance	0.8	—	—	S	V _{DS} = -10V, I _{D2} = -0.33A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
		—	—	-10		V _{DS} = -48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -10V
	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 10V
Q _G	Total Gate Charge	—	—	3.6	nC	I _{D1} = -0.53A
Q _{GS}	Gate-to-Source Charge	—	—	1.5		V _{DS} = -30V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	1.8		V _{GS} = -4.5V
t _{d(on)}	Turn-On Delay Time	—	—	22	ns	V _{DD} = -30V
Tr	Rise Time	—	—	22		I _{D1} = -0.53A
t _{d(off)}	Turn-Off Delay Time	—	—	27		R _G = 24Ω
t _f	Fall Time	—	—	27		V _{GS} = -5.0V
L _S + L _D	Total Inductance	—	8.4	—	nH	Measured from center of Drain pad to center of source pad
C _{iSS}	Input Capacitance	—	167	—	pF	V _{GS} = 0V
C _{oSS}	Output Capacitance	—	43	—		V _{DS} = -25V
C _{rSS}	Reverse Transfer Capacitance	—	10	—		f = 100KHz
R _G	Gate Resistance	—	56	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.53	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-2.12		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _J = 25°C, I _S = -0.53A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	50	ns	T _J = 25°C, I _F = -0.53A, V _{DD} ≤ 25V, di/dt = -100A/μs ④
Q _{rr}	Reverse Recovery Charge	—	—	25	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJA}	Junction-to-Ambient	—	—	220	°C/W
R _{θJL}	Junction-to-Lead	—	—	40	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = -25V, starting T_J = 25°C, L = 238mH, Peak I_L = -0.53A, V_{GS} = -10V
- ③ I_{SD} ≤ -0.53A, di/dt ≤ -100A/μs, V_{DD} ≤ -60V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V_{GS} Bias. -10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. -48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si) ¹		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V _{GS} = 0V, I _D = -250μA
V _{GS(th)}	Gate Threshold Voltage	-1.0	-2.0	V	V _{DS} = V _{GS} , I _D = -250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100	nA	V _{GS} = 10V
I _{DSS}	Zero Gate Voltage Drain Current	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (TO-39)	—	1.36	Ω	V _{GS} = -4.5V, I _{D2} = -0.33A
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (UB)	—	1.40	Ω	V _{GS} = -4.5V, I _{D2} = -0.33A
V _{SD}	Diode Forward Voltage	—	-5.0	V	V _{GS} = 0V, I _S = -0.53A

1. Part numbers IRHLUB7970Z4, IRHLUB7930Z4 and additional part numbers listed on page 10

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@ VGS = 0V	@ VGS = 2V	@ VGS = 4V	@ VGS = 5V	@ VGS = 6V	@ VGS = 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-50
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	—
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	—	—

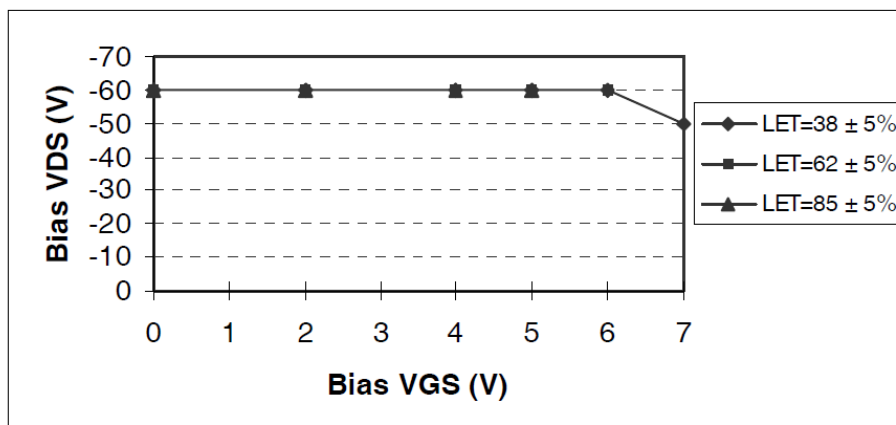


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

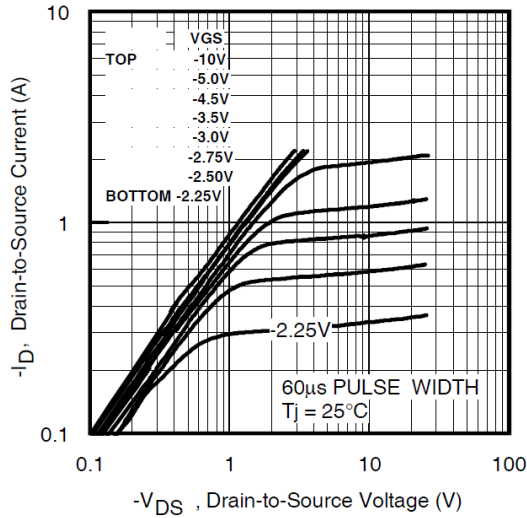


Fig 1. Typical Output Characteristics

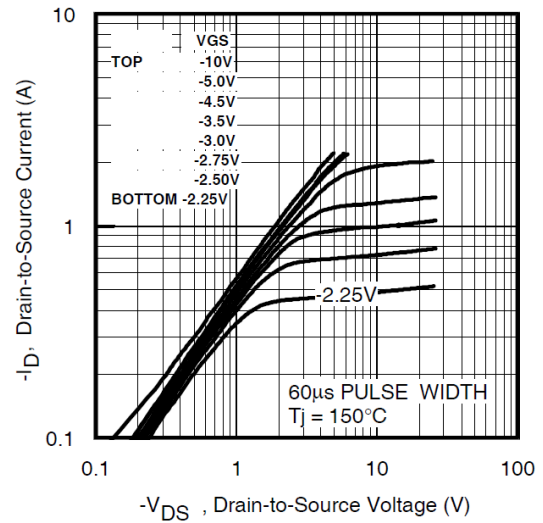


Fig 2. Typical Output Characteristics

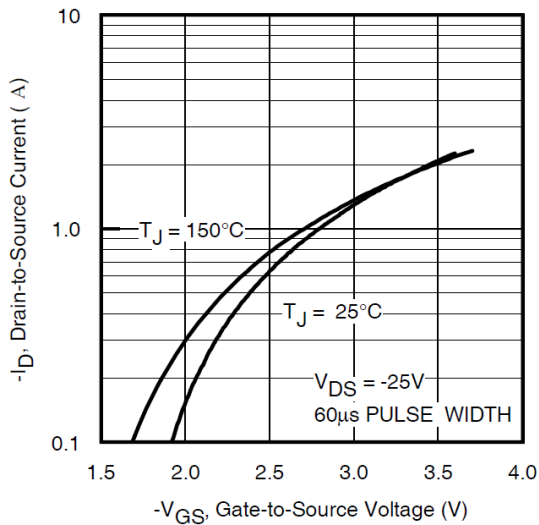


Fig 3. Typical Transfer Characteristics

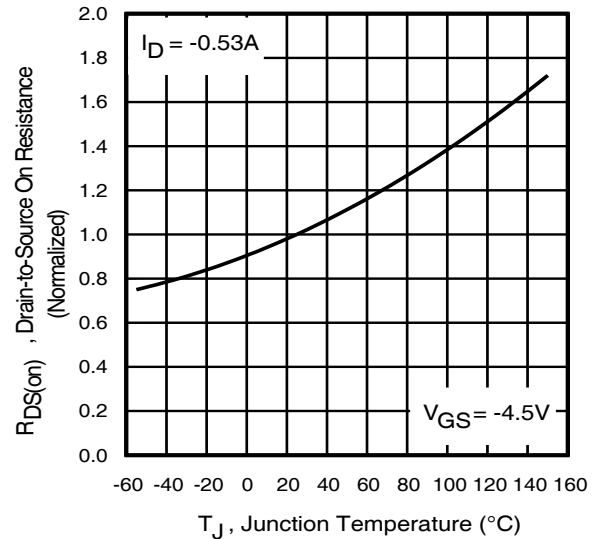


Fig 4. Normalized On-Resistance Vs. Temperature

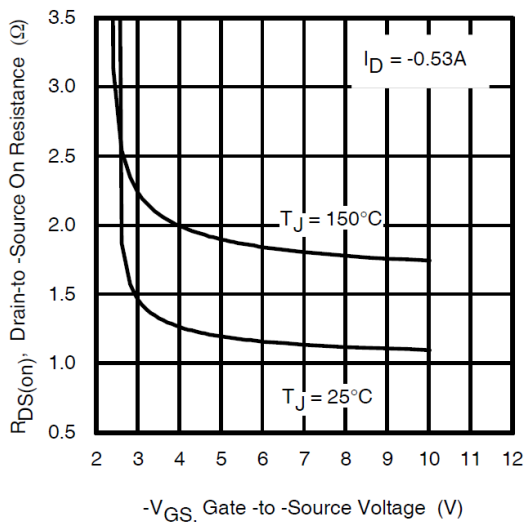


Fig 5. Typical On-Resistance Vs Gate Voltage

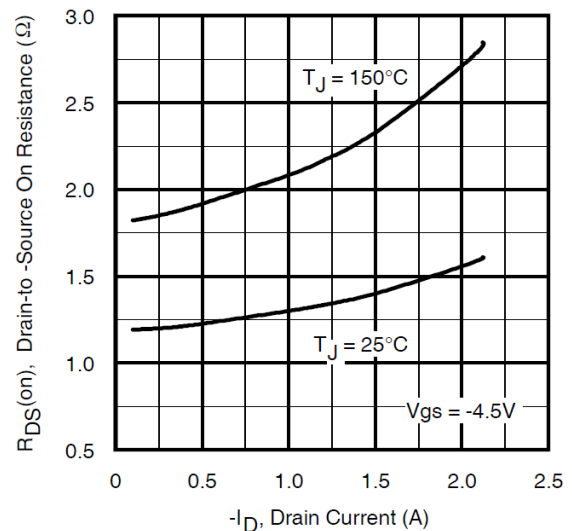


Fig 6. Typical On-Resistance Vs Drain Current

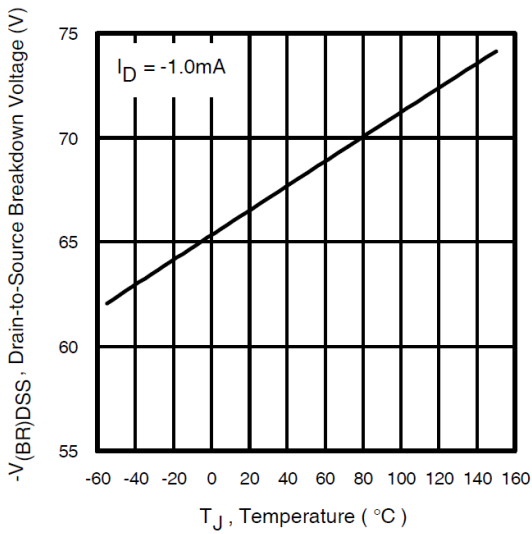


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

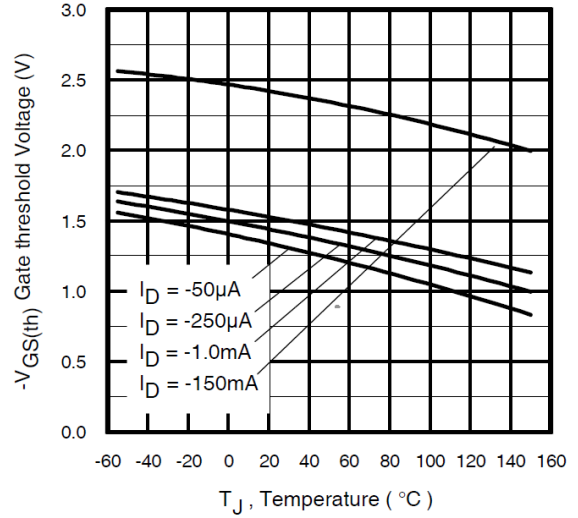


Fig 8. Typical Threshold Voltage Vs Temperature

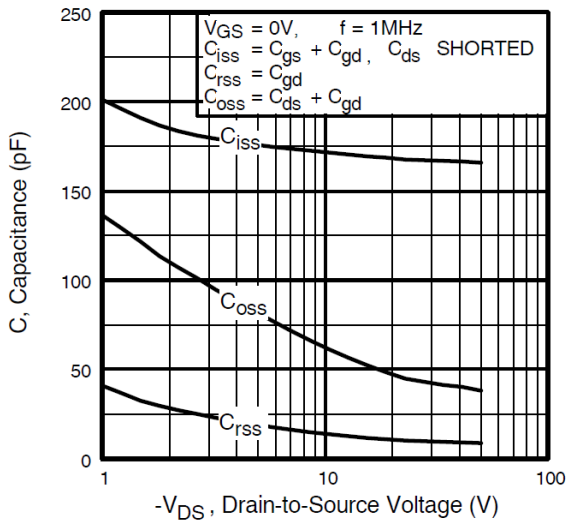


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

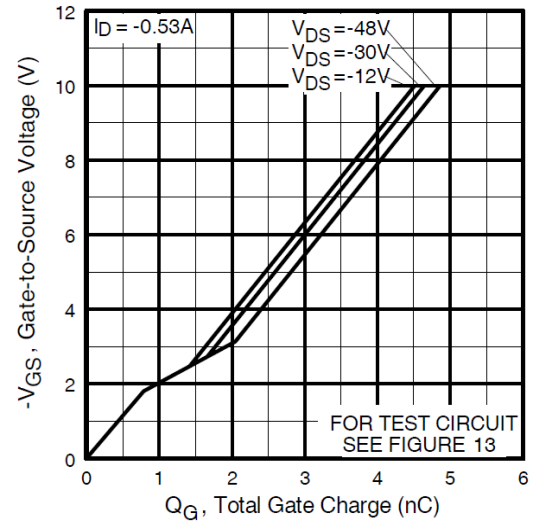


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

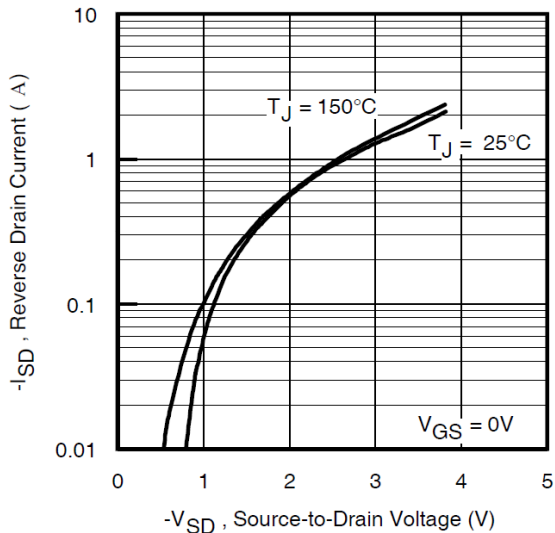


Fig 11. Typical Source-Drain Diode Forward Voltage

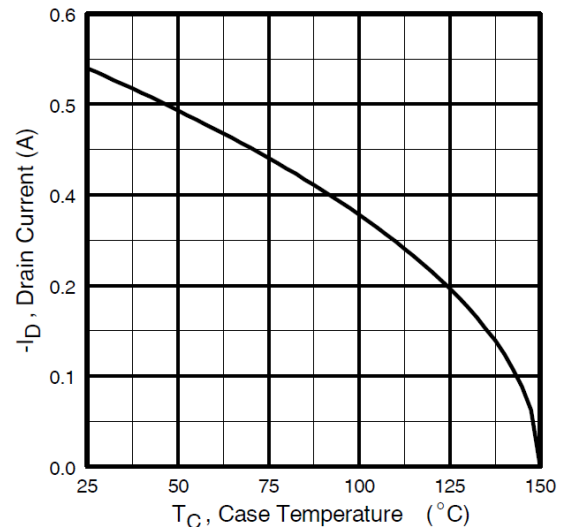


Fig 12. Maximum Drain Current Vs. Case Temperature

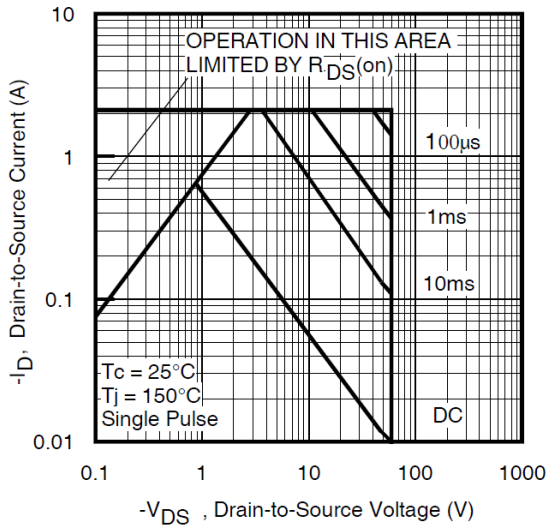


Fig 13. Maximum Safe Operating Area

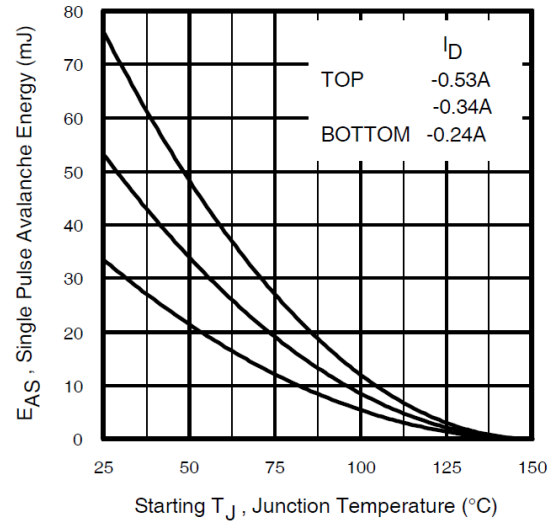


Fig 14. Maximum Avalanche Energy Vs. Drain Current

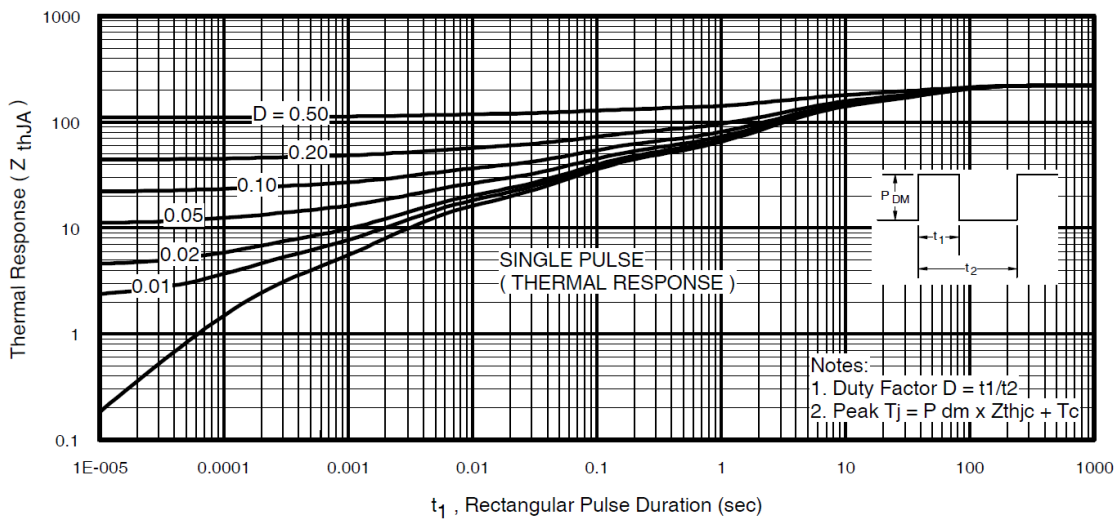


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

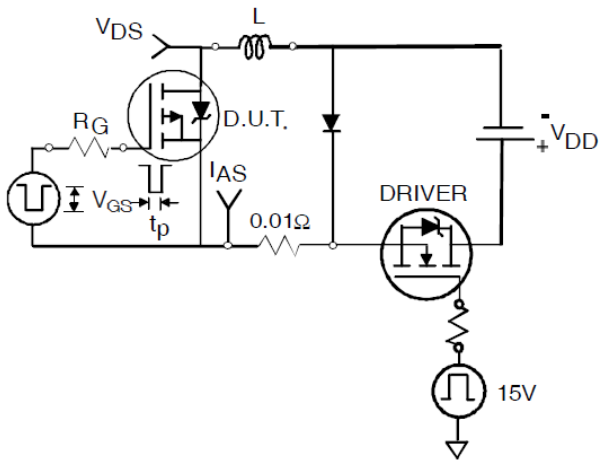


Fig 16a. Unclamped Inductive Test Circuit

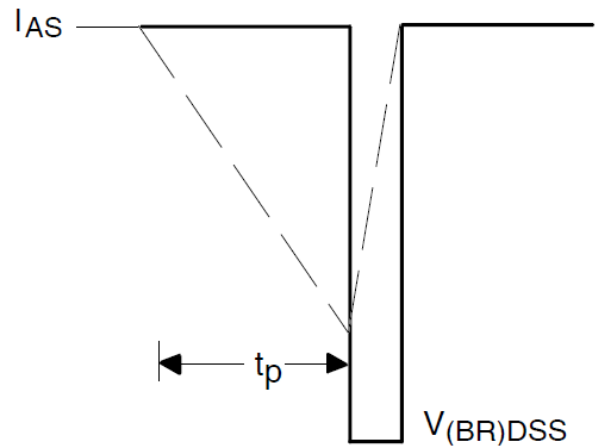


Fig 16b. Unclamped Inductive Waveforms

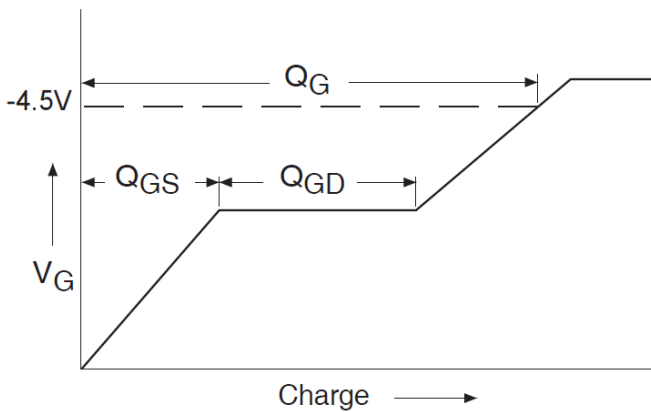


Fig 17a. Gate Charge Waveform

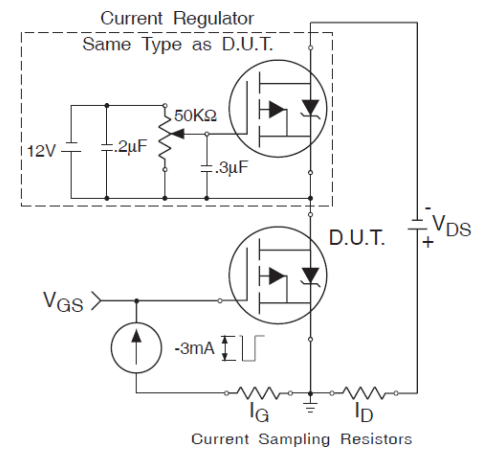


Fig 17b. Gate Charge D.U.T. Test Circuit

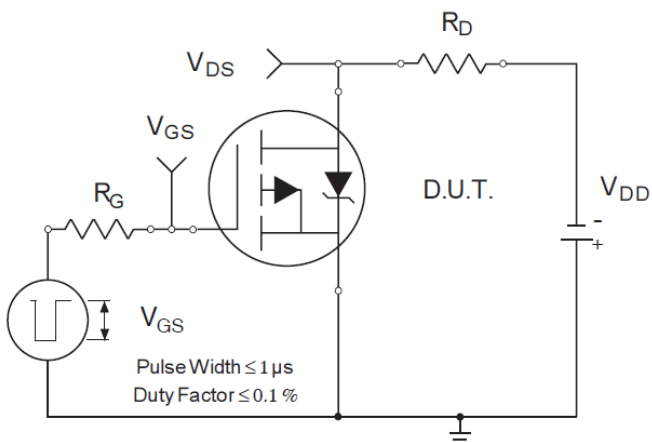


Fig 18a. Switching Time Test Circuit

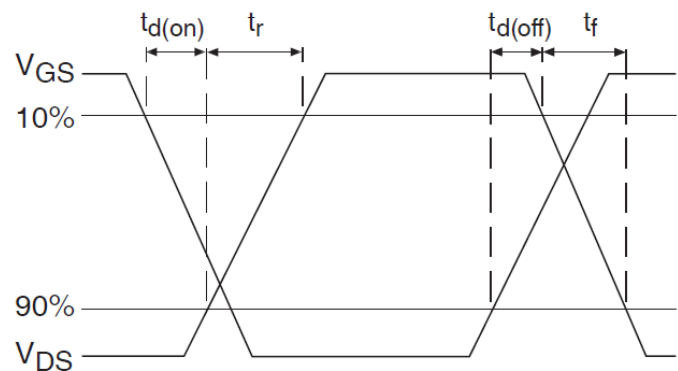
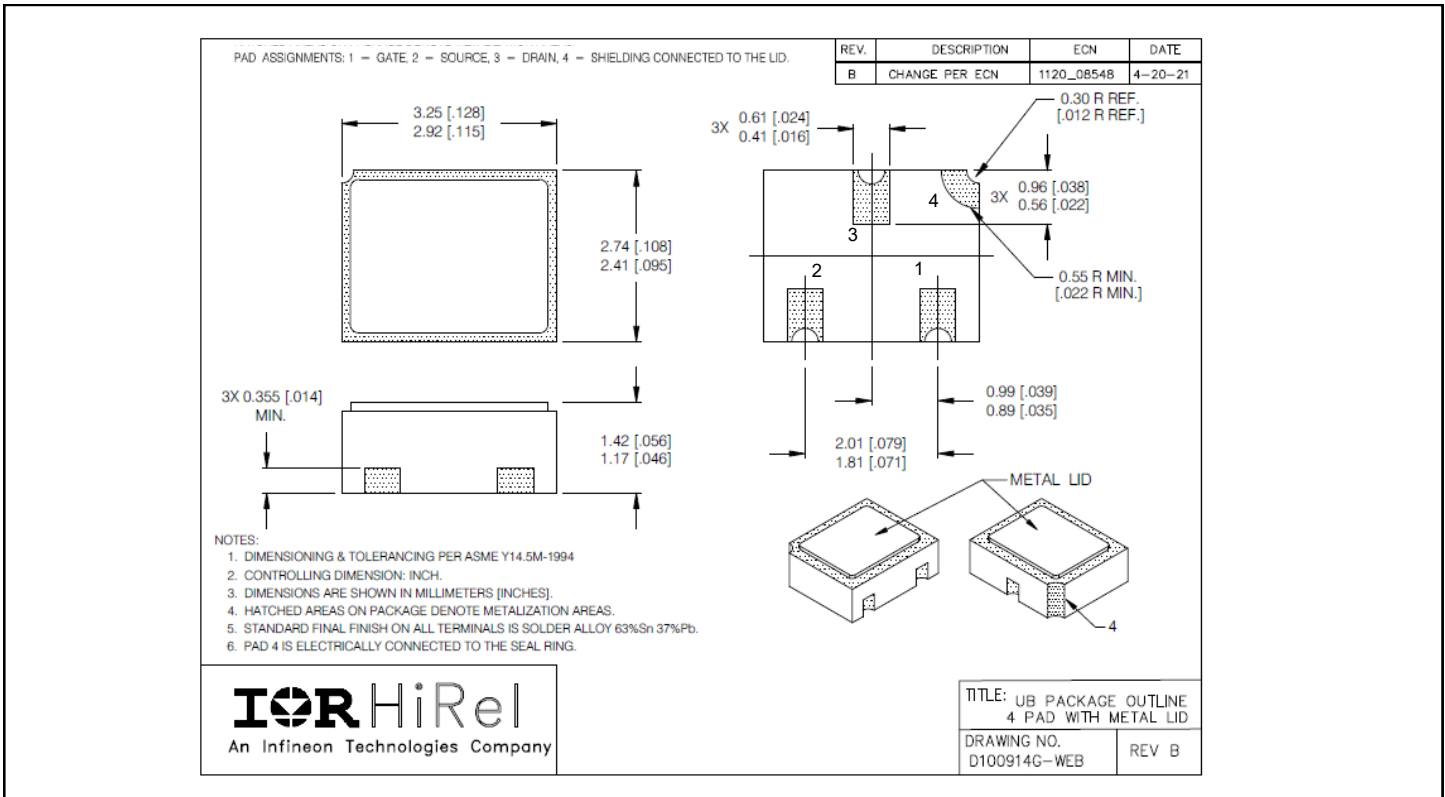


Fig 18b. Switching Time Waveforms

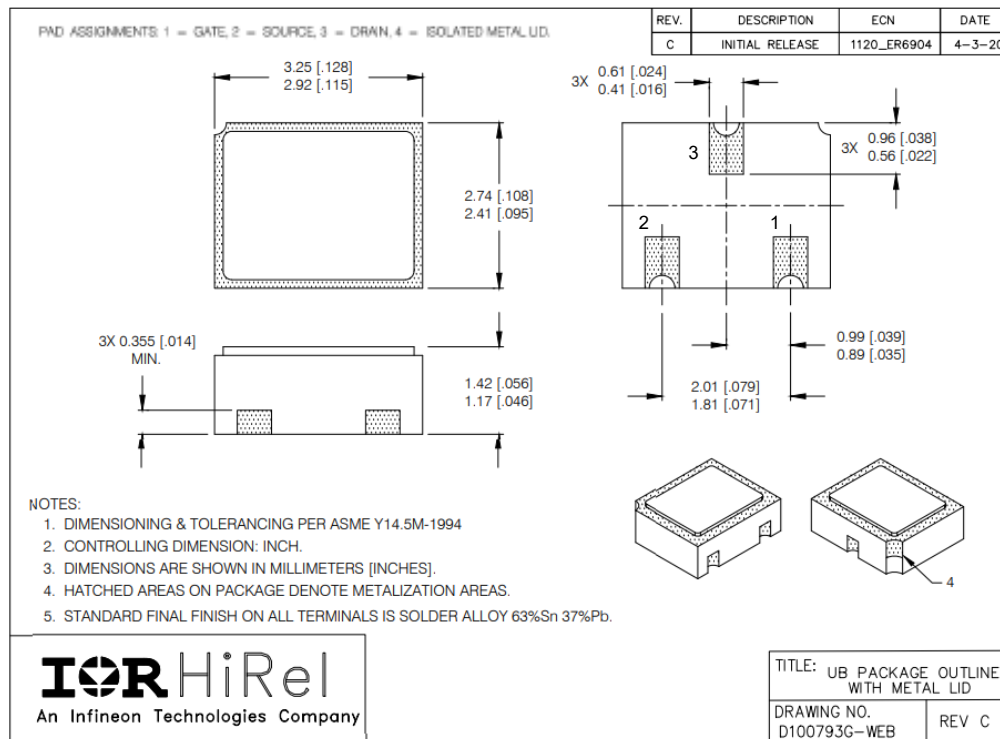
Note: For the most updated package outline, please see the website: [UB](#)

Case Outline and Dimensions - UB (Shielded Metal Lid Connected to 4th Pad)



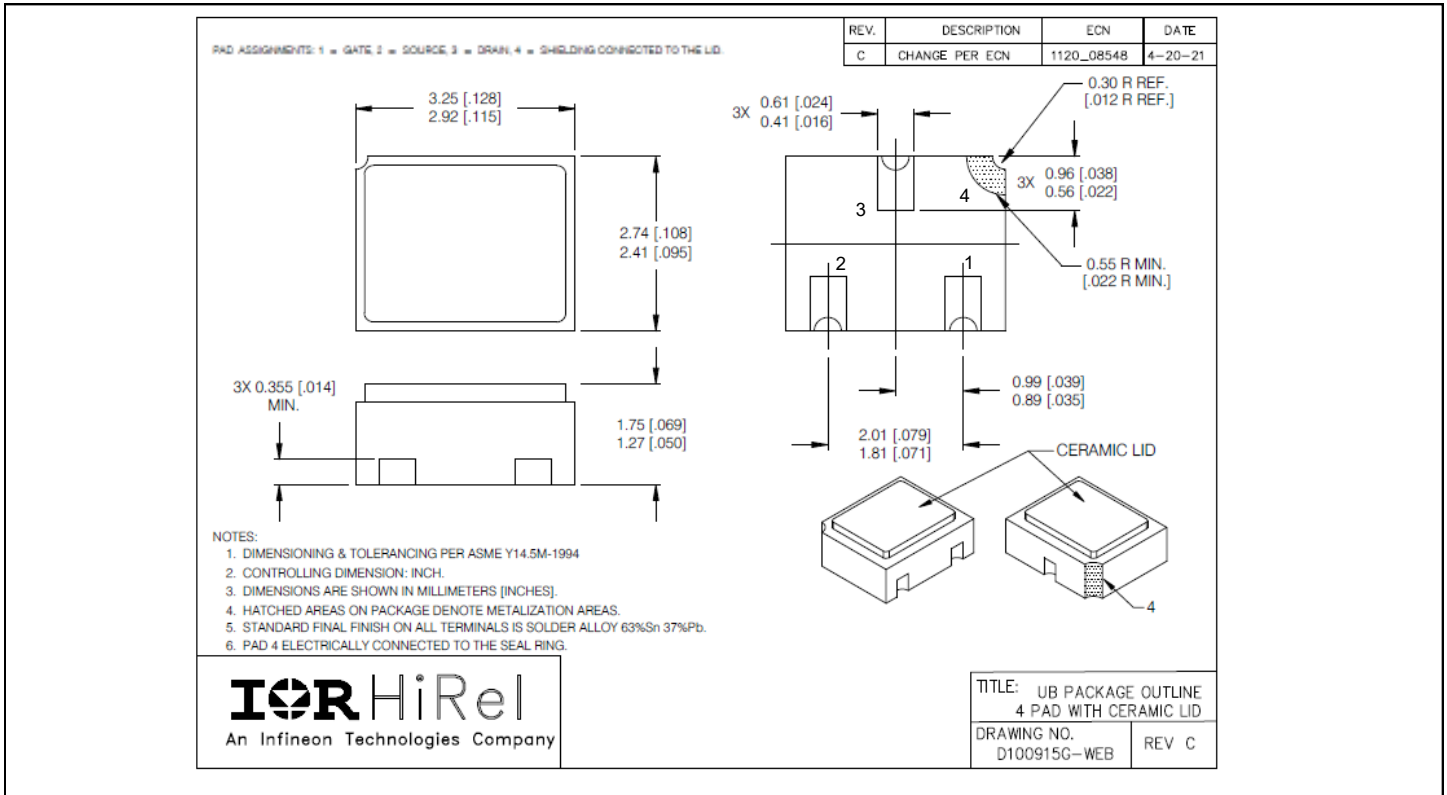
Note: For the most updated package outline, please see the website: [UBN](#)

Case Outline and Dimensions - UBN (Isolated Metal Lid, No 4th Pad)



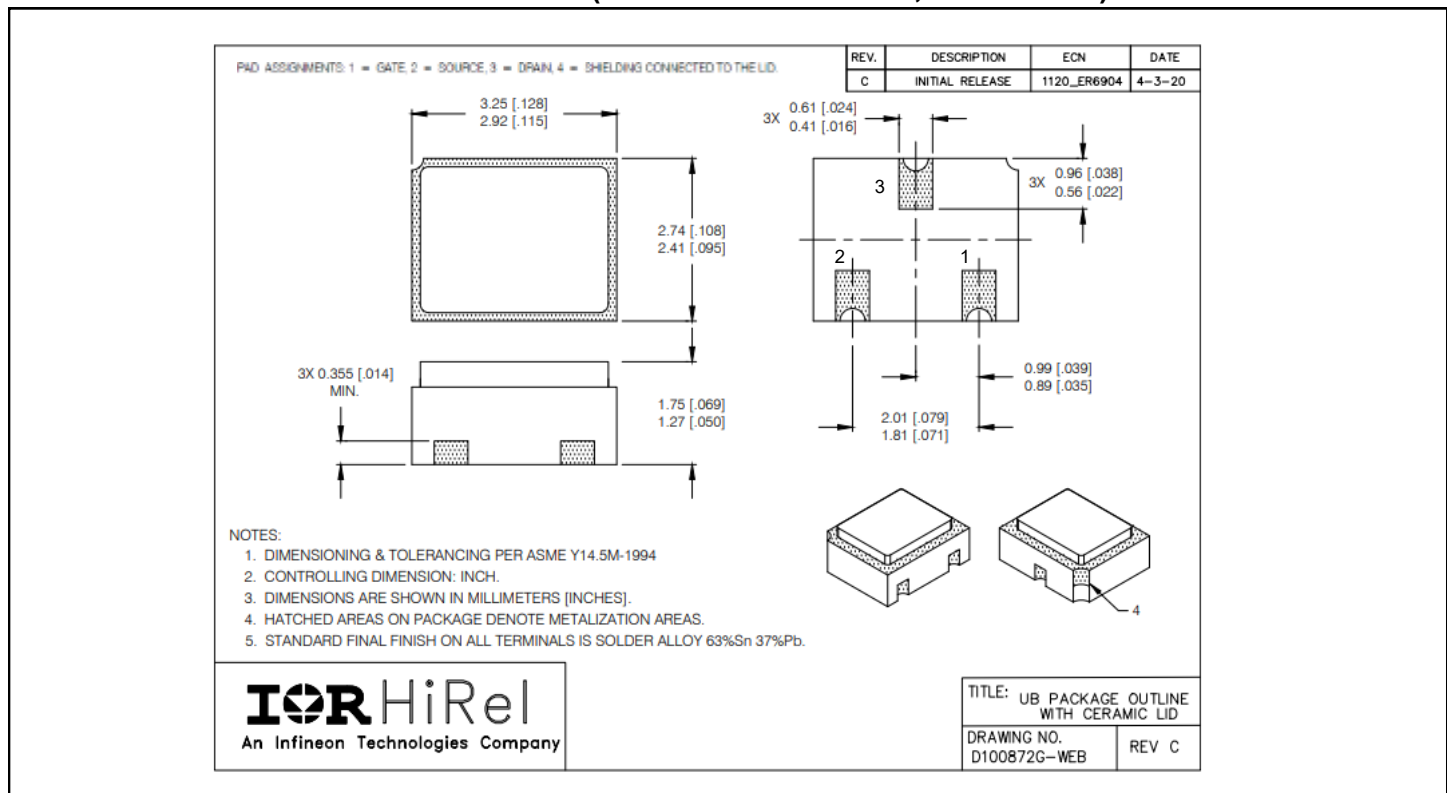
Note: For the most updated package outline, please see the website: [UBC](#)

Case Outline and Dimensions - UBC (Shielded Ceramic Lid Connected to 4th Pad)




Note: For the most updated package outline, please see the website: [UBCN](#)

Case Outline and Dimensions - UBCN (Isolated Ceramic Lid, No 4th Pad)




Additional Product Summary (continued from pages 1 and 3)


Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number	 UBN (ISOLATED METAL LID)
IRHLUBN7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UBN	
IRHLUBN7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UBN	

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number	 UBC (SHIELDED CERAMIC LID)
IRHLUBC7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UBC	
IRHLUBC7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UBC	

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number	 UBCN (ISOLATED CERAMIC LID)
IRHLUBCN7970Z4	100 kRads(Si)	1.4Ω	-0.53A	JANSR2N7626UBCN	
IRHLUBCN7930Z4	300 kRads(Si)	1.4Ω	-0.53A	JANSF2N7626UBCN	

IMPORTANT NOTICE

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