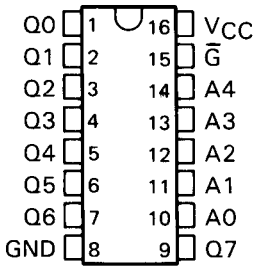
TBP18S030, TBP18SA030
256 BITS (32 WORDS BY 8 BITS)
PROGRAMMABLE READ-ONLY MEMORIES

SDMS024 – SEPTEMBER 1979 – REVISED AUGUST 1984

- **Titanium-Tungsten (Ti-W) Fuse Link for Reliable Low-Voltage Full Family Compatible Programming**
- **Full Decoding and Fast Chip Select Simplify System Design**
- **P-N-P Inputs for Reduced Loading on System Buffers/Drivers**
- **Applications Include:**
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables
- **Choice of 3-State or Open-Collector Outputs**

TBP18SA030, TBP18S030 . . . J OR N PACKAGE
(TOP VIEW)



description

These monolithic TTL programmable read-only memories (PROMs) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in 20 microseconds. The Schottky-clamped versions of these PROMs offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

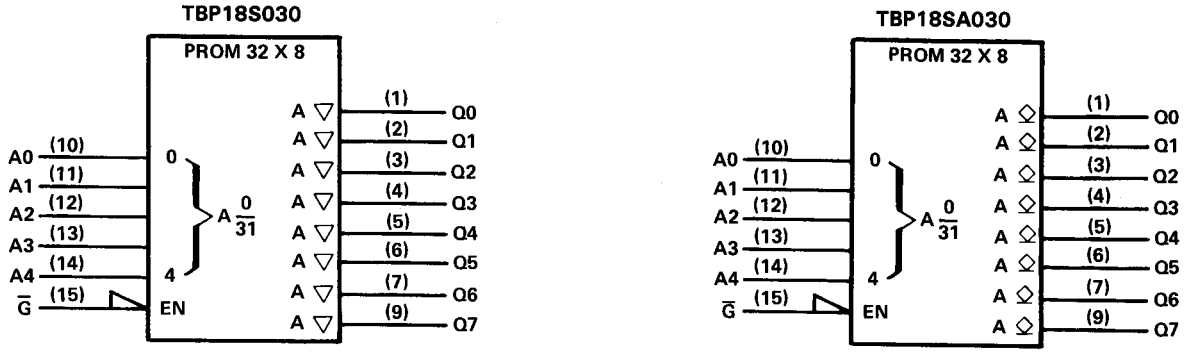
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROMs are supplied with a low-logic level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

A low level at the chip-select input(s) enables each PROM. The opposite level at any chip-select input causes the outputs to be off.

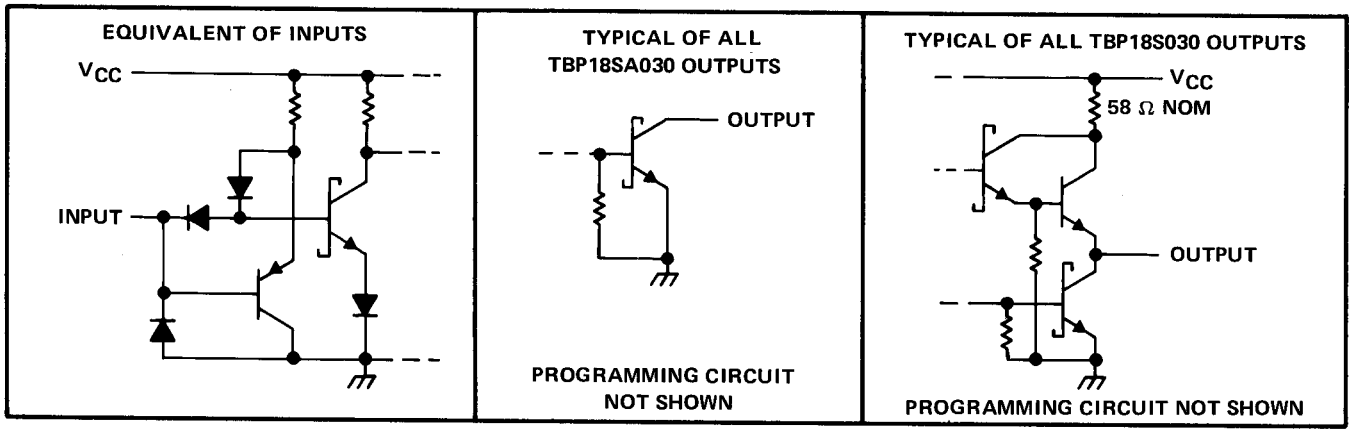
The three-state output offers the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull up.

A MJ suffix designates full-temperature circuits (formerly 54 Family) and are characterized for operation over the full military temperature range of −55°C to 125°C. A J or N suffix designates commercial-temperature circuits (formerly 74 Family) and are characterized for operation from 0°C to 70°C.

logic symbol



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Operating free-air temperature range: Full-temperature-range circuits ..... −55°C to 125°C
Commercial-temperature-range circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

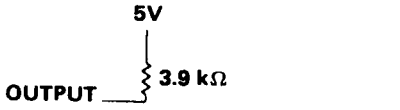
recommended conditions for programming TBP18S', TBP18SA PROMs

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	9	9.25	9.5	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse X (see Figure 2 and Note 3)		15	25	100	μs
Programming duty cycle for Y pulse			25	35	%
Free-air temperature		20	25	30	°C

NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.
2. The TBP18S030, TBP18SA030 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level.

programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current into the programmer output is 150 mA.
5. Step V_{CC} to 9.25 nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 μs and 1 ms after V_{CC} has reached its 9.25 level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within the range of 1 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

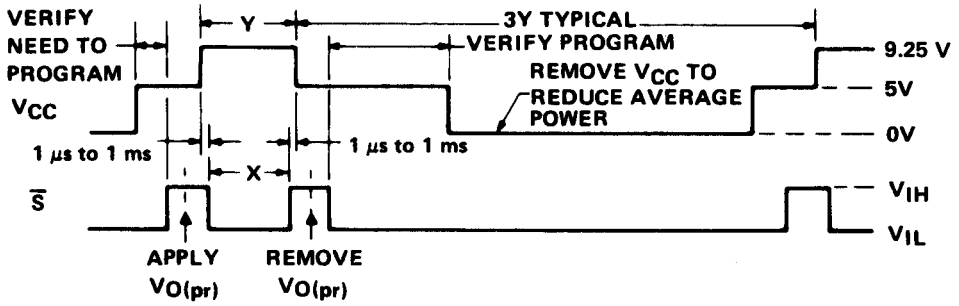


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions (see Note 4)

PARAMETER		TBP18S030			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	V
	J, N	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2	mA
	J,N			−6.5	
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	MJ	−55		125	°C
	J ,N	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS†	FULL TEMP (MJ)			COMM. TEMP (J,N)			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V,			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 5		80	110		80	110	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM CHIP SELECT (ENABLE TIME)			t_{dis} DISABLE TIME FROM HIGH OR LOW LEVEL			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP18S030MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, 5 pF for t_{dis}, See Note 6		25	50		12	30		8	30	ns
TBP18S030			25	40		12	25		8	20	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTES: 4. MJ designates full-temperature circuits (formerly 54 Family), J and N designate commercial-temperature circuits (formerly 74 Family).
5. The typical values of I_{CC} are with all outputs low.

recommended operating conditions (see Note 4)

PARAMETER		TBP18SA030			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	V
	J, N	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	MJ	−55		125	°C
	J, N	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 5			80	110	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM CHIP SELECT (ENABLE TIME)			t_{PLH} PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT FROM CHIP SELECT (DISABLE TIME)			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP18SA030MJ	C_L = 30pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 6		25	50		12	30		12	30	ns
TBP18SA030			25	40		12	25		12	25	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. MJ designates full-temperature circuits (formerly 54 Family), J and N designate commercial-temperature circuits (formerly 74 Family).
5. The typical values of I_{CC} are with all outputs low.
6. Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JBP18S030MJ	NRND	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JBP18S030MJ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

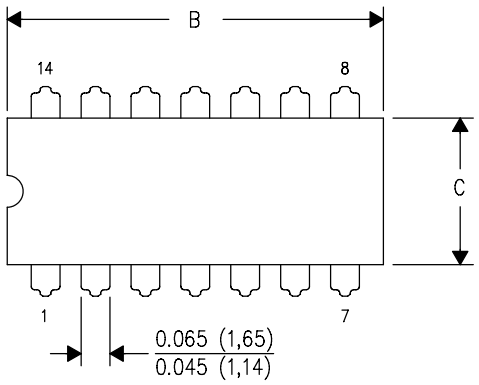
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

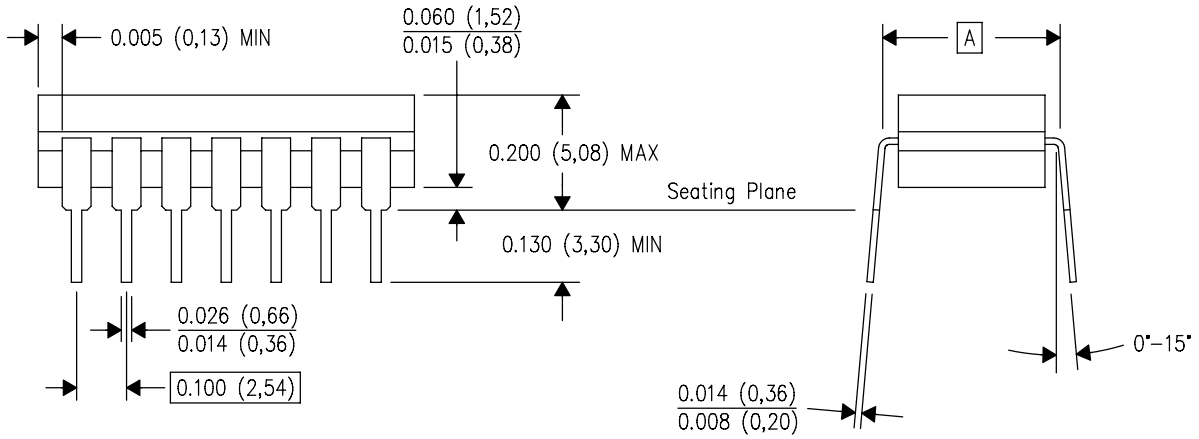
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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