天鈺科技股份有限公司

Fitipower Integrated Technology Inc

JD9851

Internal Command

240RGB x 320 dot, 262k color,
with internal GRAM, a-si TFT LCD Single Chip Driver

Preliminary Version 0.00
2018/11/23

1. Revision History

Version	Date	Description of modification
0.00	2018/12/28	New setup

2. JADARD COMMAND LIST

2.1. Jadard page 0 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
B0	SEQUENCE_CTRL	R/W	-	DC0H[2:0]			-	DC1H[2:0]			01
		R/W	-	DC2H[2:0]			-	DC3H[2:0]			23
		R/W	-	-	-	-	-	DC7H[2:0]			06
		R/W	DC0L	DC1L	DC2L	DC3L	DC4L	DC5L	DC6L	DC7L	88
		R/W	T0P[1:0]		T1P[1:0]		T8P[1:0]		-	VCOM_SEL	64
		R/W	-	SOFT0H[2:0]			-	SOFT0L[2:0]			06
		R	-	-	-	-	-	-	-	POW_ON_STATE	00
B7	GAMMA_SET	R/W	-	VGSP_S[6:0]							09
		R/W	VGMP_S[7:0]								60
		R/W	-	VGSN_S[6:0]							09
		R/W	VGMN_S[7:0]								38
B8	OTP_SET	R/W	-	-	VPP_DT[1:0]		VPP_VGHZ_CLK[3:0]				3F
		R/W	VPP_VGHZ_RT	VPP_VGHZ_NC	-	-	-	-	VPP_VGHZ_S[1:0]		00
B9	POW_CTRL	R/W	-	AP[2:0]			-	-	VCOM_EN	VGM_EN	33
		R/W	AVDDZ_NC	AVDDZ_DNC	AVEEZ_NC	-	VGHZ_NC	VGLZ_NC	-	-	08
		R/W	MVZ_EN	MVZ_D_EN	-	-	VGHZ_EN	VGLZ_EN	-	-	CC
BB	DCDC_SEL	R/W	-	VGHZ_RT	-	-	VGLZ_S[3:0]				4A
		R/W	-	AVDDZ_D_S[2:0]			AVDDZ_S[1:0]		AVEEZ_S[1:0]		79
		R/W	VGHZ_CLK[3:0]				VGHZ_CLKB[1:0]		VGHZ_CLKP[1:0]		40
		R/W	VGLZ_CLK[3:0]				VGLZ_CLKB[1:0]		VGLZ_CLKP[1:0]		40
		R/W	MVZ_S_CLK[3:0]				MVZ_S_CLKB[1:0]		MVZ_S_CLKP[1:0]		70
		R/W	MVZ_G_CLK[3:0]				MVZ_G_CLKB[1:0]		MVZ_G_CLKP[1:0]		70
		R/W	NMVZ_D_CLK[3:0]				NMVZ_D_CLKB[1:0]		NMVZ_D_CLKP[1:0]		F0
		R/W	MVZ_D_CLK[3:0]				MVZ_D_CLKB[1:0]		MVZ_D_CLKP[1:0]		70
BC	VDDD_CTRL	R/W	-	VDDD_S0[2:0]			AVSSN_EN	AVSSN_S[2:0]			3D
		R/W	-	VDDD_S1[2:0]			VDDD_VCI_EN	VDDD_S2[2:0]			3C
BD	SETRGBIF	R/W	-	-	BLK_OPT	DEM	VSPL	HSPL	DEPL	PCPL	22
		R/W	-	-	RGB_SEL[1:0]		-	-	RGB_SYNC_LN[9:8]		00
		R/W	RGB_SYNC_LN[7:0]								A0
		R/W	RGB_SYNC_RESO_X[7:0]								3C
		R/W	RGB_SYNC_VBP[7:0]								0A
		R/W	RGB_SYNC_HBP[7:0]								16
BE	GAS_CTRL	R/W	-	-	-	-	-	-	-	-	00
		R/W	GAS_SLPIN_EN	GAS_OUT_EN	GAS_VCI_EN	GAS_IOVCC_EN	GAS_BLK_NUM[3:0]				F2
		R/W	GAS_DBS_SEN	GAS_DBS_GEN	GAS_DBS_LTH[5:0]						8C
		R/W	-	-	DC_GAS_VGH_EN	DC_GAS_VGL_EN	-	-	DC_GAS_MVZ_EN	DC_GAS_MVZ_D_EN	20

C0	SETSTBA	R/W	-	GAP[2:0]			SAP[3:0]				**22**
		R/W	GAP2_EN	GAP2[2:0]			-	-	-	-	**20**
C1	SETPANEL	R/W	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	CFHR	-	**00**
C2	SET_BIST	R/W	-	LNPERLVL[1:0]		BIST_CP_OPT	TEST_PAT_EN	TEST_PATTERN[2:0]			**00**
C3	SETRGBCYC	R/W	-	-	-	-	IDLE_TYPE	RGB_INV_NP[2:0]			**0C**
		R/W	-	RGB_INV_PI[2:0]			-	RGB_INV_I[2:0]			**44**
		R/W	-	-	-	-	RGB_GND[3:0]				**07**
		R/W	-	-	-	RGB_EQ1[4:0]					**0E**
		R/W	-	-	RGB_CHGEN_ON[5:0]						**08**
		R/W	RGB_CHGEN_OFF[7:0]								**50**
		R/W	GASHORT_ON[7:0]								**51**
		R/W	RGB_OFF[7:0]								**71**
		R/W	-	-	GAOPOFFEN	GAOPOFF[4:0]					**2C**
C4	SET_TCON	R/W	-	-	LN[9:8]		TE_OPT[1:0]		RSO[1:0]		**00**
		R/W	LN[7:0]								**A0**
		R/W	SLT_NP[7:0]								**79**
		R/W	VFP_NP[7:0]								**0E**
		R/W	VBP_NP[7:0]								**0A**
		R/W	HBP_NP[7:0]								**16**
		R/W	SLT_I[7:0]								**79**
		R/W	VFP_I[7:0]								**0E**
		R/W	VBP_I[7:0]								**0A**
		R/W	HBP_I[7:0]								**16**
		R/W	SLT_PI[7:0]								**79**
		R/W	VFP_PI[7:0]								**0E**
		R/W	VBP_PI[7:0]								**0A**
		R/W	HBP_PI[7:0]								**16**
		R/W	HBP_NCK[3:0]				HFP_NCK[3:0]				**82**
		R/W	TCON_OPT1[15:8]								**00**
		R/W	TCON_OPT1[7:0]								**03**
C8	SET_R_GAMMA	R/W	-	-	RPA15[5:0]						**3F**
		R/W	-	-	RPA14[5:0]						**3E**
		R/W	-	-	RPA13[5:0]						**23**
		R/W	-	-	RPA12[5:0]						**11**
		R/W	-	-	RPA11[5:0]						**13**
		R/W	-	-	RPA10[5:0]						**14**
		R/W	-	-	RPA9[5:0]						**13**
		R/W	-	-	RPA8[5:0]						**17**
		R/W	-	-	RPA7[5:0]						**1B**
		R/W	-	-	RPA6[5:0]						**1E**
		R/W	-	-	RPA5[5:0]						**22**

		R/W	-	-	RPA4[5:0]						**23**
		R/W	-	-	RPA3[5:0]						**25**
		R/W	-	-	RPA2[5:0]						**28**
		R/W	-	-	RPA1[5:0]						**1F**
		R/W	-	-	RPA0[5:0]						**0E**
		R/W	-	-	RNA15[5:0]						**3F**
		R/W	-	-	RNA14[5:0]						**3E**
		R/W	-	-	RNA13[5:0]						**23**
		R/W	-	-	RNA12[5:0]						**10**
		R/W	-	-	RNA11[5:0]						**12**
		R/W	-	-	RNA10[5:0]						**14**
		R/W	-	-	RNA9[5:0]						**11**
		R/W	-	-	RNA8[5:0]						**12**
		R/W	-	-	RNA7[5:0]						**14**
		R/W	-	-	RNA6[5:0]						**17**
		R/W	-	-	RNA5[5:0]						**18**
		R/W	-	-	RNA4[5:0]						**16**
		R/W	-	-	RNA3[5:0]						**18**
		R/W	-	-	RNA2[5:0]						**18**
		R/W	-	-	RNA1[5:0]						**18**
		R/W	-	-	RNA0[5:0]						**0E**
CD	SETPHY1	R/W	-	RX_LDO_SEL[2:0]			-	-	HS_RX_RT[1:0]		**31**
		R/W	-	TX_LDO_SEL[2:0]			-	-	LP_TX_SR[1:0]		**31**
D0	SET_GD	R/W	-	-	-	-	-	GD_GAS_GATE_CLK	GD_EN_GND_VCI	GD_LRSW	**04**
		R/W	-	-	GD_ON[5:0]						**0C**
		R/W	GD_OFF[7:0]								**6B**
		R/W	-	-	GD_EQ_PTR0[5:0]						**0F**
		R/W	GD_EQ_PTR1[7:0]								**07**
		R/W	-	-	-	GD_PTGISC	GD_ISC[3:0]				**03**
D7	RAMCTRL	R/W	-	-	SPI_2LAN_EN	RP	RM	-	DM[1:0]		**00**
		R/W	SCL_PL	EXT_VS_PL	EPF[1:0]		ENDIAN	-	MDT[1:0]		**00**
D8	AUTO_DISP_SETTING	R/W	-	-	-	-	GON	DTE	DISP_REG[1:0]		**08**
		R/W	-	-	DISP_SW_OPT[1:0]		-	BLK_DISABLE	BLK_MODE[1:0]		**01**
D9	OTP_PROG	R/W	OTP_MASK[7:0]								**00**
		R/W	-	-	-	-	-	-	-	OTP_INDEX[8]	**00**
		R/W	OTP_INDEX[7:0]								**00**
		R/W	OTP_PROGRAM_ALL	OTP_TWOBITS_SEL	OTP_PGM_SEL	OTP_READ_SINGLE	OTP_WRITE_SINGLE	OTP_LOAD_DISABLE	OTP_INT_VPP	OTP_AUTO_PROG		**00**
		R	OTP_RDATA[7:0]								**-**
		R/W	OTP_WDATA[7:0]								**00**
		R/W	OTP_PPROG	OTP_VPP_SEL	OTP_PRD	OTP_PWE	-	-	OTP_PTM[1:0]		**00**

DD	SET_WD	R/W	-	WD_OFF	WD_MODE[1:0]		FBLK_EN	WD_CLK_SEL[2:0]			**2C**
		R/W	WD_TIMER_TCON[7:0]								**A3**
		R/W	MP_ESD_MODE[1:0]		MP_ESD_FLAG_EN	MP_ESD_E_V_FLAG	MP_ESD_E_V_AM	ESD_TCON_OPT	ESD_SD_OPT	ESD_PRT_EN	**00**
		R	-	-	-	-	-	-	WD_FMS	WD_FBLK	**00**
DE	SET_PAGE	R/W	-	-	-	-	-	PAGE[2:0]			**00**
DF	SET_PASSWD	R/W	PASSWD1[7:0]								**00**
		R/W	PASSWD2[7:0]								**00**
		R/W	PASSWD3[7:0]								**00**
E6	SETECO	R/W	-	ECO0[6:0]							**00**
E8	UP_START_CTRL	R/W	UP_KEY1[7:0]								00
		R/W	UP_KEY2[7:0]								00
		R/W	UP_START_EN[7:0]								00
		R/W	PWR_KEY[7:0]								00
E9	SETID	R/W	-	-	-	-	-	-	-	-	**00**
		R/W	ID1[7:0]								**98**
		R/W	ID2[7:0]								**51**
		R/W	ID3[7:0]								**01**
		R/W	ID4[7:0]								**00**
		R	-	-	-	-	-	-	ID_OTP_TIMES[1:0]		**00**

2.2. Jadard page 1 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
B5	PWM_CTRL	R/W	-	-	-	LE_LEDON_EN	LE_LEDON_POL	-	LE_LEDPWM_POL	LE_LED_VOL	0A
		R/W	LE_NONNORM_DD_EN	LE_EN_EXT_EN	LE_PWM_SYNC2VS	LE_DD_RST	-	LE_PWM_DUTY_PCN[2:0]			C1
		R/W	LE_SEL_CLK_DIV[7:0]								01
		R/W	LE_N_VAL[7:0]								40

2.3. Jadard page 2 command

Index	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
B8	DCDC_SET	R/W	-	VCL_S	VCIP2X_S[1:0]		VGHZ_OV_PAVDD	AVDDZ_D_OV_S[2:0]			**19**
		R/W	EQ2_EN	-	DCDC_EQ2[5:0]						**97**
		R/W	EQ3_EN	-	DCDC_EQ3[5:0]						**9E**
		R/W	-	-	DCDC_GOV_S[5:0]						**32**
		R/W	-	-	DCDC_GOV_E[5:0]						**17**
C1	SETRGBCYC2	R/W	-	SDPRDUM	SDDUM[1:0]		SDSW[1:0]		SDPORCH[1:0]		**11**
		R/W	RGB_SPAIF[3:0]				RGB_SPAIB[3:0]				**66**
		R/W	RGB_SNAIF[3:0]				RGB_SNAIB[3:0]				**66**
		R/W	-	-	SDSW_GAS[1:0]		-	-	SDPARTIAL[1:0]		**00**
C5	SET_OSCM	R/W	-	OSC_DIV_EN0	OSC_DIV_EN1[2:0]			OSCM_ADJ[2:0]			**01**
D7	SET_INH_CHKSUM	R/W	-	-	-	SLPIN_RESET_EN	INH_CHKSUM_OFF	INH_CHKSUM_SEL[2:0]			**1A**
E9	STD_SEL	R/W	-	-	RX0F_B0_SEL	-	RX0A_B2_MIX	RX0A_B0_MIX	-	-	**00**

2.4. Jadard page 0 command Description

2.4.1. SEQUENCE CTRL: Power on sequence control (Page0 - B0h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	R/W	1	0	1	1	0	0	0	0	B0
Parameter 1	R/W	-	DC0H[2:0]			-	DC1H[2:0]			-
Parameter 2	R/W	-	DC2H[2:0]			-	DC3H[2:0]			-
Parameter 3	R/W	-	-	-	-	-	DC7H[2:0]			-
Parameter 4	R/W	DC0L	DC1L	DC2L	DC3L	DC4L	DC5L	DC6L	DC7L	-
Parameter 5	R/W	T0P[1:0]		T1P[1:0]		T8P[1:0]		-	VCOM_SEL	-
Parameter 6	R/W	-	SOFT0H[2:0]			-	SOFT0L[2:0]			-
Parameter 7	R	-	-	-	-	-	-	-	POW_ON_STATE	-

Description

This command is used to set power on sequence Related Setting.

VCOM_SEL:no use.

DC0H[2:0]: Select the AVDD power on timing(P1~P8).
DC1H[2:0]: Select the VCL power on timing(P1~P8).
DC2H[2:0]: Select the AVEE power on timing(P1~P8).
DC3H[2:0]: Select the VGL power on timing(P1~P8).
DC7H[2:0]: Option.

Power-on Sequence option		
DCxH[2:0]	Go High	
0	P1	DC0H default
1	P2	DC1H default
2	P3	DC2H default
3	P4	DC3H default
4	P5	DC4H fixed
5	P6	DC5H fixed
6	P7	DC6H fixed / DC7H default
7	P8	

DC0L: Select the AVDD power off timing(P10~P11).
DC1L: Select the VCL power off timing(P10~P11)
DC2L: Select the AVEE/VDDN power off timing(P10~P11)
DC3L: Select the VGL power off timing(P10~P11)
DC4L: Select the VGH power off timing(P10~P11)
DC5L: Select the Gamma reference voltage power off timing(P10~P11)
DC6L: Select the VCOM power off timing(P10~P11)
DC7L: Option

Power-off Sequence option		
DCxL	Go Low	
0	P10	DC1-3L,DC5-7L default
1	P11	DC0/4L default

TP0[1:0]: Select the period time for T0.
TP1[1:0]: Select the period time for T1.
TP8[1:0]: Select the period time for T8.

Power-on Period option		
TxP[1:0]	Period	
0	0.5ms	
1	3ms	T0 / T8 defualt

2	6ms	T1 default
3	10ms	

SOFT0H[2:0]: Select the AVDD soft pump start timing(P0~P7).

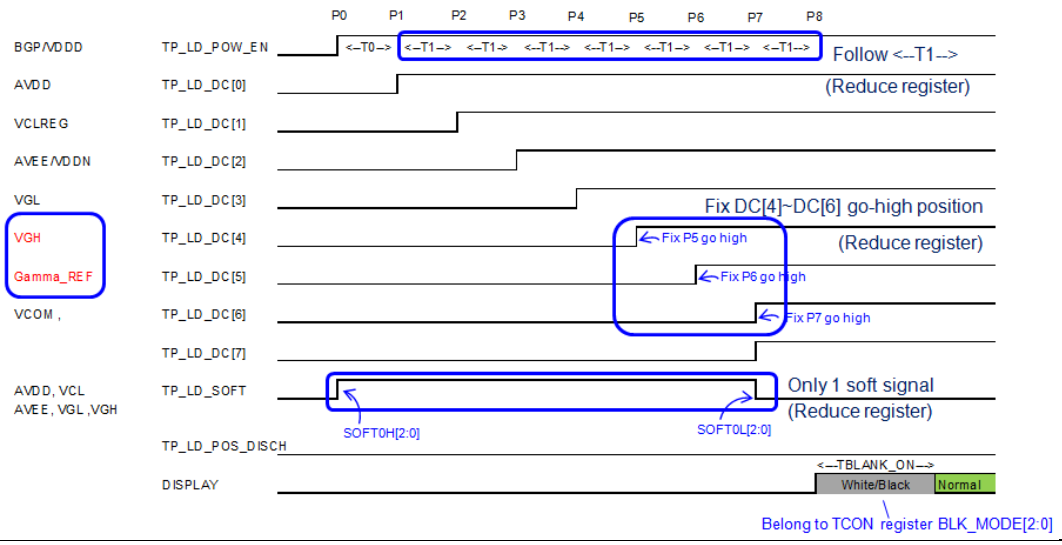
Soft Start Option		
SOFTxH[2:0]	Go High	
0	P0	SOFT0H default
1	P1	
2	P2	
3	P3	
4	P4	
5	P5	
6	P6	
7	P7	

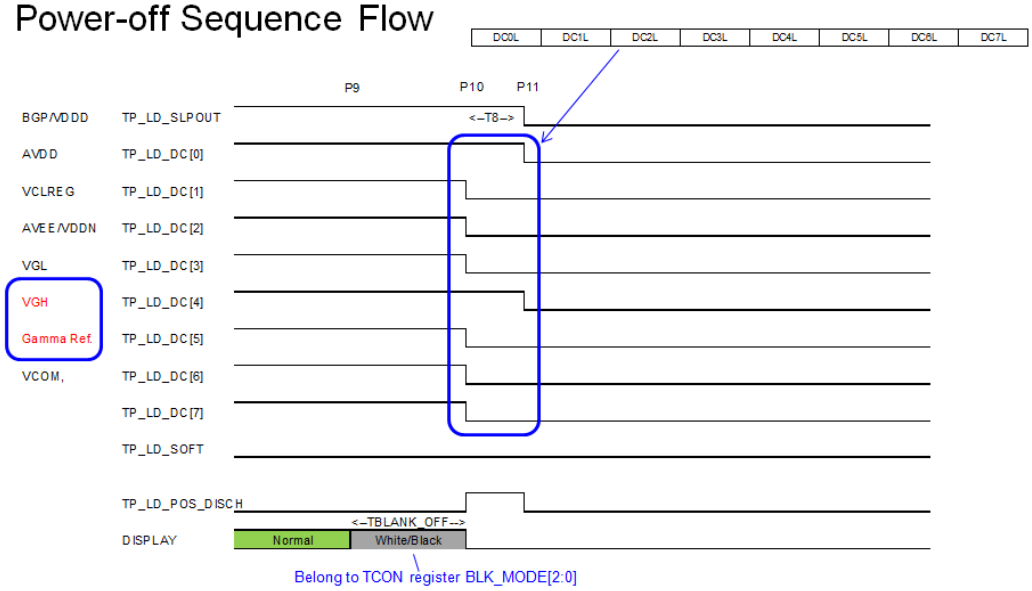
SOFT0L[2:0]: Select the AVDD soft pump stop timing(P1~P8).

Soft End Option		
SOFTxL[2:0]	Go Low	
0	P1	
1	P2	
2	P3	
3	P4	
4	P5	
5	P6	
6	P7	SOFT0L default
7	P8	

POW_ON_STATE: All power ready when this bit is high.

- Power-on Sequence Flow



	● Power-off Sequence Flow 
Restriction	-

2.4.2. GAMMA_SET: Set positive / negative voltage of Gamma power (Page0 - RB7h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	0	1	1	1	B7
Parameter 1	**R/W**	-	VGSP_S[6:0]							-
Parameter 2	**R/W**	VGMP_S[7:0]								-
Parameter 3	**R/W**	-	VGSN_S[6:0]							-
Parameter 4	**R/W**	VGMN_S[7:0]								-

Description

This command is used to set postive / Negative reference volatge of Gamma. (Gamma setting please refer to page2 BEh)

VGMP_S[7:0]: Set power source volatge of postive polarity.

VGMP_S[7:0]	VGMP(v)
00h	0
01h	2.125
~	0.025/step
60h	4.500
~	0.025/step
FDh	8.425
FEh	AVDD
FFh	Hiz

VGSP_S[6:0]: Set refernce volatge of postive polarity.

VGSP_S[6:0]	VGSP(v)
00h	0
01h	0.300
~	0.025/step
09h	0.500
~	0.025/step
10h	0.675
11h	0.700
~	0.025/step
7Eh	3.425
7Fh	Hiz

VGMN_S[7:0]: Set power source volatge of negative polarity.

VGMN_S[7:0]	VGMN(v)
00h	0
01h	-2.125
~	0.025/step
38h	-3.500
~	0.025/step
FDh	-8.425
FEh	AVEE
FFh	Hiz

	VGSN_S[6:0]: Set refernce volatge of negative polarity. VGSN_S[6:0] / VGSN(v) 00h / 0 01h / 0.300 ~ / 0.025/step 09h / 0.500 ~ / 0.025/step 7Eh / 3.425 7Fh / HiZ
Restriction	-

2.4.3. OTP_SET: Set internal OTP program related setting(Page0 - B8h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	1	0	0	0	B8
Parameter 1	**R/W**	-	-	VPP_DT[1:0]		VPP_VGHZ_CLK[3:0]				-
Parameter 2	**R/W**	VPP_VGHZ_RT	VPP_VGHZ_NC					VPP_VGHZ_S[1:0]		-

Description

This command is used to set internal OTP program relaetd setting.

VPP_DT[1:0]:When INT_VPP=1(D9h), internal OTP will program 1bit step by step until 1 byte program finished. VPP_DT[1:0] can define delay time between each cycle.

VPP_DT[2:0]	Delaytime (ms)
0h	0.25
1h	0.5
2h	1
3h	2

VPP_VGHZ_CLK[3:0] :
When OTP_INT_VPP=1, TP_LT_CPCLKZ [5] = VPP_VGHZ_CLK[3:0])

VPP_VGHZ_CLK[3:0] :	Frequence	VPP_VGHZ_CLK[3:0]	Frequence
0	OSCM / 256	8	OSCM / 768
1	OSCM / 128	9	OSCM / 384
2	OSCM / 64	A	OSCM / 192
3	OSCM / 32	B	OSCM / 96
4	OSCM / 16	C	OSCM / 48
5	OSCM / 8	D	OSCM / 24
6	OSCM / 4	E	OSCM / 12
7	OSCM / 2	F	OSCM / 6

VPP_VGHZ_RT : Working on OTP_INT_VPP=1.

VPP_VGHZ_RT	VGH (V)
0	2*AVDD
1	4*AVDD

VPP_VGH_S[4:0]: When OTP_INT_VPP=1, set VGH voltage level of internal OTP program.

VPP_VGH_S [1:0]	VGHZ (V)
00h	8.2
01h	8.4
02h	8.6
03h	8.8

Restriction	-

2.4.4. POWER_CTRL2: Set power function related setting (Page0 - B9h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	1	0	0	1	B9
Parameter 1	**R/W**	-	AP[2:0]			-	-	VCOM EN	VGM_EN	-
Parameter 2	**R/W**	AVDDZ_NC	AVDDZ_D_NC	AVEEZ_NC	-	VGHZ_NC	VGLZ_NC	-	-	-
Parameter 3	**R/W**	MVZ_EN	MVZ_D_EN	-	-	VGHZ_EN	VGLZ_EN	-	-	-

Description

This command is used to control engineer mode of power related setting.

AP[2:0]: Adjust the ratio of fixed current for the operatinal amplifier in the power supply circuit.

AP[2:0]	Bias Current
0h	25%
1h	50%
2h	75%
3h	100%
4h	125%
5h	150%
6h	175%
7h	200%

VCOM_EN: Control VCOM regulator output.

VCOM_EN	VCOM
0	Hi-Z
1	Regulator on

VGM_EN: Control Gamma power regulator output

VGM_EN	VDDN
0	Hi-Z
1	Regulator on

AVDDZ_NC: Set AVDDZ output state

AVDDZ_NC	AVDDZ output
0	Clamping
1	No clamping

AVDDZ_D_NC: Set AVDDZ_D output state

AVDDZ_D_NC	AVDDZ_D output
0	Clamping
1	No clamping

AVEEZ_NC: Set AVEEZ output state

AVEEZ_NC	AVEEZ output
0	Clamping
1	No clamping

VGHZ_NC: Set VGHZ output state.

VGHZ_NC	VGHZ output
0	Clamping
1	No clamping

VGLZ_NC: Set VGLZ output state

VGLZ_NC	VGLZ output
0	Clamping
1	No clamping

VGHZ_EN: Control VGHZ DC/DC circuit On/Off.

VGHZ_EN	VGHZ DC/DC circuit
0	Disbale
1	Enable

VGLZ_EN: Control VGLZ DC/DC circuit On/Off.

VGLZ_EN	VGLZ DC/DC circuit
0	Disbale
1	Enable

MVZ_EN: Select DCDC for Source block turn on and turn off

MVZ_EN	MVZ
0	Disable
1	Enable

MVZ_D_EN: Set DCDC for MV_Z block enable

MVZ_D_EN	MVZ_D
0	Disable
1	Enable

Restriction	

2.4.5. DCDC_SEL: Power mode and charge pump related setting (Page0 - BBh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	R/W	1	0	1	1	1	0	1	1	BB
Parameter 1	R/W	-	VGHZ_RT	-	-	VGLZ_S[3:0]				-
Parameter 2	R/W	-	AVDDZ_D_S[2:0]			AVDDZ_S[1:0]		AVEEZ_S[1:0]		-
Parameter 3	R/W	VGHZ_CLK[3:0]				VGHZ_CLKB[1:0]		VGHZ_CLKP[1:0]		-
Parameter 4	R/W	VGLZ_CLK[3:0]				VGLZ_CLKB[1:0]		VGLZ_CLKP[1:0]		-
Parameter 5	R/W	MVZ_S_CLK[3:0]				MVZ_S_CLKB[1:0]		MVZ_S_CLKP[1:0]		-
Parameter 6	R/W	MVZ_G_CLK[3:0]				MVZ_G_CLKB[1:0]		MVZ_G_CLKP[1:0]		-
Parameter 7	R/W	NMVZ_D_CLK[3:0]				NMVZ_D_CLKB[1:0]		NMVZ_D_CLKP[1:0]		-
Parameter 8	R/W	MVZ_D_CLK[3:0]				MVZ_D_CLKB[1:0]		MVZ_D_CLKP[1:0]		-

Description

This command is used to set charge pump related setting. Which inlcude pumping frequency and ratio of voltage .

VGHZ_RT: Specify the charge pump ratio of VGHZ.

VGH Z_RT	VGHZ_PAVDD	VGH charge pump
0h	-	2xAVDD
1h	0	2xAVDD + VCI
	1	3xAVDD

Note1: VGHZ_PAVDD (page2,B7h)
Note2 : Internal charge pump (always) :
AVDD=3.0xVCI ; VCL=-1.0xVCI ; AVEE=-2.0xVCI
Note3: VGL charge pump = 4xAVEE

VGLZ_S[3:0]: Set clamping voltage level of VGLZ.

VGLZ _S[3:0]	VGLZ (V)
0h	-7
1h	-7.5
2h	-8.0
:	500mv / step
Ah	-12.0
Bh	-12.5
Ch	-13
Dh~Fh	inhibit

AVDDZ_D_S[3:0]: Set clamping voltage level of AVDDZ_D.

AVDDZ_D_S[2:0]	AVDDZ_D Clamping Voltage	VGH = 3 x AVDD Estimate / sim	
0h	inhibit	21.0	19.87
1h	6.8V	20.4	19.36
2h	6.6V	19.8	18.8
3h	6.4V	19.2	18.23
4h	6.2V	18.6	17.66
5h	6.0V	18.0	17.1
6h	5.8V	17.4	16.54
7h	5.6V	16.8	15.98

AVDDZ_S[1:0]: Set clamping voltage level of AVDDZ.

AVDDZ_S[1:0]	AVDDZ (V)
0h	Inhibit
1h	6.8
2h	6.6
3h	6.4

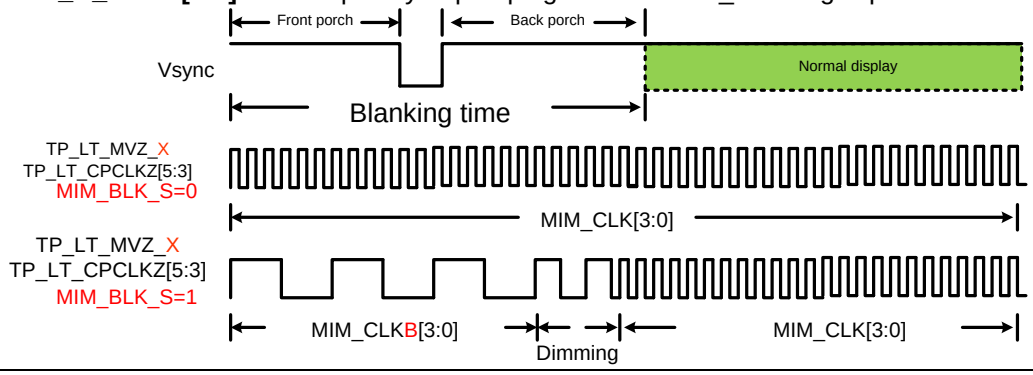
AVEEZ_S[1:0]: Set clamping voltage level of AVEEZ_S.

AVEEZ_S[1:0]	AVEEZ (V)
0h	-5.2
1h	-5.0
2h	-4.8
3h	-4.6

VGHZ_CLK[3:0]: Set frequency of pumping clock of VGHZ under normal mode.
VGLZ_CLK[3:0]: Set frequency of pumping clock of VGLZ under normal mode.
MVZ_S_CLK[3:0]: Set frequency of pumping clock of MVZ_S under normal mode.
MVZ_G_CLK[3:0]: Set frequency of pumping clock of MVZ_G under normal mode.
NMVZ_D_CLK[3:0]: Set frequency of pumping clock of NMVZ_D under normal mode.
MVZ_D_CLK[3:0]: Set frequency of pumping clock of MVZ_D under normal mode.

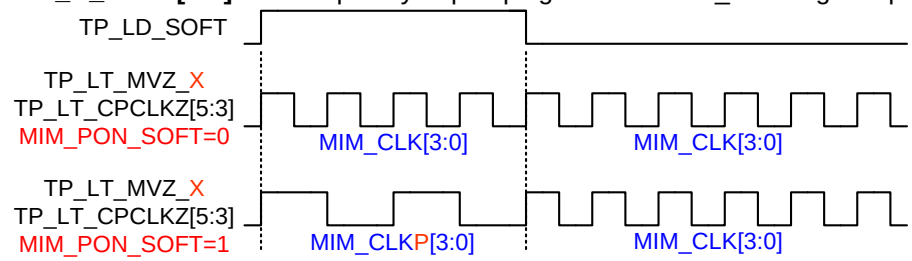
Name (MIM_CLK[3:0])	APR Pin name
MVZ_CLK[3:0]	TP_LT_CPCLKZ_ TP_LT_CPCLKZ_ TP_LT_CPCLKZ_
NMVZ_CLK[3:0]	TP_LT_CPCLKZ_ND
VGLZ_CLK[3:0]	TP_LT_CPCLKZ[3]
VGHZ_CLK[3:0]	TP_LT_CPCLKZ[4]
0h	OSCM_D256
1h	OSCM_D128
2h	OSCM_D64
3h	OSCM_D32
4h	OSCM_D16
5h	OSCM_D8
6h	OSCM_D4
7h	OSCM_D2
8h	OSCM_D768
9h	OSCM_D384
Ah	OSCM_D192
Bh	OSCM_D96
Ch	OSCM_D48
Dh	OSCM_D24
Eh	OSCM_D12
Fh	OSCM_D6

VGHZ_CLKB[1:0]: Set frequency of pumping clock of VGHZ during V-porch.
VGLZ_CLKB[1:0]: Set frequency of pumping clock of VGLZ during V-porch.
MVZ_S_CLKB[1:0]: Set frequency of pumping clock of MVZ_S during V-porch.
MVZ_G_CLKB[1:0]: Set frequency of pumping clock of MVZ_G during V-porch.
NMVZ_D_CLKB[1:0]: Set frequency of pumping clock of NMVZ_D during V-porch.
MVZ_D_CLKB[1:0]: Set frequency of pumping clock of MVZ_D during V-porch.



MIM_CLKB[3:0]	
MVZ_CLK[3:0]	TP_LT_MVZ_S TP_LT_MVZ_G TP_LT_MVZ_D
NMVZ_CLK[3:0]	TP_LT_MVZ_ND
VGLZ_CLKB[3:0]	TP_LT_CPCLKZ[3]
VGHZ_CLKB[3:0]	TP_LT_CPCLKZ[4]
0h	MIM_CLK[3:0] period X1
1h	MIM_CLK[3:0] period X2
2h	MIM_CLK[3:0] period X4
3h	MIM_CLK[3:0] period X8

VGHZ_CLKP[1:0]: Set frequency of pumping clock of VGHZ during soft pump.
VGLZ_CLKP[1:0]: Set frequency of pumping clock of VGLZ during soft pump.
MVZ_S_CLKP[1:0]: Set frequency of pumping clock of MVZ_S during soft pump.
MVZ_G_CLKP[1:0]: Set frequency of pumping clock of MVZ_G during soft pump.
NMVZ_D_CLKP[1:0]: Set frequency of pumping clock of NMVZ_D during soft pump.
MVZ_D_CLKP[1:0]: Set frequency of pumping clock of MVZ_D during soft pump.



MIM_CLKP[3:0]	
MVZ_CLK[3:0]	TP_LT_MVZ_S TP_LT_MVZ_G TP_LT_MVZ_D
NMVZ_CLK[3:0]	TP_LT_MVZ_ND
VGLZ_CLKP[3:0]	TP_LT_CPCLKZ[3]
VGHZ_CLKP[3:0]	TP_LT_CPCLKZ[4]
0h	MIM_CLK[3:0] period X1
1h	MIM_CLK[3:0] period X2
2h	MIM_CLK[3:0] period X4
3h	MIM_CLK[3:0] period X8

Restriction	-

2.4.6. VDDD_CTRL: Control logic voltage setting (Page0 - BCh)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	1	1	0	0	BC
Parameter 1	**R/W**	-	VDDD_S0[2:0]			AVSSN_EN	AVSSN_S[2:0]			-
Parameter 2	**R/W**	-	VDDD_S1[2:0]			VDDD_VCI_EN	VDDD_S2[2:0]			

Description

This command is used to control internal logic voltage setting.

VDDD_VCI_EN: Control VDDD_VCI regualtor On/Off of GAS function. Internal VDDD will generate 1.3V to keep IOVCC voltage when GAS happen.
0: Disable
1: Enable (default)
Note : VDDD_S0 an VDDD_S1 always turn on

VDDD_S0[2:0]: Set VDDD voltage for VDDD_OSC.
VDDD_S1[2:0]: Set VDDD voltage.
VDDD_S2[2:0]: Set VDDD when VDDD_VCI_EN=1.

VDDD_S0[2:0]	VDDD (V)
0h	1.35
1h	1.4
2h	1.45
3h	1.5
4h	1.55
5h	1.6
6h	1.65
7h	1.7

VDDD_S1[2:0]	VDDD (V)
0h	1.35
1h	1.4
2h	1.45
3h	1.5
4h	1.55
5h	1.6
6h	1.65
7h	1.7

VDDD_S2[2:0]	VDDD (V)
0h	1.1
1h	1.15
2h	1.2
3h	1.25
4h	1.3
5h	1.35
6h	1.4
7h	1.45

AVSSN_EN: Enable/disable AVSSN regulator.

<table>
<tr><td></td><td>AVSSN_S[2:0]:Set AVSSN voltage setting.
<table>
<tr><th>AVSSN_S[2:0]</th><th>AVSSN (V)</th></tr>
<tr><td>0h</td><td>1.5</td></tr>
<tr><td>1h</td><td>1.6</td></tr>
<tr><td>2h</td><td>1.7</td></tr>
<tr><td>3h</td><td>1.8</td></tr>
<tr><td>4h</td><td>1.9</td></tr>
<tr><td>5h</td><td>2</td></tr>
<tr><td>6h</td><td>2.1</td></tr>
<tr><td>7h</td><td>2.2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td>-</td></tr>
</table>

2.4.7. SETRGBIF: (Page0 - BDh)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	1	1	0	1	BD
Parameter 1	**R/W**	-	-	BLK_ OTP	DEM	VSPL	HSPL	DEPL	PCPL	-
Parameter 2	**R/W**	-	-	RGB_SEL[1:0]		-	-	RGB_SYNC_L N[9:8]		-
Parameter 3	**R/W**	RGB_SYNC_LN[7:0]								-
Parameter 4	**R/W**	RGB_SYNC_RESO_X[7:0]								-
Parameter 5	**R/W**	RGB_SYNC_VBP[7:0]								-
Parameter 6	**R/W**	RGB_SYNC_HBP[7:0]								-
Description	This command is used to set RGB interface Related Setting. **BLK_OPT:** TBD. **DEM:** chose DE mode 0: external DE (DE mode) 1: internal DE (HV mode) **VSPL:** Indicate the VSYNC active polarity 0: active low 1: active high **HSPL:** Indicate the HSYNC active polarity 0: active low 1: active high **PCPL:** Indicate the PCLK polarity 0: normal 1: reverse PCLK **DEPL:** Indicate the DE polarity 0: normal 1: reverse DE **RGB_SYNC_LN[10:0]:** line setting for internal timing. line = RGB_SYNC_LN[10:0]*2. **RGB_SYNC_RESO_X[7:0]:** pixel setting for internal timing. Pixel/line = RGB_SYNC_RESO_X[7:0]*4 **RGB_SYNC_VBP[7:0]:** VBP setting for internal DE generate. **RGB_SYNC_HBP[7:0]:** HBP setting for internal DE generate.									
Restriction	-									

2.4.8. GAS_CTRL: GAS function control (Page0 - BEh)

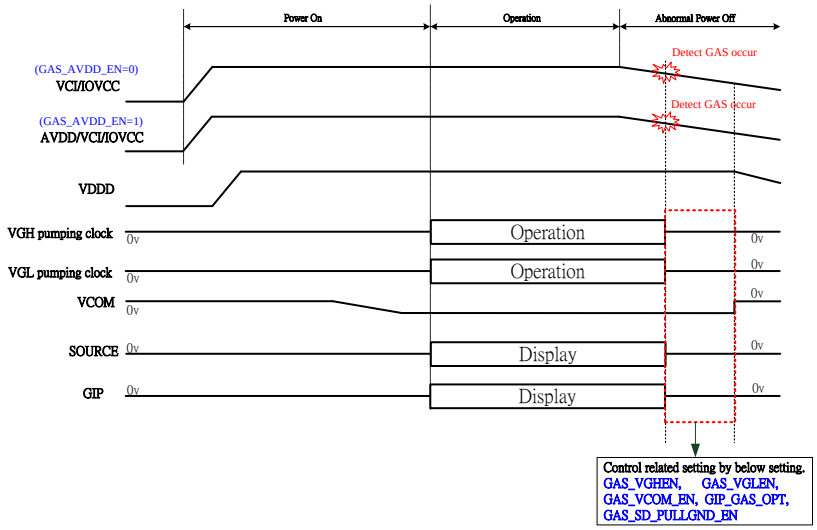
CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	1	1	1	0	BE
Parameter 1	**R/W**	-	-	-	-	-	-	-	-	-
Parameter 2	**R/W**	GAS_SLPIN_EN	GAS_OUT_EN	GAS_VCI_EN	GAS_IOVCC_EN	GAS_BLK_NUM[3:0]				-
Parameter 3	**R/W**	GAS_DBS_SEN	GAS_DBS_GEN	GAS_DBS_LTH[5:0]						-
Parameter 4	**R/W**	-	-	DC_GAS_VGH_EN	DC_GAS_VGL_EN	-	-	DC_GAS_MVZ_EN	DC_GAS_MVZ_EN	-

Description

This command is used to set related setting while abnormal pwoer off cccurs.
GAS_SLPIN_EN: Enable SLPIN function On/Off during GAS occurs.
0: When GAS occurs, DDIC will keep blanking until all power off.
1: When GAS occurs, DDIC will excute SLPIN flow after blanking frame satisfy

GAS_OUT_EN: GAS signal output enable. It means GAS function enable.
GAS_VCI_EN: GAS function enable for VCI. (REG*SleepOut)
GAS_IOVCC_EN: GAS function enable for IOVCC. (REG*SleepOut)

GAS_BLK_NUM[3:0]:GAS sweep white frame number to sleep in.
Sweep white number = GAS_BLK_NUM[3:0]



GAS_DBS_SEN:gas debounce for source tcon enable
GAS_DBS_GEN:gas debounce for gip enable
GAS_DBS_LTH[5:0]:gas debounce counter.
Debounce time = OSC period * 8 * GAS_DBS_LTH[5:0]

DC_GAS_VGH_EN: Enable VGH function at GAS
0: Disable
1: Enable – VGH pumping at GAS
DC_GAS_VGL_EN: Enable VGL function at GAS
0: Disable
1: Enable – VGL pumping at GAS
DC_GAS_MVZ_D_EN: Enable MVZ_D function at GAS
0: Disable
1: Enable – MVZ_D pumping at GAS

Restriction	-

2.4.9. SETSTBA: Set Source Output driving ability (Page0 - C0h)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	0	0	0	0	0	C0
Parameter 1	**R/W**	-	GAP[2:0]			SAP[3:0]				-
Parameter 2	**R/W**	GAP2_EN	GAP2[2:0]			-	-	-	-	

Description

This command is used to set internal OTP program related setting.

GAP2_EN:enable GAP2 setting during idle mode.
GAP[2:0]:Set Gamma OP output driving ability.
GAP2[2:0]:Set Gamma OP output driving ability during idle mode

GAP[2:0]/ GAP2[2:0]	Bias current (uA)
000	4.29
001	7.96
010	11.4
011	14.9
100	18.2
101	21.5
110	24.8
111	28

SAP[3:0]: Set channel OP output driving ability of general pattern.

SAP[3:0]	Bias current (uA)	SAP[3:0]	Bias current (uA)
0000	0.37	1000	3.06
0001	0.72	1001	3.38
0010	1.07	1010	3.71
0011	1.41	1011	4.03
0100	1.74	1100	4.35
0101	2.08	1101	4.67
0110	2.41	1110	4.99
0111	2.74	1111	5.31

Restriction: -

2.4.10.SETPANEL: Set Panel relate register (Page0 - C1h)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	0	0	0	0	1	C1
Parameter 1	**R/W**	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	CFHR	-	-

Description

This command is used to panel related setting.

SS_Panel: Set Source scan output direction.

SS_Panel	S/D scan direction
0	S1 -> S240
1	S240-> S1

GS_Panel: Set Gate scan output direction.

GS_Panel	G/D scan direction
0	Top -> Bottom Scan (G1->G320)
1	Bottom -> Top Scan (G320 -> G1)

Note: Exmaple, resolution is 1080RGB x 1920.

REV_Panel: Set the display of the same data on both normally-white and normally-black panels.

REV_Panel	Panel (Normally-type)
0	Normal Black panel
1	Normal White panel

CFHR: Set color fliter horizontial alignment order.

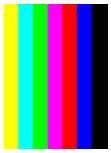
CFHR	Horizontial color fliter alignment
0	<S1><S2> alignment to <R1><G1><B1><R2><G2><B2> alignment
1	<S1><S2> alignment to <B1><G1><R1><B2><G2><R2> alignment

Restriction	-

2.4.11.SET_BIST: BIST Pattern setting (Page0 - C2h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>R/W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>C2</td></tr>
<tr><td>Parameter 1</td><td>R/W</td><td>-</td><td>-</td><td>-</td><td>-</td><td>TEST_
PAT_EN</td><td colspan="3">TEST_PATTERN[2:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set internal BIST pattern selection.

TEST_PAT_EN: Enable BIST Pattern On/Off.
0: Disable (default)
1: Enable

TEST_PATTERN[2:0]: Set which BIST pattern on display.
<table>
<tr><th>TEST_PATTERN[2:0]</th><th>Image</th><th>Description</th></tr>
<tr><td>0</td><td>  </td><td>8 Color</td></tr>
<tr><td>1</td><td>  </td><td>Black</td></tr>
<tr><td>2</td><td>  </td><td>White</td></tr>
<tr><td>3</td><td>  </td><td>Red</td></tr>
<tr><td>4</td><td>  </td><td>Green</td></tr>
<tr><td>5</td><td>  </td><td>Blue</td></tr>
<tr><td>6:</td><td>  </td><td>V256 Gray which is evenly distributed in Y-direction</td></tr>
<tr><td>7</td><td>  </td><td>BGWB2
Outer border : Red；
Inner border : Blue；Inside: Black</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.4.12.SETRGBCYC: Set Display Waveform Cycles of RGB Mode (Page0 - C3h)

CMD_ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	0	0	0	1	1	C3
Parameter 1	**R/W**					IDLE_ TYPE	RGB_INV_NP[2:0]			
Parameter 2	**R/W**		RGB_INV_PI[2:0]				RGB_INV_I[2:0]			
Parameter 3	**R/W**					RGB_GND[3:0]				
Parameter 4	**R/W**				RGB_EQ1[4:0]					
Parameter 5	**R/W**			RGB_CHGEN_ON[5:0]						
Parameter 6	**R/W**	RGB_CHGEN_OFF[7:0]								
Parameter 7	**R/W**	GASHORT_ON[7:0]								
Parameter 8	**R/W**	RGB_OFF[7:0]								
Parameter 9	**R/W**		GAOP OFFEN	GAOPOFF[4:0]						

Description

This command is used to set internal SD output timing.

IDLE_TYPE:
0: (MSB,5'b0)
1: 6'b(MSB)

RGB_INV_NP[2:0]: Set source dot inversion type at normal or partial mode.
RGB_INV_PI[2:0]: Set source dot inversion type at (idle+partial) mode.
RGB_INV_I[2:0]: Set source dot inversion type at idle mode.

RGB_INV_NP[2:0]/ RGB_INV_PI[2:0]/ RGB_INV_I[2:0]	Dot inversion type
000	1-dot
001	1+2-dot
010	2-dot
011	4-dot
100	Column
Others	Inhibit

RGB_GND[3:0]: Set positive source output GND function.

RGB _GND[3:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
:	1 timing clock /step
0Eh	14 timing clock
0Fh	15 timing clock

Note: 1 timing clock = 8 multiple of Fosc.

RGB _EQ1[4:0]: Set negative SD EQ1 time.

RGB _EQ1[4:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
:	1 timing clock /step
1Eh	30 timing clock
1Fh	31 timing clock

Note: 1 timing clock = 8 multiple of Fosc.

RGB _CHGEN_ON[5:0]: Set SD OP output time.

RGB _CHGEN_ON[5:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
:	1 timing clock /step
3Eh	62 timing clock
3Fh	63 timing clock

Note: 1 timing clock = 8 multiple of Fosc.

RGB _CHGEN_OFF[7:0]: Set SD OP output time.

RGB _CHGEN_OFF[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

GASHORT_ON[7:0]: Set Gamma short output time.

GASHORE_ON[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

RGB _OFF[7:0]: Set SD data output time.

RGB _OFF[7:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
:	1 timing clock /step
FEh	254 timing clock
FFh	255 timing clock

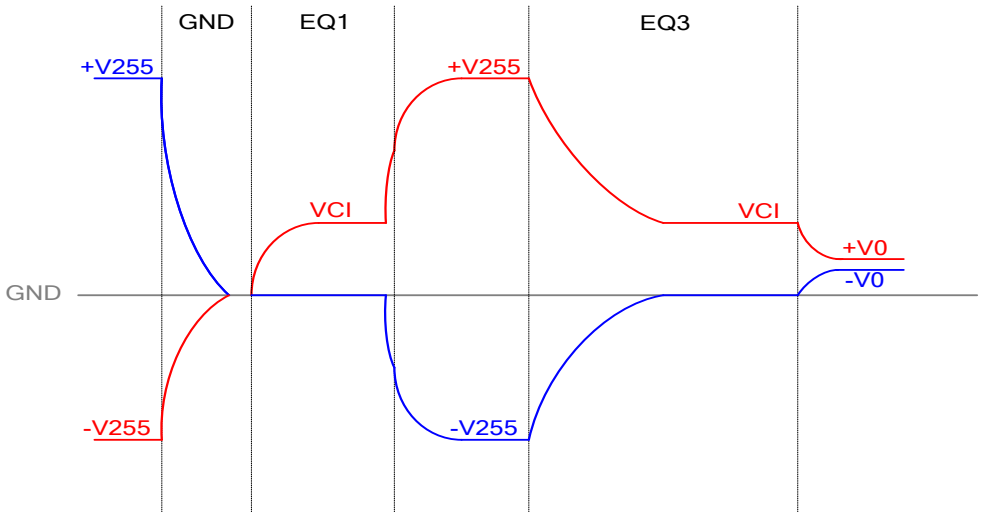
Note: 1 timing clock = 4 multiple of Fosc.

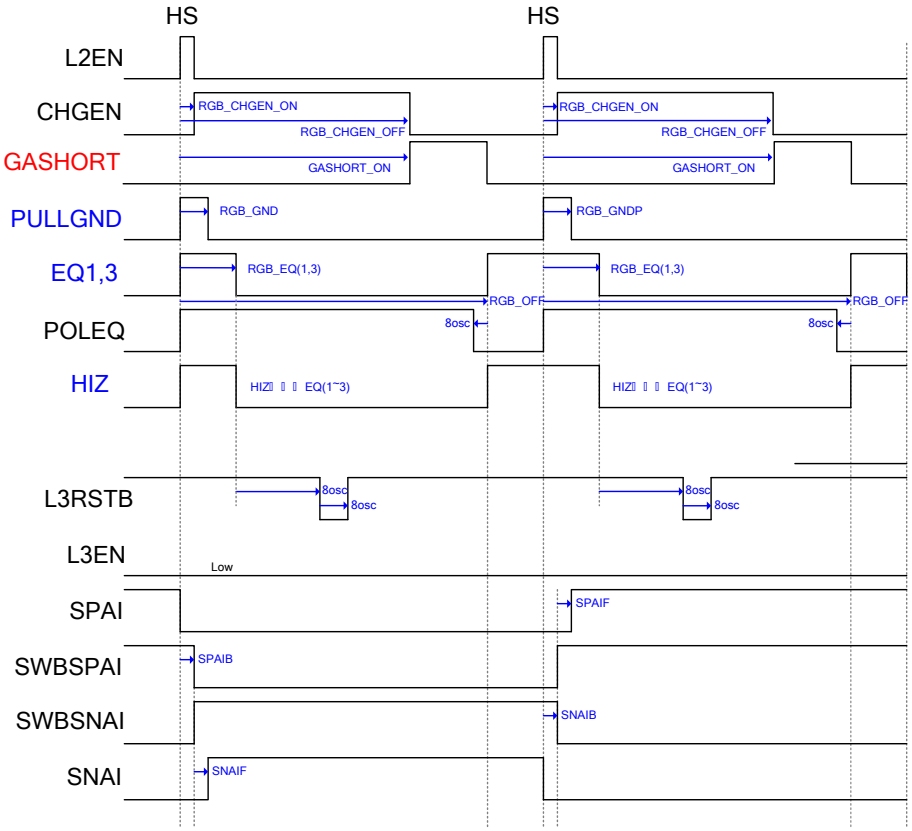
GAOPOFFEN:
1:Enable
0:Disable(GAOPOFF keeps low)

GAOPOFF [4:0]: Set GAMMA OP OFF time.

GAOPOFF[4:0]	Clock cycle
00h	0 timing clock
01h	1 timing clock
:	1 timing clock /step
1Eh	30 timing clock
1Fh	31 timing clock

Note: 1 timing clock = 8 multiple of Fosc.





Note:

1. L2EN high pulse needs to be covered by PULLGND high pulse when changing polarity.
2. If sets RGB_EQ*=00, EQ pulse will keep low.

Restriction	-

2.4.13.SET TCON: Timing control setting (Page0 - C4h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	R/W	1	1	0	0	0	1	0	0	C4
Parameter 1	R/W	-	-	LN[9:8]		-	-	-	-	-
Parameter 2	R/W	LN[7:0]								-
Parameter 3	R/W	SLT_NP[7:0]								-
Parameter 4	R/W	VFP_NP[7:0]								-
Parameter 5	R/W	VBP_NP[7:0]								-
Parameter 6	R/W	HBP_NP[7:0]								-
Parameter 3	R/W	SLT_I[7:0]								-
Parameter 4	R/W	VFP_I[7:0]								-
Parameter 5	R/W	VBP_I[7:0]								-
Parameter 6	R/W	HBP_I[7:0]								-
Parameter 3	R/W	SLT_PI[7:0]								-
Parameter 4	R/W	VFP_PI [7:0]								-
Parameter 5	R/W	VBP_PI [7:0]								-
Parameter 6	R/W	HBP_PI [7:0]								-
Parameter 7	R/W	HBP_NCK[3:0]				HFP_NCK[3:0]				-
Parameter 8	R/W	TCON_OPT1[15:8]								-
Parameter 9	R/W	TCON_OPT1[7:0]								-

Description

This command is used to set timing control.

LN[9:0]: Sets the gate line number to drive LCD panel. The number of lines must be equal or more than the gate line number of LCD panel. Gate line number = LN*2.

LN[9:0]										Gate Line
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	2
-	-	-	-	-	-	-	-	-	-	2 line / step
0	1	1	1	1	0	0	0	0	0	960
-	-	-	-	-	-	-	-	-	-	2 line / step
1	1	1	1	1	1	1	1	1	0	2044
1	1	1	1	1	1	1	1	1	1	2046

XXX_NP[7:0]: for normal+partial mode
XXX_I[7:0]: for idle mode
XXX_PI[7:0]: for partial +idle mode

SLT_xx[7:0]: Sets the scan line time width. (4 x OSC) CLK / step

STL_xx[7:0]								Scan Line time(OSC CLK)
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	(4x OSC) CLK
0	0	0	0	0	0	1	0	(8 x OSC) CLK
-	-	-	-	-	-	-	-	(4 x OSC) CLK / step
1	0	0	1	0	0	0	1	(580x OSC) CLK
1	0	0	1	0	0	1	0	(584 x OSC) CLK
-	-	-	-	-	-	-	-	(4 x OSC) CLK / step
1	1	1	1	1	1	0	1	(1012 x OSC) CLK
1	1	1	1	1	1	1	0	(1016 x OSC) CLK
1	1	1	1	1	1	1	1	(1020 x OSC) CLK

Note: fosc = 10MHz.

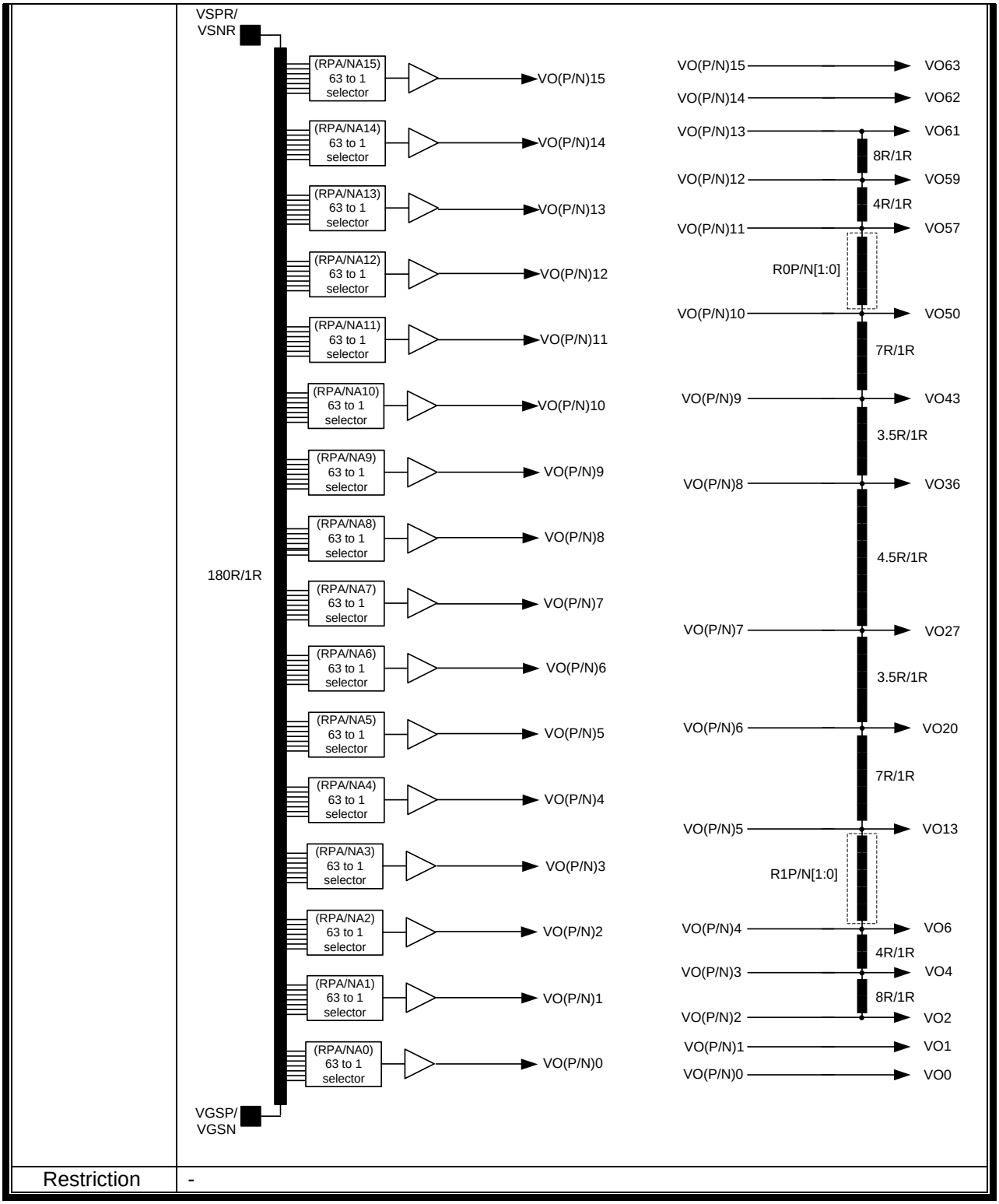
VBP_xx[7:0]: Vertical back porch number setting.
VFP_xx[7:0]: Vertical front porch number setting.
HBP_xx[7:0]: Horizontal back porch number setting.(for DPI sync mode)

VBP_xx[7:0] / VFP_xx[7:0]/HBP_xx[7:0]	Number of VBP / VFP/HBP(line)
8h'00	Inhibit
8h'01	1
8h'02	2

	: 8h'FB 8h'FC 8h'FD 8h'FE 8h'FF	: 251 252 253 254 255
	Note: VBP = External (VS + VBP) -1 line. VFP = External VFP line. **HFP_NCK[3:0]:** Defined the number of HFP in the internal time. **HBP_NCK[3:0]:** Defined the number of HBP in the internal time. **TCON_OPT1[15:0]:** Internal used.	
Restriction	-	

2.4.14.SET_R_GAMMA: Set Red Gamma output voltage(Page0 - C8h)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	0	1	0	0	0	C8
Parameter 1	**R/W**	-	RPA15[5:0]							-
Parameter 2	**R/W**	-	RPA14[5:0]							-
Parameter 3	**R/W**	-	RPA13[5:0]							-
Parameter 4	**R/W**	-	RPA12[5:0]							-
Parameter 5	**R/W**	-	RPA11[5:0]							-
Parameter 6	**R/W**	-	RPA10[5:0]							-
Parameter 7	**R/W**	-	RPA9[5:0]							-
Parameter 8	**R/W**	-	RPA8[5:0]							-
Parameter 9	**R/W**	-	RPA7[5:0]							-
Parameter 10	**R/W**	-	RPA6[5:0]							-
Parameter 11	**R/W**	-	RPA5[5:0]							-
Parameter 12	**R/W**	-	RPA4[5:0]							-
Parameter 13	**R/W**	-	RPA3[5:0]							-
Parameter 14	**R/W**	-	RPA2[5:0]							-
Parameter 15	**R/W**	-	RPA1[5:0]							-
Parameter 16	**R/W**	-	RPA0[5:0]							-
Parameter 17	**R/W**	-	RNA15[5:0]							-
Parameter 18	**R/W**	-	RNA14[5:0]							-
Parameter 19	**R/W**	-	RNA13[5:0]							-
Parameter 20	**R/W**	-	RNA12[5:0]							-
Parameter 21	**R/W**	-	RNA11[5:0]							-
Parameter 22	**R/W**	-	RNA10[5:0]							-
Parameter 23	**R/W**	-	RNA9[5:0]							-
Parameter 24	**R/W**	-	RNA8[5:0]							-
Parameter 25	**R/W**	-	RNA7[5:0]							-
Parameter 26	**R/W**	-	RNA6[5:0]							-
Parameter 27	**R/W**	-	RNA5[5:0]							-
Parameter 28	**R/W**	-	RNA4[5:0]							-
Parameter 29	**R/W**	-	RNA3[5:0]							-
Parameter 30	**R/W**	-	RNA2[5:0]							-
Parameter 31	**R/W**	-	RNA1[5:0]							-
Parameter 32	**R/W**	-	RNA0[5:0]							-
Description	This command is used to set postive /neagative volatge of source output.									



Restriction	-

2.4.15.SET_GD: SET Gate Function (Page0-D0h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	1	0	0	0	0	D0
Parameter 1	**R/W**	-	-	-	-	-	GD_GAS_GATE_CLK	-	GD_LRSW	-
Parameter 2	**R/W**	-	-	GD_ON[5:0]						-
Parameter 3	**R/W**	GD_OFF[7:0]								-
Parameter 4	**R/W**	-	-	GD_EQ_PTR0[5:0]						-
Parameter 5	**R/W**	-	-	-	GD_PTGISC	GD_ISC[3:0]				-

Description

This command sets GIP CGOUTx_L signal mapping when XOR(GS_Panel, GS)=0.

GD_GAS_GATE_CLK

// 0: not gating clock in gas (default)

// 1: gating clock in gas

GD_LRSW

gate driver L/R switch

// 0: gate driver L (default)

// 1: gate driver R

GD_ON[5:0]

gate driver on (Time unit = osc*4)

GD_OFF[7:0]

gate driver off (Time unit = osc*4)

GD_EQ_PTR0[5:0]

gate driver EQ0 pulse width(Time unit = osc*4)

EQ0 end point = gate driver on + EQ0 pulse wodth

GD_EQ_PTR1[7:0]

gate driver EQ1 pulse width(Time unit = osc*4)

EQ1 start point = gate driver off - EQ1 pulse wodth

GD_PTGISC

frame refresh GD enable

// 0: frame refresh GD disable (default)

// 1: frame refresh GD enable

	GD_ISC[3:0]: frame refresh cycle

Hex	Frame refresh cycle
00h	Normal scan
01h	Every 3 cycles scan 1 time
02h	Every 5 cycles scan 1 time
03h	Every 7 cycles scan 1 time
04h	Every 9 cycles scan 1 time
05h	Every 11 cycles scan 1 time
06h	Every 13 cycles scan 1 time
07h	Every 15 cycles scan 1 time
08h	Every 17 cycles scan 1 time
09h	Every 19 cycles scan 1 time
0Ah	Every 21 cycles scan 1 time
0Bh	Every 23 cycles scan 1 time
0Ch	Every 25 cycles scan 1 time
0Dh	Every 27 cycles scan 1 time
0Eh	Every 29 cycles scan 1 time
0Fh	Every 31 cycles scan 1 time

Restriction	-

2.4.16.RAMCTRL (Page0 - D7h)

CMD/Pas	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	1	0	1	1	1	D7
Parameter 1	**R/W**	-	-	SPI_2LAN_EN	RP	RM	-	DM[1:0]		-
Parameter 2	**R/W**	SCL_PL	EXT_VS_PL	EPF[1:0]		ENDIAN	-	MDT[1:0]		-

Description

This command is use to set interface related setting.

SPI_2LAN_EN: Enable SPI 2 data lane when IM[3:0]=0101.

RP : Enable DPI data path.
0:disble
1:enable

RM : select data path for GRAM
1:data from DPI/DSI
0:data from 2C/3C command

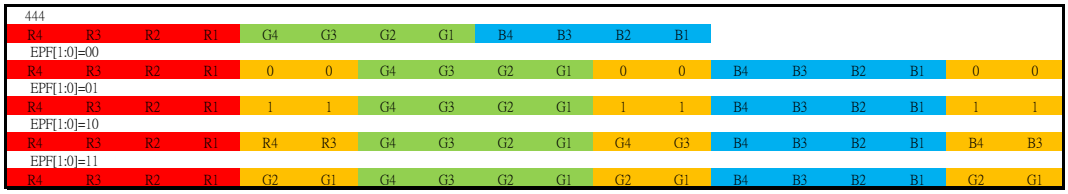
DM[1:0]: select contol timing and display data path

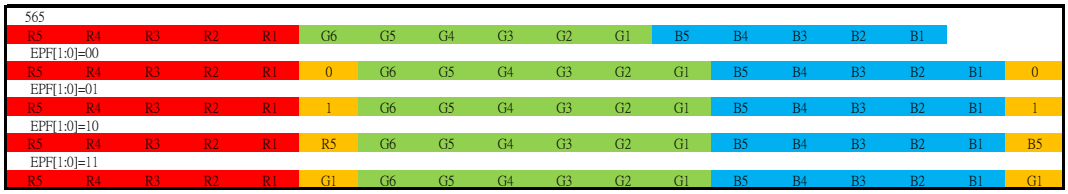
DM[1:0]	Control Timing	Display Data Path
00	internal vs, hs ,de	GRAM
10	external vs(video vs)	GRAM
11	external vs ,hs, de(video mode)	DPI/DSI

SCL_PL: Indicate the HSYNC active polarity
0:normal
1:reverse PCLK

EXT_VS_PL: Indicate the HSYNC active polarity
0:active
1:active

EPF[1:0]: 12/16bits to 18 bits data mapping





ENDIAN: only for 8/9bit DBIB in 565
0:normal(MSB first)
1:little Endian(LSB first)

MDT[1:0]: select display data mapping for parallel interface.

Restriction	-

2.4.17.AUTO_DISP_SETTING (Page0 - D8h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>R/W</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>D8</td></tr>
<tr><td>Parameter 1</td><td>R/W</td><td>-</td><td>-</td><td>-</td><td>-</td><td>GON</td><td>DTE</td><td colspan="2">DISP[1:0]</td><td>-</td></tr>
<tr><td>Parameter 2</td><td>R/W</td><td>-</td><td>-</td><td colspan="2">DISP_SW_OPT [1:0]</td><td>-</td><td>BLK_DISABLE</td><td colspan="2">BLK_MODE [1:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">
This command is used to set display sequence Related Setting.
DISP[1:0]: Source output setting.
<table>
<tr><th>DISP1</th><th>DISP0</th><th>Internal Display Operations</th><th>Source Output</th></tr>
<tr><td>0</td><td>0</td><td>Halt</td><td>VSSD</td></tr>
<tr><td>0</td><td>1</td><td>Inhibit</td><td>Inhibit</td></tr>
<tr><td>1</td><td>0</td><td>Operate</td><td>V255</td></tr>
<tr><td>1</td><td>1</td><td>Operate</td><td>Display</td></tr>
</table>
DTE, GON: Gate / SD output setting.
<table>
<tr><th>GON</th><th>Gate Output</th></tr>
<tr><td>0</td><td>VGL</td></tr>
<tr><td>1</td><td>VGH/VGL</td></tr>
</table>
<table>
<tr><th>DTE</th><th>SD Output</th></tr>
<tr><td>0</td><td>Off (Hi-Z)</td></tr>
<tr><td>1</td><td>ON</td></tr>
</table>
BLK_DISABLE: Control blanking frame is displayed after SLPOUT/SLPIN.
1: No blanking frame is displayed.
0: 2blanking frame are displayed. (default)

BLK_MODE[1:0]: When BLK_DISABLE=0,
<table>
<tr><th>BLK_MODE [1:0]</th><th>Blank mode</th></tr>
<tr><td>00</td><td>Turn off blanking after 2 blanking frame</td></tr>
<tr><td>01</td><td>Keep blanking after 2 blanking frames</td></tr>
<tr><td>Others</td><td>Inhibit</td></tr>
</table>
DISP_SW_OPT[1:0]: Define status of DISP[1:0] after SW reset command receivered.
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.4.18.OTP_PROG: OTP Program (Page0 - D9h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	1	1	0	0	1	D9
Parameter 1	**R/W**	OTP_MASK[7:0]								-
Parameter 2	**R/W**	-	-	-	-	-	-	OTP_INDEX[9:8]		-
Parameter 3	**R/W**	OTP_INDEX[7:0]								-
Parameter 4	**R/W**	OTP_PROGRAM_ALL	OTP_TWOBITS_SEL	OTP_PGM_SEL	OTP_READ_SINGLE	OTP_WRITE_SINGLE	OTP_LOAD_DISABLE	OTP_INT_VPP	OTP_AUTO_PROG	-
Parameter 5	**R**	OTP_RDATA[7:0]								-
Parameter 6	**R/W**	OTP_WDATA[7:0]								-

Description

OTP_MASK[7:0]: Bit programming mask, if 1, means this bit can't be programmed.
OTP_INDEX[9:0] : Set index of OTP table for programming.
OTP_PGM_SEL:
OTP_INT_VPP: Select VPP voltage from external or internal.
0: VPP voltage from external power supply. (VPP pad) (default)
1: VPP voltage from internal power supply (VGH).

OTP_INT_VPP	OTP_PGM_SEL	VPP Voltage source	OTP program bit number
1	0	Internal(VGH)	1 bit
0	1	External(VPP pad)	1 bit

Note: OTP progrma bit number will affect total progrma time. (1Byte: Fastest, 1bit: slowest)

OTP_ READ_SINGLE: Read 1 byte OTP value.
0: Disable. (default)
1: Enable.
EX: set INDEX[9:0], READ_SINGLE=1 and AUTO_PROG=1, then read OTP_RDATA[7:0]

OTP_LOAD_DISABLE: Auto reload OTP value.
0: Enable auto reload OTP value after SLPOUT command send. (default)
1: Disable auto reload OTP value after SLPOUT command send.

OTP_AUTO_PROG: When set to 1, the register content of OTP index is programmed.

OTP_WRITE_SINGLE: For 1 byte OTP programing only.(Not release to customer)
0: Disable. (default)
1: Enable.
EX: set MASK[7:0], INDEX[9:0] ,WDATA[7:0] and WRITE_SINGLE=1 first then set AUTO_PROG=1, the WDATA will write to INDEX.

OTP_ RDATA[7:0]: Read back the OTP index data. (Not release to customer)
OTP_WDATA[7:0]: Set OTP data for programming when OTP_WRITE_SINGLE=1.

Restriction: -

2.4.19.SET_WD: Setup watch dog (Page0 - DDh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>R/W</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>DD</td></tr>
<tr><td>Parameter 1</td><td>R/W</td><td>-</td><td>WD_
off</td><td colspan="2">WD_MODE[1:0]</td><td>FBLK_
EN</td><td colspan="3">WD_CLK_SEL[2:0]</td><td>-</td></tr>
<tr><td>Parameter 2</td><td>R/W</td><td colspan="8">WD_Timer[7:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">
WD_MODE[1:0]: Watch dog mode select.
<table>
<tr><th colspan="2">WD_MODE[1:0]</th><th>WD Alarm start</th><th>WD Alarm stop</th></tr>
<tr><td>0</td><td>0</td><td>Inhibit</td><td>Inhibit</td></tr>
<tr><td>0</td><td>1</td><td>Inhibit</td><td>Inhibit</td></tr>
<tr><td>1</td><td>0</td><td>Display off</td><td>Display on</td></tr>
<tr><td>1</td><td>1</td><td>Inhibit</td><td>Inhibit</td></tr>
</table>
WD_off: Control watch dog function on/off while externl video singal was disappear.
0: Enable watch dog function. (default)
1: Disable watch dog function.

WD_CLK_SEL[2:0]: Set base clock frequency of watch dog.
<table>
<tr><th>WD_CLK_SEL[2:0]</th><th>WDosc (us)</th></tr>
<tr><td>000</td><td>0.5us</td></tr>
<tr><td>001</td><td>1us</td></tr>
<tr><td>010</td><td>2us</td></tr>
<tr><td>011</td><td>4us</td></tr>
<tr><td>100</td><td>8us</td></tr>
</table>
WD_Timer[7:0]: Set watch dog timer. When external HSYNC stop, watch dog timer start to count. Send alarm signal to watch dog if timer counting value is the same as WD_Timer[7:0] setting. When HSYNC resume, alarm signal is stoped.
<table>
<tr><th>WD_Timer[7:0]</th><th>Time to alarm (ms)</th></tr>
<tr><td>0x00</td><td>0 x WDosc(Inhibit)</td></tr>
<tr><td>0x01</td><td>1 x WDosc</td></tr>
<tr><td>…</td><td>1 WDosc / step</td></tr>
<tr><td>0xFE</td><td>254 x WDosc</td></tr>
<tr><td>0xFF</td><td>255 x WDosc</td></tr>
</table>
Total duration to activate WD_Alarm = WD_TIMER[7:0]*Time Unit*4
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.4.20.SET_PAGE(Page0 - DEh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	1	1	1	1	0	DE
Parameter 1	**R/W**	-					PAGE[2:0]			-
Description	This command is used to change page. **PAGE[2:0]:** Register page select.									
Restriction	-									

2.4.21.SET_PASSWD: (Page0 - DFh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	1	0	1	1	1	1	1	DF
Parameter 1	**R/W**	PASSWD1[7:0]								-
Parameter 2	**R/W**	PASSWD2[7:0]								-
Parameter 3	**R/W**	PASSWD3[7:0]								-
Description	This command is used to set password to access inhouse register. Normal mode:									
Restriction	-									

{PASSWD1, PASSWD2, PASSWD3}	Description
{98h, 51h, E9h}	Standard & All inhouse CMD access
{5Ah, A5h, FFh}	Enable STD CMD and P0, P1 Registers
{09h, B1h, 7Fh}	Enter ESD protection mode
Others	Standard CMD access (default)

2.4.22.UP_START_CTRL: Micro process control (Page0 - E8h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>R/W</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>E8</td></tr>
<tr><td>Parameter 1</td><td>R/W</td><td colspan="8">UP_KEY1[7:0]</td><td>-</td></tr>
<tr><td>Parameter 2</td><td>R/W</td><td colspan="8">UP_KEY2[7:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">UP_KEY1/UP_KEY2[7:0]: This command is used to enter OTP program mode.
Before OTP programming, setting UP_KEY1=5Ah and UP_KEY2=A5h first. Otherwise OTP programming will fail.
<table>
<tr><td>UP_KEY1[7:0]</td><td>UP_KEY2[7:0]</td><td>Description</td><td>Mode</td></tr>
<tr><td>0x5Ah</td><td>0xA5h</td><td>Enter OTP program mode</td><td>1</td></tr>
<tr><td>0x00h</td><td>0x00h</td><td>Leave OTP program mode</td><td>1</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.4.23.SETID: Set ID (Page0 - E9h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>R/W</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>E9</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Parameter 2</td><td>R/W</td><td colspan="8">ID1[7:0]</td><td>-</td></tr>
<tr><td>Parameter 3</td><td>R/W</td><td colspan="8">ID2[7:0]</td><td>-</td></tr>
<tr><td>Parameter 4</td><td>R/W</td><td colspan="8">ID3[7:0]</td><td>-</td></tr>
<tr><td>Parameter 5</td><td>R/W</td><td colspan="8">ID4[7:0]</td><td>-</td></tr>
<tr><td>Parameter 6</td><td>R</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td><td>ID_OTP_
TIMES[1:0]</td><td></td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">ID1[7:0]: This is used to set ID1 and read value from DAh.
ID2[7:0]: This is used to set ID2 and read value from DBh.
ID3[7:0]: This is used to set ID3 and read value from DCh.
ID4[7:0]: This is used to set ID4.
ID_OTP_TIMES [1:0]: Read the OTP program times of ID. (Not release to customer)
0: No valid SETID in OTP, use register default value.
1: SETID is programmed once in OTP. Reload 1st valid one.
2: SETID is programmed 2 times in OTP. Reload 2th valid one.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

2.5. Jadard page 1 command Description

2.5.1. PWM CTRL: PWM Control (Page1-B5h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	R/W	1	0	1	1	0	1	0	1	B5
Parameter 1	R/W	-	-	-	LE_LED ON_EN	LE_LED ON_ POL	-	LE_LED PWM_ POL	LE_LED _VOL	
Parameter 2	R/W	-	-	LE_PWM _SYNC2 VS	LE_DD_ RST	-	LE_PWM_DUTY_PCN[2:0]			
Parameter 3	R/W	LE_SEL_CLK_DIV[7:0]								
Parameter 4	R/W	LE_N_VAL[7:0]								

Description

LE_LED_VOL: The voltage level for LEDON and LE_LEDPWM pins

LE_LEDPWM_POL: Active polarity for LEDPWM pin.

LE_LEDON_EN: On/Off control for LEDON pin.

LE_LEDON_POL: Active polarity for LEDON pin.

LEDON_EN	LEDON_POL	Status of LEDON Pin
0	0	Keep “high”
0	1	Keep “low”
1	0	Keep “low”
1	1	Keep “high”

PWM_SYNC2VS: PWM sync control.

1: Sync to Vsync.

0: Not sync.

SEL_CLK_DIV[7:0] : PWM clock select.

SEL_CLK_DIV[7:0]	PWM Clock
0x01	OSC / 1
0x02	OSC / 2
:	:
0x40	OSC / 64
0x80	OSC / 128

N_VAL[7:0]: PWM Frequency output.

OSC default is 10 MHz.

$$\mathrm{PWM_f} = \frac{\mathrm{OSC}}{(2\text{^}\mathrm{PS}) \times (\mathrm{N\_VAL}[7:0] + 1) \times \mathrm{SEL\_CLK\_DIV}[7:0]}$$

LE_PWM_DUTY_PCN[2:0]: Real pwm output resolution from 10bit~3bit.

LE_PWM_DUT Y_PCN[2:0](P)	pwm resolution (PS)
3‘h0	2^10 = 1024
3’h1	2^9=512
3’h2	2^8=256

	<table><tr><td>3’h3</td><td>2^7=128</td></tr><tr><td>3’h4</td><td>2^6=64</td></tr><tr><td>3’h5</td><td>2^5=32</td></tr><tr><td>3’h6</td><td>2^4=16</td></tr><tr><td>3’h7</td><td>2^3=8</td></tr></table> **LE_EN_EXT_EN:** extend LE_en when LE off until content dimming finish. **LE_DD_RST:** 0: DD 為0，old_tar_val = tar_val 1: DD 為0，old_tar_val = 0 **LE_NONNORM_DD_EN:** first non_normal(idle/scroll/partial) disp frame backlight dimming or not. 0: dimming off 1: dimming on
Restriction	-

2.6. Jadard page 2 command Description

2.6.1. DCDC_SET : DCDC setting (Page2 – B8h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**R/W**	1	0	1	1	1	0	0	0	B8
Parameter 1	**R/W**	-	VCL_S	VCIP2X_S[1:0]		VGHZ_OV_PAVDD	AVDDZ_D_OV_S[2:0]			-
Parameter 2	**R/W**	EQ2_EN	-	DCDC_EQ2[5:0]						
Parameter 3	**R/W**	EQ3_EN	-	DCDC_EQ3[5:0]						
Parameter 4	**R/W**	-	-	DCDC_GOV_S[5:0]						
Parameter 5	**R/W**	-	-	DCDC_GOV_E[5:0]						

Description

This command is used to set DCDC setting.

VCL_S :

VCL_S	AVEE Clamping Voltage
0h	2.8V
1h	3.0V

VCIP2X_S [1:0] :

VCIP2X_S[1:0]	AVDD Clamping Voltage
0h	5.2V
1h	5.0V
2h	4.8V
3h	4.6V

VGHZ_OV_PAVDD :

0: Disable VGH over-driving at GOV period

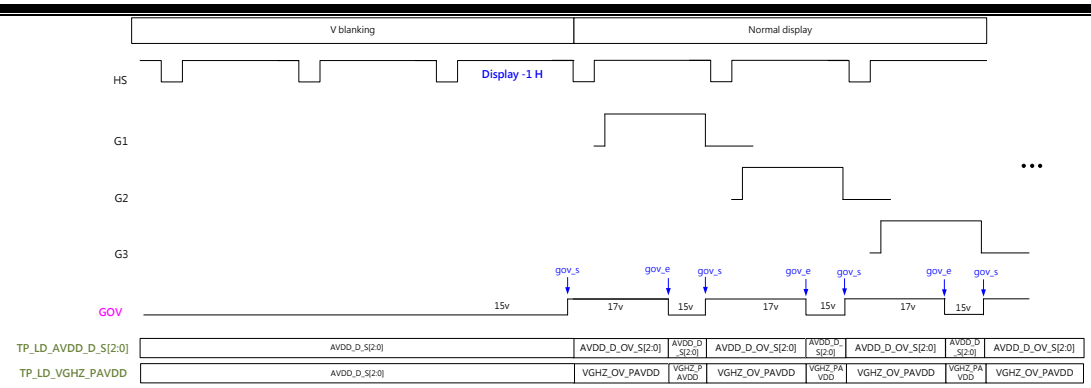
1: Enable VGH over-driving at GOV period

AVDDZ_D_OV_S[2:0] :

AVDDZ_D_S[2:0]/ AVDDZ_D_OV_S [2:0]	AVDDZ_D Clamping Voltage	VGH = 3 x AVDD Estimate / sim		AVDDZ_D_T[2:0]	AVDDZ_D Clamping Voltage
0h	inhibit	21.0	19.87	0h	+0.6v
1h	6.8V	20.4	19.36	1h	+0.4V
2h	6.6V	19.8	18.8	2h	+0.2V
3h	6.4V	19.2	18.23	3h	+0V
4h	6.2V	18.6	17.66	4h	-0.2v
5h	6.0V	18.0	17.1	5h	-0.4v
6h	5.8V	17.4	16.54	6h	-0.6v
7h	5.6V	16.8	15.98	7h	-0.8v

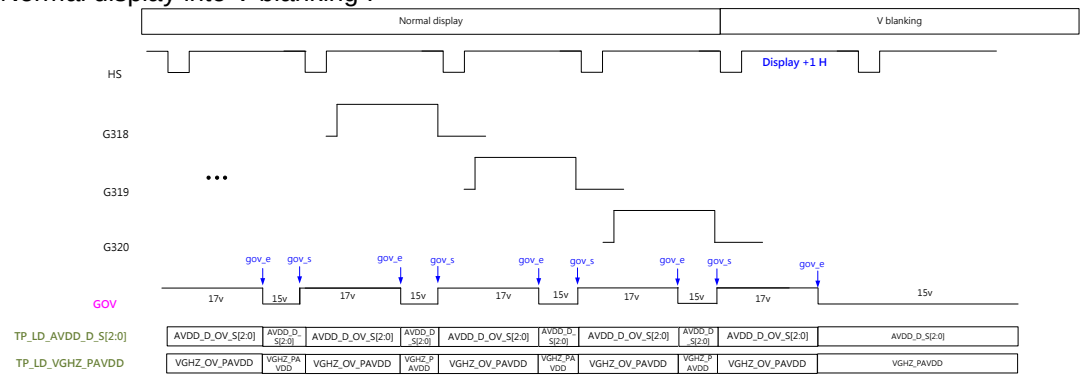
Note :

V blanking into normal display :



GOV off : set : gov_s=gov_e
Power on, default , blanking, non-display area → AVDD_D_S [2:0]
GOV start @ Display -1 H

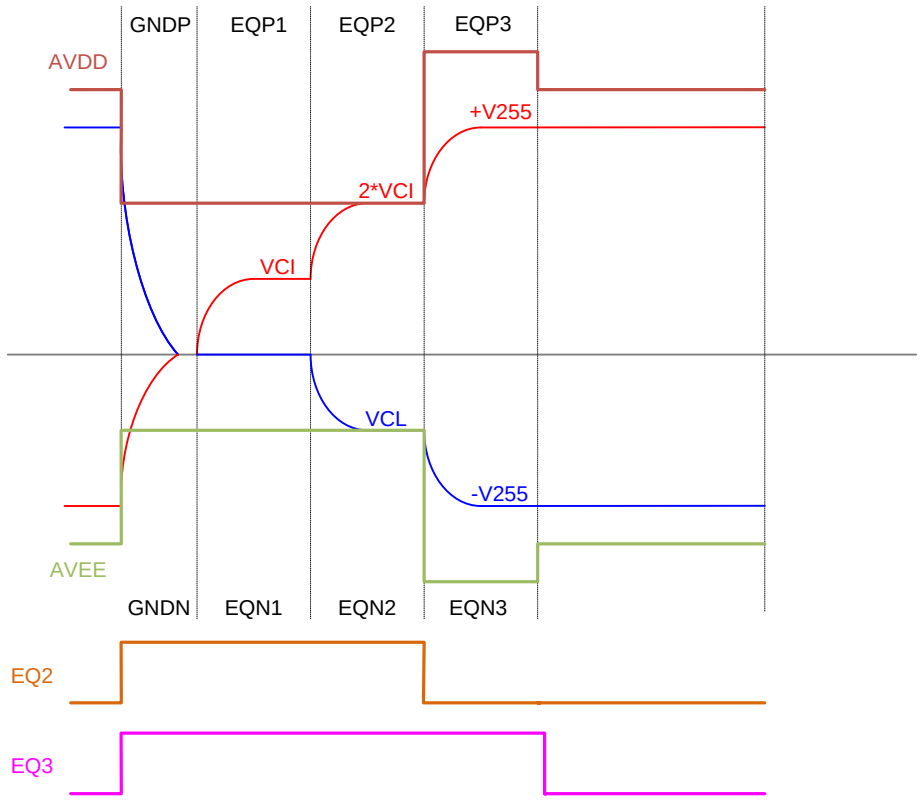
Normal display into V blanking :



GOV end @ Display +1 H

EQ2_EN : Set DCDC EQ2 timing enable
EQ3_EN : Set DCDC EQ3 timing enable
DCDC_EQ2[5:0] : Set DCDC EQ2 timing
DCDC_EQ3[5:0] : Set DCDC EQ3 timing

Note :
EQP1: +V0→VCI; EQN1:-V0→GND.
EQP2/EQN2 : AVDD=VCIP2X ; AVEE=VCL
EQP3/EQN3 : AVDD=7.2V ; AVEE=-5.4V (Over driver range)



換極性 : EQ2/EQ3 on
Blanking : EQ2 on
Sweep white/black : EQ2/EQ3 off

	EQ2	EQ3
BIT	6	6
Number	0-64	0-64
Time step	OSC/8	OSC/8
Period	0~51us	0~51us

DCDC_GOV_S[5:0] : Set GOV_S timing
DCDC_GOV_E[5:0] : Set GOV_E timing

	gov_s	gov_e
BIT	6	6
Number	0-64	0-64
Time step	OSC/8	OSC/8
Period	0~51us	0~51us

Restriction	-

2.6.2. SETRGBCYC2: Set RGB IF source switch control timing (Page2 - C1h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	R/W	1	1	0	0	0	0	0	1	C1
Parameter 1	R/W	-	SDPRDUM	SDDUM[1:0]		SDSW[1:0]		SDPORCH[1:0]		-
Parameter 2	R/W	RGB_SPAIF[3:0]				RGB_SPAIB[3:0]				-
Parameter 3	R/W	RGB_SNAIF[3:0]				RGB_SNAIB[3:0]				-
Parameter 4	R/W	-	-	SDSW_GAS[1:0]		-	-	SDPARTIAL[1:0]		-

Description

This command is used to set SD relaetd control timing.

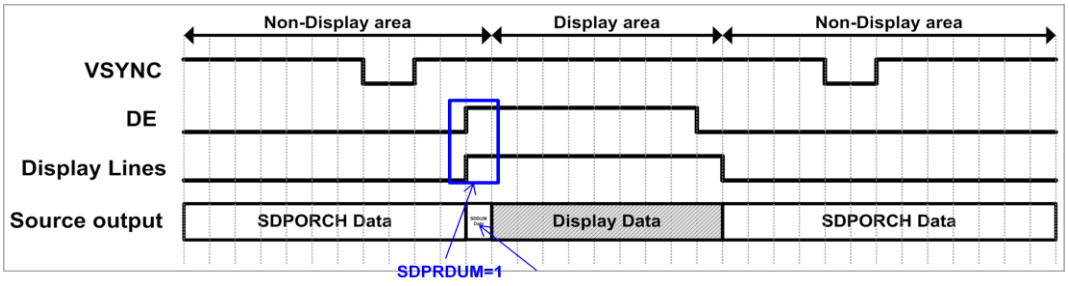
SDPORCH[1:0]: Set SD output at blanking area.
SDSW[1:0]: Set SD output at sweep white case.
SDSW_GAS[1:0]: Set SD output during abnormal power off.
SDPARTIAL[1:0]: Set SD output for partial display.

SDPORCH[1:0]/ SDSW [1:0]/ SDSW_GAS [1:0]/ SDPARTIAL[1:0]	SD Output
00	PullGND
01	V0
10	V255
11	Hi-Z

SDPRDUM: Enable SD pre-dummy line function.
0:indicates normal display lines
1:indicates add one dummy display lines

SDDUM[1:0]: Set SD output at dummy display line.

SDDUM[1:0]	SD Output
00	PullGND
01	V0
10	V255
11	EQ Level

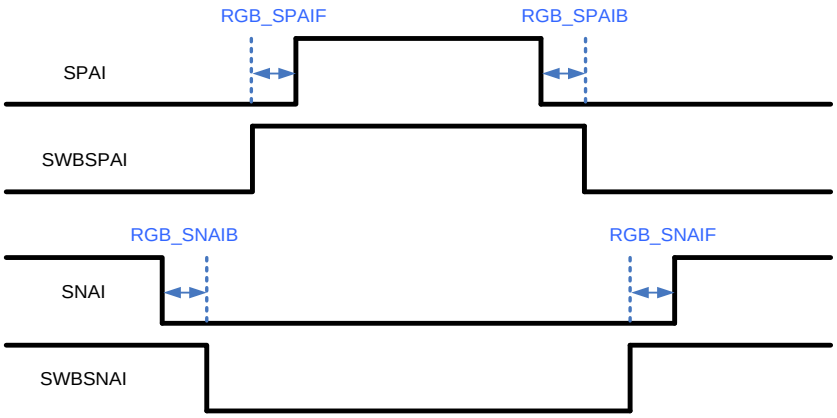


Below parameters are setting shift time between SWBSPAI / SWBSNAI and SPAI / SNAI for channel OP polarity control timing.

RGB_SPAIF[3:0]: Set rising edge delay time of SPA to SWBSPAI rising edge.
RGB_SPAIB[3:0]: Set falling edge shift time of SPA to SWBSPAI falling edge.
RGB_SNAIF[3:0]: Set rising edge shift time of SNA to SWBSNAI rising edge.
RGB_SNAIB[3:0]: Set falling edge delay time of SNA to SWBSNAI falling edge.

RGB_SPAIF [7:0]	RGB_SPAIB [7:0]	RGB_SNAIF [7:0]	RGB_SNAIB [7:0]	Clock cycle
0h	0h	0h	0h	0 timing clock
1h	1h	1h	1h	1 timing clock
2h	2h	2h	2h	2 timing clock
:	:	:	:	1 timing clock /step
Eh	Eh	Eh	Eh	14 timing clock
Fh	Fh	Fh	Fh	15 timing clock

Note: 1 timing clock = 4 multiple of Fosc.

	
Restriction	-

2.6.3. SET OSCM: Oscillator M setting (Page2 - C5h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>R/W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>C5</td></tr>
<tr><td>Parameter 1</td><td>R/W</td><td>-</td><td>OSC_DIV_EN0</td><td colspan="3">OSC_DIV_EN1[2:0]</td><td colspan="3">OSCM_ADJ[2:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">
This command is used to set oscillator M. OSCM (RC type) is used for HWRST & faster startup for MIPI LP mode.

OSC_DIV_EN0: Control oscillation of OSCM On/Off.
0: No division.
1: Division step is 2.

OSC_DIV_EN1: Control oscillation of OSCM On/Off.

<table>
<tr><th colspan="3">OSC_DIV_EN1[2:0]</th><th>Divided Step</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No divided</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>16</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>16</td></tr>
</table>

OSCM_ADJ[2:0]: Adjust frequency oscillator M.
<table>
<tr><th colspan="3">OSCL_ADJ[2:0]</th><th>frequency (MHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8.2328</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>10.234(default)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>12.221</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>14.197</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>16.166</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>18.108</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>20.043</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>21.976</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

3. JADARD COMMAND LIST

3.1. OTP table

OTP_INDEX (HEX)	Ref. Command	Ref. Index	Duplicate	B7	B6	B5	B4	B3	B2	B1	B0
0	SEQUENCE_CTRL	**P0_B0_01**	1	**NVALID**	DC0H[2:0]			-	DC1H[2:0]		
1		**P0_B0_02**		-	DC2H[2:0]			-	DC3H[2:0]		
2		**P0_B0_03**		-	-	-	-	-	DC7H[2:0]		
3		**P0_B0_04**		DC0L	DC1L	DC2L	DC3L	DC4L	DC5L	DC6L	DC7L
4		**P0_B0_05**		T0P[1:0]		T1P[1:0]		T8P[1:0]		-	VCOM_SEL
5		**P0_B0_06**		-	SOFT0H[2:0]			-	SOFT0L[2:0]		
E	SETRGBIF	**P0_BD_01**	1	**NVALID**	-	BLK_OPT	DEM	VSPL	HSPL	DEPL	PCPL
F		**P0_BD_02**		-	-	RGB_SEL[1:0]		-	-	RGB_SYNC_LN[9:8]	
10		**P0_BD_03**		RGB_SYNC_LN[7:0]							
11		**P0_BD_04**		RGB_SYNC_RESO_X[7:0]							
12		**P0_BD_05**		RGB_SYNC_VBP[7:0]							
13		**P0_BD_06**		RGB_SYNC_HBP[7:0]							
16	GAMMA_SET	**P0_B7_01**	1	**NVALID**	VGSP_S[6:0]						
17		**P0_B7_02**		VGMP_S[7:0]							
18		**P0_B7_03**		-	VGSN_S[6:0]						
19		**P0_B7_04**		VGMN_S[7:0]							
1A	OTP_SET	**P0_B8_01**	1	**NVALID**	-	VPP_DT[1:0]		VPP_VGHZ_CLK[3:0]			
1B		**P0_B8_02**		VPP_VGHZ_RT	VPP_VGHZ_NC	-	-	-	-	VPP_VGHZ_S[1:0]	
1C	POW_CTRL	**P0_B9_01**	1	**NVALID**	AP[2:0]			-	-	VCOM_EN	VGM_EN
1D		**P0_B9_02**		AVDDZ_NC	AVDDZ_D_NC	AVEEZ_NC	-	VGHZ_NC	VGLZ_NC	-	-
1E		**P0_B9_03**		MVZ_EN	MVZ_D_EN	-	-	VGHZ_EN	VGLZ_EN	-	-
20	DCDC_SEL	**P0_BB_01**	1	**NVALID**	VGHZ_RT	-	-	VGLZ_S[3:0]			
21		**P0_BB_02**		-	AVDDZ_D_S[2:0]			AVDDZ_S[1:0]		AVEEZ_S[1:0]	
22		**P0_BB_03**		VGHZ_CLK[3:0]				VGHZ_CLKB[1:0]		VGHZ_CLKP[1:0]	
23		**P0_BB_04**		VGLZ_CLK[3:0]				VGLZ_CLKB[1:0]		VGLZ_CLKP[1:0]	
24		**P0_BB_05**		MVZ_S_CLK[3:0]				MVZ_S_CLKB[1:0]		MVZ_S_CLKP[1:0]	
25		**P0_BB_06**		MVZ_G_CLK[3:0]				MVZ_G_CLKB[1:0]		MVZ_G_CLKP[1:0]	
26		**P0_BB_07**		NMVZ_D_CLK[3:0]				NMVZ_D_CLKB[1:0]		NMVZ_D_CLKP[1:0]	
27		**P0_BB_08**		MVZ_D_CLK[3:0]				MVZ_D_CLKB[1:0]		MVZ_D_CLKP[1:0]	
28	VDDD_CTRL	**P0_BC_01**	1	**NVALID**	VDDD_S0[2:0]			AVSSN_EN	AVSSN_S[2:0]		
29		**P0_BC_02**		-	VDDD_S1[2:0]			VDDD_VCI_EN	VDDD_S2[2:0]		
2A	GAS_CTRL	**P0_BE_01**	1	**NVALID**	-	-	-	-	-	-	-
2B		**P0_BE_02**		GAS_SLPIN_EN	GAS_OUT_EN	GAS_VCI_EN	GAS_IOVCC_EN	GAS_BLK_NUM[3:0]			

2C		**P0_BE_03**		GAS_DBS_SEN	GAS_DBS_GEN	GAS_DBS_LTH[5:0]						
2D		**P0_BE_04**		-	-	DC_GAS_VGH_EN	DC_GAS_VGL_EN	-	-	DC_GAS_MVZ_EN	DC_GAS_MVZ_D_EN	
32	SETSTBA	**P0_C0_01**	1	**NVALID**	GAP[2:0]			SAP[3:0]				
33		**P0_C0_02**		GAP2_EN	GAP2[2:0]			-	-	-	-	
34	SETPANEL	**P0_C1_01**	1	**NVALID**	-	-	SS_PANEL	GS_PANEL	REV_PANEL	CFHR	-	
35	SET_BIST	**P0_C2_01**	1	**NVALID**	-	-	-	TEST_PAT_EN	TEST_PATTERN[2:0]			
36	SETRGBCYC	**P0_C3_01**	1	**NVALID**	-	-	-	IDLE_TYPE	RGB_INV_NP[2:0]			
37		**P0_C3_02**		-	RGB_INV_PI[2:0]			-	RGB_INV_I[2:0]			
38		**P0_C3_03**		-	-	-	-	RGB_GND[3:0]				
39		**P0_C3_04**		-	-	-	RGB_EQ1[4:0]					
3A		**P0_C3_05**		-	-	RGB_CHGEN_ON[5:0]						
3B		**P0_C3_06**		RGB_CHGEN_OFF[7:0]								
3C		**P0_C3_07**		GASHORT_ON[7:0]								
3D		**P0_C3_08**		RGB_OFF[7:0]								
3E		**P0_C3_09**		-	-	GAOPOFFEN	GAOPOFF[4:0]					
45	SET_TCON	**P0_C4_01**	1	**NVALID**	-	LN[9:8]		-	-	-	-	
46		**P0_C4_02**		LN[7:0]								
47		**P0_C4_03**		SLT_NP[7:0]								
48		**P0_C4_04**		VFP_NP[7:0]								
49		**P0_C4_05**		VBP_NP[7:0]								
4A		**P0_C4_06**		HBP_NP[7:0]								
4B		**P0_C4_07**		SLT_I[7:0]								
4C		**P0_C4_08**		VFP_I[7:0]								
4D		**P0_C4_09**		VBP_I[7:0]								
4E		**P0_C4_10**		HBP_I[7:0]								
4F		**P0_C4_11**		SLT_PI[7:0]								
50		**P0_C4_12**		VFP_PI[7:0]								
51		**P0_C4_13**		VBP_PI[7:0]								
52		**P0_C4_14**		HBP_PI[7:0]								
53		**P0_C4_15**		HBP_NCK[3:0]				HFP_NCK[3:0]				
54		**P0_C4_16**		TCON_OPT1[15:8]								
55		**P0_C4_17**		TCON_OPT1[7:0]								
56	SET_GD	**P0_D0_01**	1	**NVALID**	-	-	-	-	GD_GAS_GATE_CLK	GD_EN_GND_VCI	GD_LRSW	
57		**P0_D0_02**		-	-	GD_ON[5:0]						
58		**P0_D0_03**		GD_OFF[7:0]								
59		**P0_D0_04**		-	-	GD_EQ_PTR0[5:0]						
5A		**P0_D0_05**		GD_EQ_PTR1[7:0]								

5B		**P0_D0_06**		-	-	-	GD_PT GISC	GD_ISC[3:0]
68	SET_R_GAMMA	**P0_C8_01**	1	**NVALID**	-	RPA15[5:0]		
69		**P0_C8_02**		-	-	RPA14[5:0]		
6A		**P0_C8_03**		-	-	RPA13[5:0]		
6B		**P0_C8_04**		-	-	RPA12[5:0]		
6C		**P0_C8_05**		-	-	RPA11[5:0]		
6D		**P0_C8_06**		-	-	RPA10[5:0]		
6E		**P0_C8_07**		-	-	RPA9[5:0]		
6F		**P0_C8_08**		-	-	RPA8[5:0]		
70		**P0_C8_09**		-	-	RPA7[5:0]		
71		**P0_C8_10**		-	-	RPA6[5:0]		
72		**P0_C8_11**		-	-	RPA5[5:0]		
73		**P0_C8_12**		-	-	RPA4[5:0]		
74		**P0_C8_13**		-	-	RPA3[5:0]		
75		**P0_C8_14**		-	-	RPA2[5:0]		
76		**P0_C8_15**		-	-	RPA1[5:0]		
77		**P0_C8_16**		-	-	RPA0[5:0]		
78		**P0_C8_17**		-	-	RNA15[5:0]		
79		**P0_C8_18**		-	-	RNA14[5:0]		
7A		**P0_C8_19**		-	-	RNA13[5:0]		
7B		**P0_C8_20**		-	-	RNA12[5:0]		
7C		**P0_C8_21**		-	-	RNA11[5:0]		
7D		**P0_C8_22**		-	-	RNA10[5:0]		
7E		**P0_C8_23**		-	-	RNA9[5:0]		
7F		**P0_C8_24**		-	-	RNA8[5:0]		
80		**P0_C8_25**		-	-	RNA7[5:0]		
81		**P0_C8_26**		-	-	RNA6[5:0]		
82		**P0_C8_27**		-	-	RNA5[5:0]		
83		**P0_C8_28**		-	-	RNA4[5:0]		
84		**P0_C8_29**		-	-	RNA3[5:0]		
85		**P0_C8_30**		-	-	RNA2[5:0]		
86		**P0_C8_31**		-	-	RNA1[5:0]		
87		**P0_C8_32**		-	-	RNA0[5:0]		
88		**P0_C8_01**	2	**NVALID**	-	RPA15[5:0]		
89		**P0_C8_02**		-	-	RPA14[5:0]		
8A		**P0_C8_03**		-	-	RPA13[5:0]		
8B		**P0_C8_04**		-	-	RPA12[5:0]		
8C		**P0_C8_05**		-	-	RPA11[5:0]		
8D		**P0_C8_06**		-	-	RPA10[5:0]		
8E		**P0_C8_07**		-	-	RPA9[5:0]		
8F		**P0_C8_08**		-	-	RPA8[5:0]		

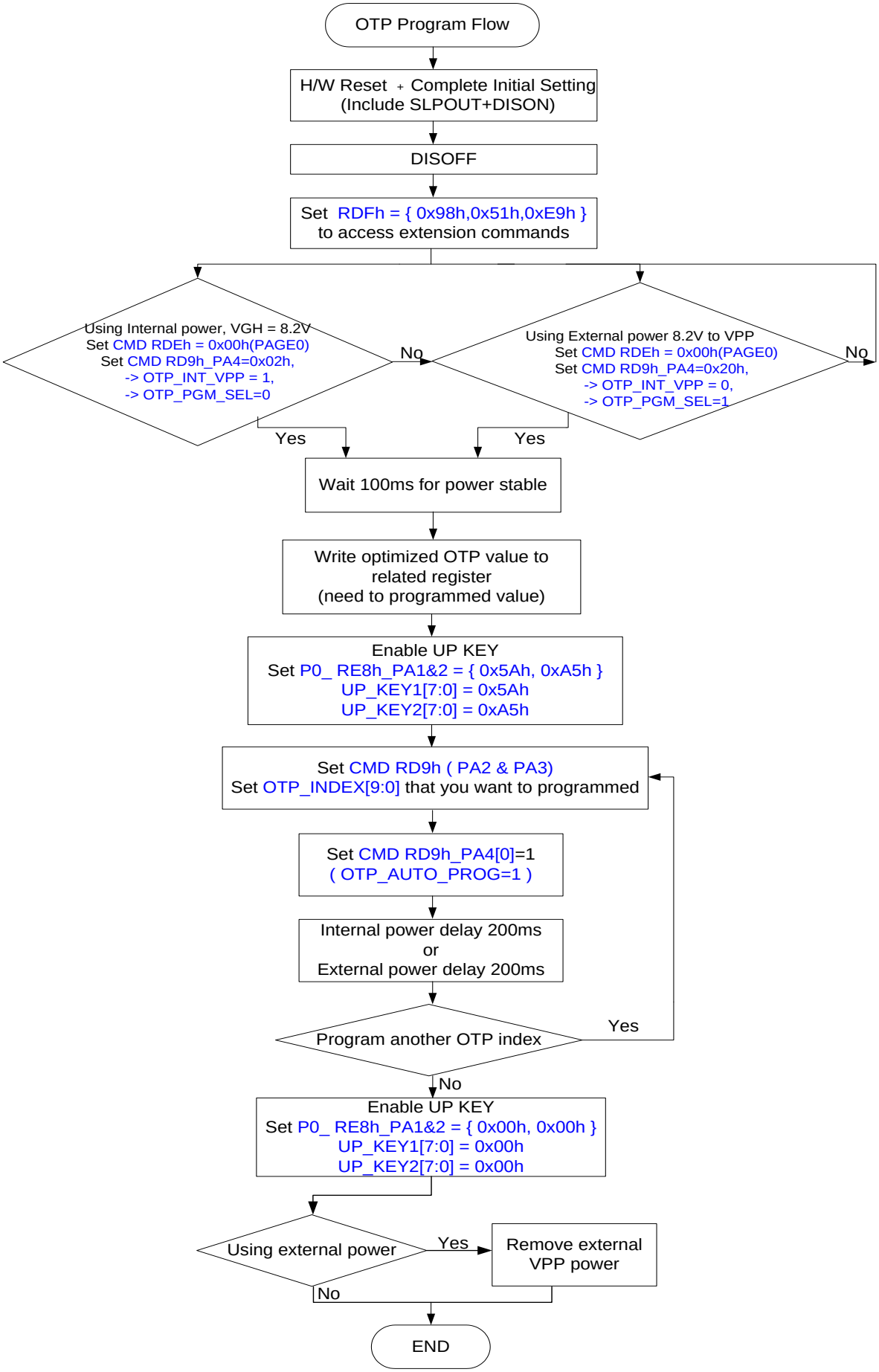
90		**P0_C8_09**		-	-	RPA7[5:0]
91		**P0_C8_10**		-	-	RPA6[5:0]
92		**P0_C8_11**		-	-	RPA5[5:0]
93		**P0_C8_12**		-	-	RPA4[5:0]
94		**P0_C8_13**		-	-	RPA3[5:0]
95		**P0_C8_14**		-	-	RPA2[5:0]
96		**P0_C8_15**		-	-	RPA1[5:0]
97		**P0_C8_16**		-	-	RPA0[5:0]
98		**P0_C8_17**		-	-	RNA15[5:0]
99		**P0_C8_18**		-	-	RNA14[5:0]
9A		**P0_C8_19**		-	-	RNA13[5:0]
9B		**P0_C8_20**		-	-	RNA12[5:0]
9C		**P0_C8_21**		-	-	RNA11[5:0]
9D		**P0_C8_22**		-	-	RNA10[5:0]
9E		**P0_C8_23**		-	-	RNA9[5:0]
9F		**P0_C8_24**		-	-	RNA8[5:0]
A0		**P0_C8_25**		-	-	RNA7[5:0]
A1		**P0_C8_26**		-	-	RNA6[5:0]
A2		**P0_C8_27**		-	-	RNA5[5:0]
A3		**P0_C8_28**		-	-	RNA4[5:0]
A4		**P0_C8_29**		-	-	RNA3[5:0]
A5		**P0_C8_30**		-	-	RNA2[5:0]
A6		**P0_C8_31**		-	-	RNA1[5:0]
A7		**P0_C8_32**		-	-	RNA0[5:0]
A8		**P0_C8_01**		**NVALID**	-	RPA15[5:0]
A9		**P0_C8_02**		-	-	RPA14[5:0]
AA		**P0_C8_03**		-	-	RPA13[5:0]
AB		**P0_C8_04**		-	-	RPA12[5:0]
AC		**P0_C8_05**		-	-	RPA11[5:0]
AD		**P0_C8_06**		-	-	RPA10[5:0]
AE		**P0_C8_07**		-	-	RPA9[5:0]
AF		**P0_C8_08**		-	-	RPA8[5:0]
B0		**P0_C8_09**	3	-	-	RPA7[5:0]
B1		**P0_C8_10**		-	-	RPA6[5:0]
B2		**P0_C8_11**		-	-	RPA5[5:0]
B3		**P0_C8_12**		-	-	RPA4[5:0]
B4		**P0_C8_13**		-	-	RPA3[5:0]
B5		**P0_C8_14**		-	-	RPA2[5:0]
B6		**P0_C8_15**		-	-	RPA1[5:0]
B7		**P0_C8_16**		-	-	RPA0[5:0]
B8		**P0_C8_17**		-	-	RNA15[5:0]

B9		**P0_C8_18**		-	-	RNA14[5:0]
BA		**P0_C8_19**		-	-	RNA13[5:0]
BB		**P0_C8_20**		-	-	RNA12[5:0]
BC		**P0_C8_21**		-	-	RNA11[5:0]
BD		**P0_C8_22**		-	-	RNA10[5:0]
BE		**P0_C8_23**		-	-	RNA9[5:0]
BF		**P0_C8_24**		-	-	RNA8[5:0]
C0		**P0_C8_25**		-	-	RNA7[5:0]
C1		**P0_C8_26**		-	-	RNA6[5:0]
C2		**P0_C8_27**		-	-	RNA5[5:0]
C3		**P0_C8_28**		-	-	RNA4[5:0]
C4		**P0_C8_29**		-	-	RNA3[5:0]
C5		**P0_C8_30**		-	-	RNA2[5:0]
C6		**P0_C8_31**		-	-	RNA1[5:0]
C7		**P0_C8_32**		-	-	RNA0[5:0]
C8		**P0_C8_01**		**NVALID**	-	RPA15[5:0]
C9		**P0_C8_02**		-	-	RPA14[5:0]
CA		**P0_C8_03**		-	-	RPA13[5:0]
CB		**P0_C8_04**		-	-	RPA12[5:0]
CC		**P0_C8_05**		-	-	RPA11[5:0]
CD		**P0_C8_06**		-	-	RPA10[5:0]
CE		**P0_C8_07**		-	-	RPA9[5:0]
CF		**P0_C8_08**		-	-	RPA8[5:0]
D0		**P0_C8_09**		-	-	RPA7[5:0]
D1		**P0_C8_10**		-	-	RPA6[5:0]
D2		**P0_C8_11**		-	-	RPA5[5:0]
D3		**P0_C8_12**		-	-	RPA4[5:0]
D4		**P0_C8_13**		-	-	RPA3[5:0]
D5		**P0_C8_14**	4	-	-	RPA2[5:0]
D6		**P0_C8_15**		-	-	RPA1[5:0]
D7		**P0_C8_16**		-	-	RPA0[5:0]
D8		**P0_C8_17**		-	-	RNA15[5:0]
D9		**P0_C8_18**		-	-	RNA14[5:0]
DA		**P0_C8_19**		-	-	RNA13[5:0]
DB		**P0_C8_20**		-	-	RNA12[5:0]
DC		**P0_C8_21**		-	-	RNA11[5:0]
DD		**P0_C8_22**		-	-	RNA10[5:0]
DE		**P0_C8_23**		-	-	RNA9[5:0]
DF		**P0_C8_24**		-	-	RNA8[5:0]
E0		**P0_C8_25**		-	-	RNA7[5:0]
E1		**P0_C8_26**		-	-	RNA6[5:0]

E2		**P0_C8_27**		-	-	RNA5[5:0]					
E3		**P0_C8_28**		-	-	RNA4[5:0]					
E4		**P0_C8_29**		-	-	RNA3[5:0]					
E5		**P0_C8_30**		-	-	RNA2[5:0]					
E6		**P0_C8_31**		-	-	RNA1[5:0]					
E7		**P0_C8_32**		-	-	RNA0[5:0]					
134	SETDSISETUP1	**P0_CC_01**	1	**NVALID**	ULPS_BY_D0	ESD_PROTECT_CLK	RST_TRIGGER_EN	SPECIAL_PKT_EN	-	-	-
135		**P0_CC_02**		SETUP11_7	VC_ID_CHK	VC_ID[1:0]		ERR_FG_EN	ERR_RPT_EN	INIT_TIME_SET[1:0]	
136		**P0_CC_03**		SETUP12_7	-	TX_OSC_DIV	TA_GO[2:0]			TA_GET[1:0]	
137	SETPHY1	**P0_CD_01**	1	**NVALID**	RX_LDO_SEL[2:0]			-	-	HS_RX_RT[1:0]	
138		**P0_CD_02**		-	TX_LDO_SEL[2:0]			-	-	LP_TX_SR[1:0]	
139	RAMCTRL	**P0_D7_01**	1	**NVALID**	-	SPI_2LAN_EN	RP	RM	-	DM[1:0]	
13A		**P0_D7_02**		SCL_PL	EXT_VS_PL	EPF[1:0]		ENDIAN	-	MDT[1:0]	
13B	SET_WD	**P0_DD_01**	1	**NVALID**	WD_OFF	WD_MODE[1:0]		FBLK_EN	WD_CLK_SEL[2:0]		
13C		**P0_DD_02**		WD_TIMER_TCON[7:0]							
144	SETID(OTP*2)	**P0_E9_01**	1	**NVALID**	-	-	-	-	-	-	-
145		**P0_E9_02**		ID1[7:0]							
146		**P0_E9_03**		ID2[7:0]							
147		**P0_E9_04**		ID3[7:0]							
148		**P0_E9_05**		ID4[7:0]							
149		**P0_E9_01**	2	**NVALID**	-	-	-	-	-	-	-
14A		**P0_E9_02**		ID1[7:0]							
14B		**P0_E9_03**		ID2[7:0]							
14C		**P0_E9_04**		ID3[7:0]							
14D		**P0_E9_05**		ID4[7:0]							
150	PWM_CTRL	**P1_B5_01**	1	**NVALID**	-	-	LE_LEDON_EN	LE_LEDON_POL	-	LE_LEDPWM_POL	LE_LED_VOL
151		**P1_B5_02**		LE_NONNORM_DD_EN	LE_EN_EXT_EN	LE_PWM_SYNC2VS	LE_DD_RST	-	LE_PWM_DUTY_PCN[2:0]		
152		**P1_B5_03**		LE_SEL_CLK_DIV[7:0]							
153		**P1_B5_04**		LE_N_VAL[7:0]							
15D	DCDC_OPT	**P2_B7_01**	1	**NVALID**	GAS_SHT_EN	MVZ_S2D	MVZ_S2G	MIM_BLK_AND_DISP3	MIM_BPASS_2DFF	MIM_PON_SOFT	MIM_BLK_S
15E		**P2_B7_02**		MVZ_IBS	MVZ_D_IBS	MVZ_SOFT	-	VGHZ_IBS	VGLZ_IBS	-	-
15F		**P2_B7_03**		MVZ_NOPS	MVZ_D_NOPS	VGHZ_NOPS	VGLZ_NOPS	VGHZ_DISCH	VGLZ_DISCH	VGHZ_PAVDD	VDDS_OPT
160		**P2_B7_04**		DDS[7:0]							
161	DCDC_SET	**P2_B8_01**	1	**NVALID**	VCL_S	VCIP2X_S[1:0]		VGHZ_OV_PAVDD	AVDDZ_D_OV_S[2:0]		
162		**P2_B8_02**		EQ2_EN	-	DCDC_EQ2[5:0]					

163		**P2_B8_03**		EQ3_EN	-	DCDC_EQ3[5:0]				
164		**P2_B8_04**		-	-	DCDC_GOV_S[5:0]				
165		**P2_B8_05**		-	-	DCDC_GOV_E[5:0]				
16C	SETRGBCYC2	**P2_C1_01**	1	**NVALID**	SDPRDUM	SDDUM[1:0]	SDSW[1:0]	SDPORCH[1:0]		
16D		**P2_C1_02**		RGB_SPAIF[3:0]			RGB_SPAIB[3:0]			
16E		**P2_C1_03**		RGB_SNAIF[3:0]			RGB_SNAIB[3:0]			
16F		**P2_C1_04**		-	-	SDSW_GAS[1:0]	-	-	SDPARTIAL[1:0]	
178	SETTCON_OPT	**P2_C3_01**	1	**NVALID**	TCON_OPT2[22:16]					
179		**P2_C3_02**		TCON_OPT2[15:8]						
17A		**P2_C3_03**		TCON_OPT2[7:0]						
17B		**P2_C3_04**		LCLK_STA[3:0]			LCLK_PARK_STA	PWR_TC_CLK_OFF	PWR_SD_OFF	-
17C		**P2_C3_05**		L2EN_STR_OPT	STPLUSE_E[2:0]		-	-	STPLUSE_S[1:0]	
17D		**P2_C3_06**		L3EN_E[3:0]			L3EN_S[3:0]			
17E		**P2_C3_07**		L2EN_OFFSET[7:0]						
17F		**P2_C3_08**		L2EN0_E[3:0]			L2EN0_S[3:0]			
180		**P2_C3_09**		L2EN1_E[3:0]			L2EN1_S[3:0]			
181		**P2_C3_10**		L2EN2_E[3:0]			L2EN2_S[3:0]			
182		**P2_C3_11**		L2EN3_E[3:0]			L2EN3_S[3:0]			
183		**P2_C3_12**		L2EN_STR[7:0]						
184	SET_OSCM	**P2_C5_01**	1	**NVALID**	OSC_DIV_EN0	OSC_DIV_EN1[2:0]		OSCM_ADJ[2:0]		

3.2. OTP Programming Flow



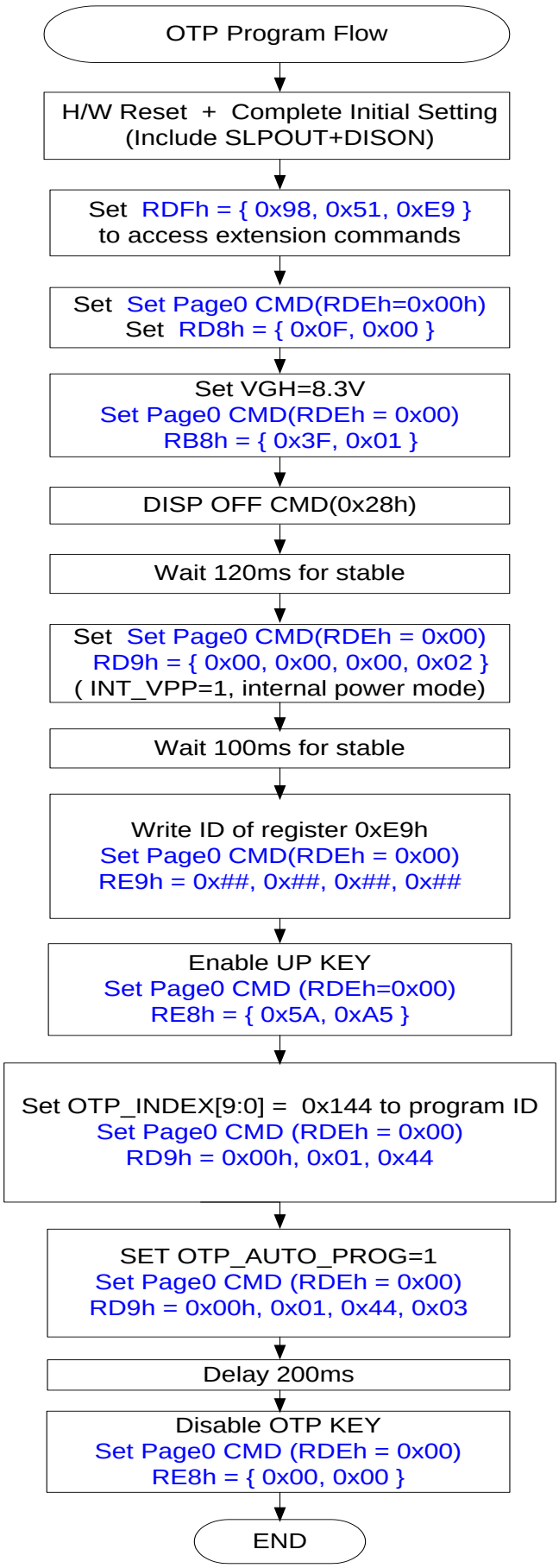
3.3. Programming Sequence

Step	Operation
1	Power on and HWRST the module. Then do SLPOOUT.
2	Set 0xDFh = 0x98h,0x51h,0XE9h to access extension commands.
3	Set page0 CMD(RDEh=0x00h) , 1) Internal power mode, set Page0 RD9h_PA4=0x02 (OTP_INT_VPP = 1 and OTP_PGM_SEL=0) 2) External power mode , feed external power 8.3 to VPP then set CMD RD9h_PA4=0x20 (OTP_INT_VPP = 0 and OTP_PGM_SEL=1).
4	Wait 100ms for VPP power stable.
5	Write optimized OTP value to related register.
6	Set Page0 CMD(RDEh=0x00h), then set Page0_0xE8h = 0x5Ah, 0xA5h to enable UP KEY.
7	Set 0xD9h_PA2&PA3 (OTP_INDEX[9:0]) that you want to programmed.
8	Set 0xD9h_PA4[0]=1 (OTP_AUTO_PROG=1)
9	Delay 200ms for internal power to program OTP. Or delay 200ms for external power to program OTP.
10	One OTP block programming was completed. Return to step (7) for next OTP block programming. Or go next step if all OTP programming is finished.
11	Set Page0_0xE8h = 0x00h, 0x00h to disable OTP KEY.
12	If you use external power, remove the external power 8.3V from VPP.

Note:

1. All OTP default value is 1.
2. OTP can be reloaded only NVALID bit is burned(value is 0).
3. Fifipower driver IC do auto OTP programming. User only set the start OTP_INDEX of the Ref. CMD block then all block is programmed by driver IC. This function also can be used for MTP Ref. CMD block.
   For example:
   a. To program VCOM_SET 1st time, user set OTP_INDEX=006h then from OTP_INDEX=006h to OTP_INDEX=007h(Ref. CMD block of 1st VCOM_SET) is programmed by driver IC.
   b. To program VCOM_SET 2nd time, user still set OTP_INDEX=006h then from OTP_INDEX=008h to OTP_INDEX=009h(Ref. CMD block of 2nd VCOM_SET) is programmed by driver IC.

3.4. OTP Programming example of SETID setting



3.5. OTP read example