



JADARD

JD9853

Data Sheet

240RGB x 320 dot, 262K color,
with internal GRAM, a-Si TFT LCD Single Chip Driver

Preliminary Version 0.00
2022/03/24

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1. Revision History

Version	Date	Description of modification
0.00	2023/2/14	New setup

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2. Introduction

The JD9853 is a 262,144-color single-chip SOC driver for a-Si TFT liquid crystal display with resolution of 240RGBx320dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

The JD9853 supports parallel 8-/9-bit data bus MCU interface, 6-bit data bus RGB interface, 3-/4-line serial peripheral interface (SPI), 2 lane SPI data transmission and Quad serial peripheral interface (QSPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The JD9853 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. JD9853 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the JD9853 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

3. Features

- Display resolution: 240xRGB(H) x 320(V)
- LCD Driver Output:
 - 720 source channels
 - 320 gate channels
- Frame Memory Size: 240 x 320 x 18-bit = 1382400 bits
- System Interface
 - Parallel 8080-series MCU Interface (8-bits, 9-bits)
 - RGB Interface (6-bits)
 - Serial Peripheral Interface (SPI) (8-bits, 9-bits and 2 data lane SPI)
 - Quad serial peripheral interface (QSPI)
- Display mode:
 - Full color mode (Idle mode OFF): 262K-color
 - Reduce color mode (Idle mode ON): 8-color
- Pixel Color Format (Color Depth)
 - 16-bit/pixel: RGB=(565)
 - 18-bit/pixel: RGB=(666)
- On chip functions:
 - DC/DC converter
 - Timing generator
 - Internal Oscillator generation
 - OTP memory to store initialization register settings
 - Support Sunlight Readability (SLR)
- Display inversion type support
 - Dot Inversion
 - Column Inversion
- Operation Temperature range: -40 to +85 °C
- Wide Supply Voltage Range
 - IOVCC = 1.65V ~ 3.3V (logic)
 - VCI = 2.6V ~ 3.3V (analog)
- On-Chip Power System:
 - Source Voltage: +6.4~ -4.6V
 - Gate driver output voltage
 - VGH - GND = 11.0V ~ 16.0V
 - VGL - GND = -7.0V ~ -12.25V

-
- On-chip OTP program voltage generator
 - OTP memory to store initialization register settings
 - 1 time OTP for Gamma Correction setting
 - 3 times OTP for VGMP/VGSP/VGMN/VGSN setting
 - 2 times OTP for ID setting

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4. Device Overview

4.1. Block Diagram

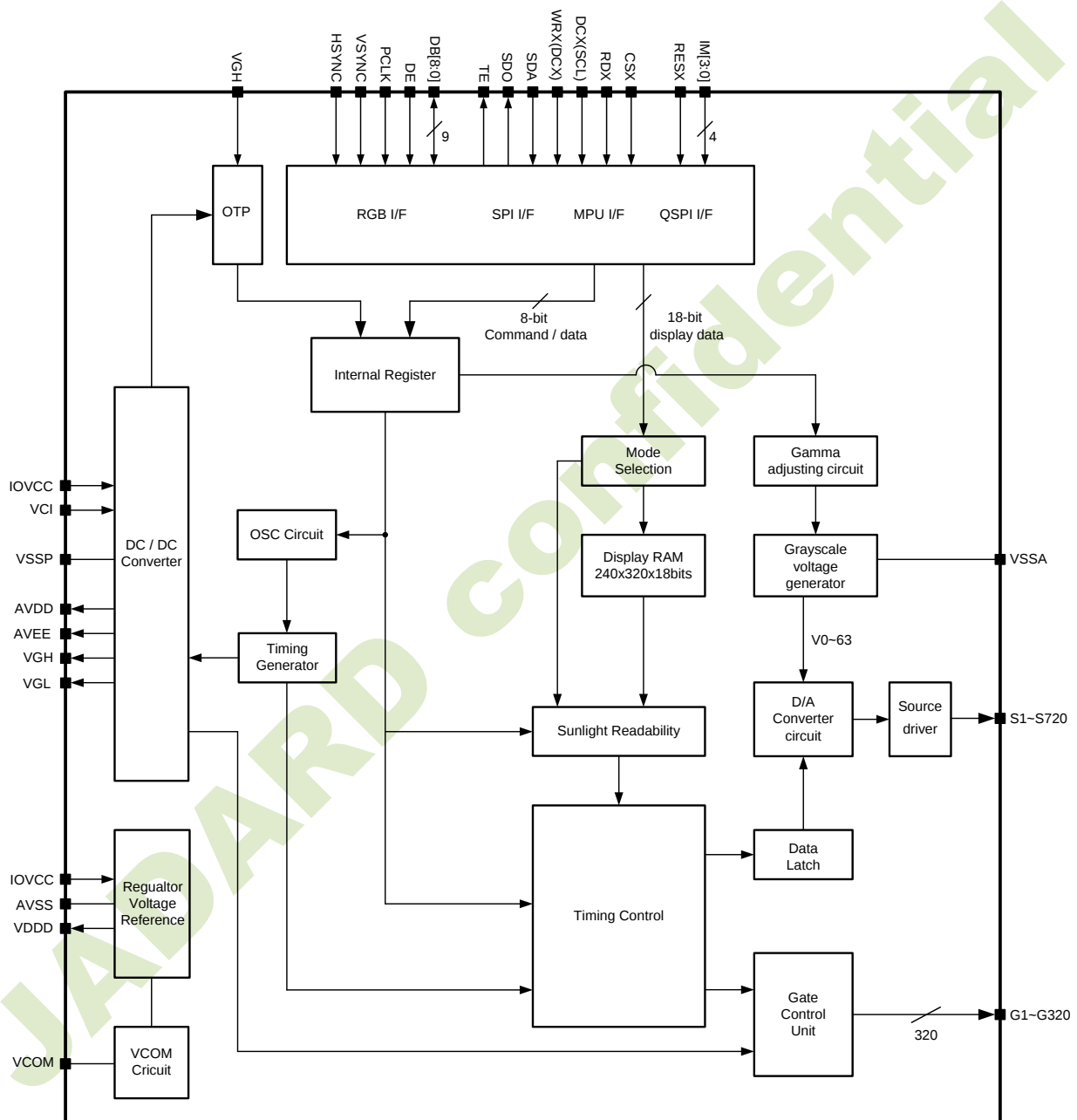


Figure. 4.1 Block Diagram

4.2. LCD power generation scheme

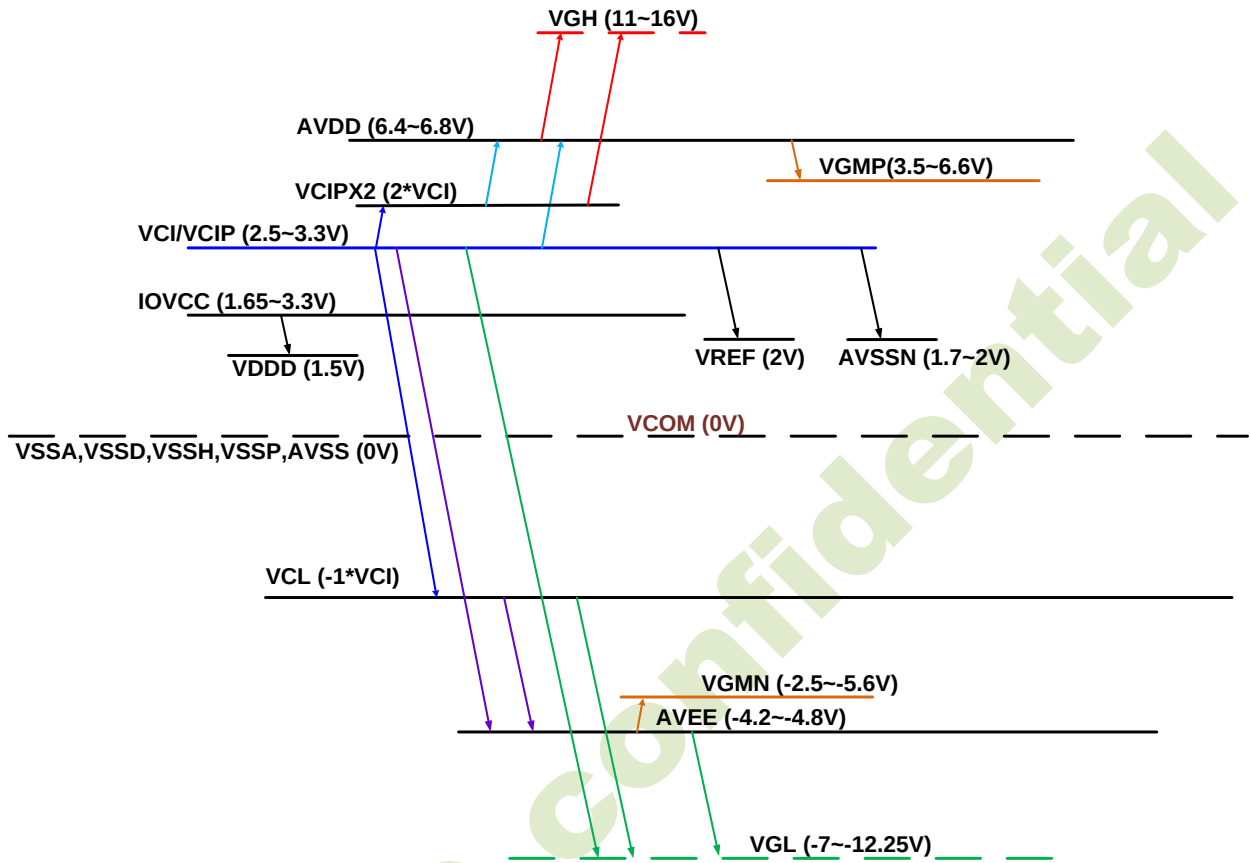


Figure. 4.2 LCD power generation scheme

4.3. Output voltage range

JD9853 generates corresponding voltage with a-Si TFT LCD panel by internal power supply circuit. Please set up each voltage output according to the LCD panel.

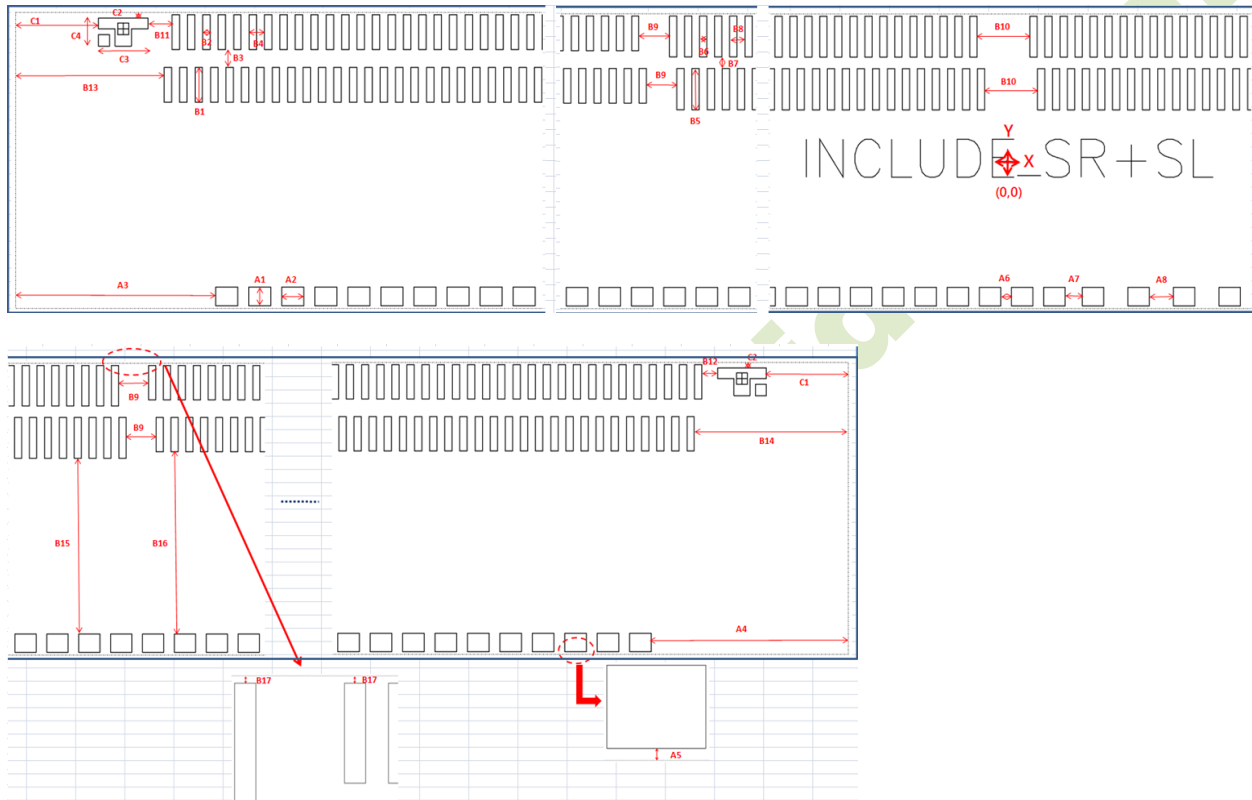
Name	Function	Set up value	Note
AVDD	DC/DC converter circuit output	+6.4~ +6.8V	Do not exceed 6.8V
AVEE	DC/DC converter circuit output	-4.2~ -4.8V	Do not exceed -4.8V
VGMP	Reference voltage for gamma circuit	+3.5V~ +6.6V	Reference register
VGMPN	Reference voltage for gamma circuit	-2.5V~ -5.6V	Reference register
VGH	Positive gate driver output voltage level	+11~ +16V	Depend on AVDD & AVEE
VGL	Negative gate driver output voltage level	-7V ~ -12.25V	Depend on AVDD & AVEE
VCOM	VCOM DC voltage	0V	-
T_VDDD	Digital power.	+1.5V	-

5. Pad Arrangement

5.1.PAD assignment

Chip Size: 15352um * 510um

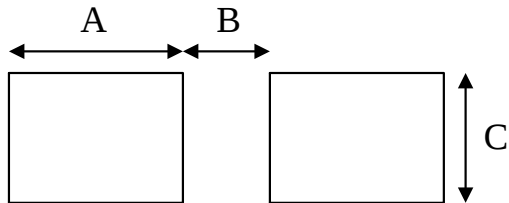
Overview (Simple view)



Condition-1 (+/- 0um temp. compensation)				Unit=um							
INPUT PAD				OUTPUT PAD				AMARK(如下圖)			
Symbol	Size	Number	Tolerance	Symbol	Size	Number	Tolerance	Symbol	Size	Tolerance	
A1	31.8	NO.1 ~ NO.232		B1	60	NO.233 ~ NO.395		C1	151		
A2	40	NO.1 ~ NO.232		B2	13.5	NO.1116 ~ NO.1278		C2	10.5		
A3	363.5			B3	31	NO.233 ~ NO.395		C3	90		
A4	363.5			B4	28	NO.1116 ~ NO.1278		C4	48		
A5	4.5			B5	71						
A6	20	NO.1 ~ NO.124		B6	13.5	NO.396 ~ NO.1115					
:	:	NO.153 ~ NO.154		B7	20	NO.396 ~ NO.1115					
:	:	NO.161 ~ NO.232		B8	28						
A7	32.5	NO.124 ~ NO.125		B9	56.5						
:	:	NO.129 ~ NO.131		B10	98.5						
:	:	NO.134 ~ NO.136		B11	43.25						
:	:	NO.139 ~ NO.143		B12	29.25						
:	:	NO.144 ~ NO.146		B13	270.25						
:	:	NO.147 ~ NO.149		B14	284.25						
:	:	NO.152 ~ NO.153		B15	307.2						
:	:	NO.154 ~ NO.155		B16	318.2						
A8	45	NO.125 ~ NO.129		B17	4.5						
:	:	NO.131 ~ NO.134									
:	:	NO.136 ~ NO.139									
:	:	NO.143 ~ NO.144									
:	:	NO.146 ~ NO.147									
:	:	NO.149 ~ NO.152									
:	:	NO.155 ~ NO.160									

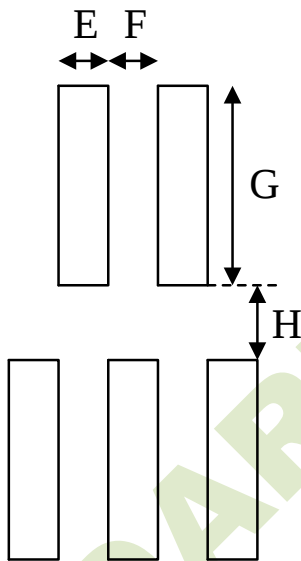
5.2. Input and Output Bump Dimension

5.2.1. Input Pad



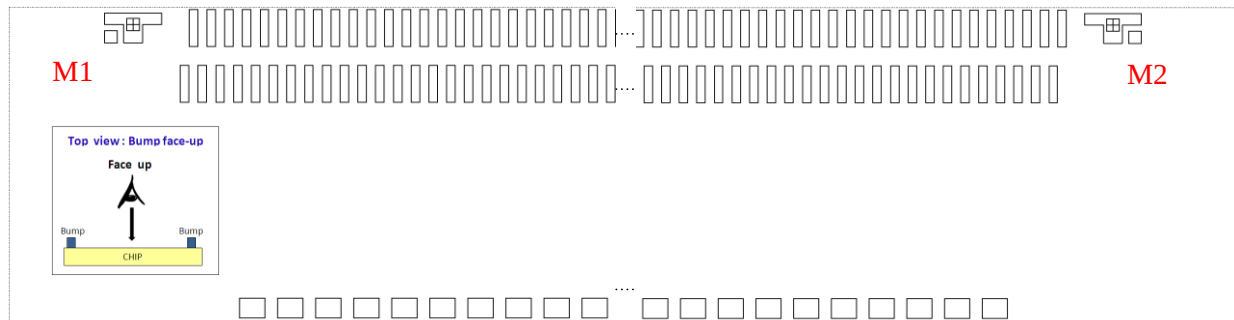
Symbol	Item	Size
A	Bump Width	40 μm
B	Bump Gap	20~ 45 μm
C	Bump Hight	31.8 μm

5.2.2. Output Pad

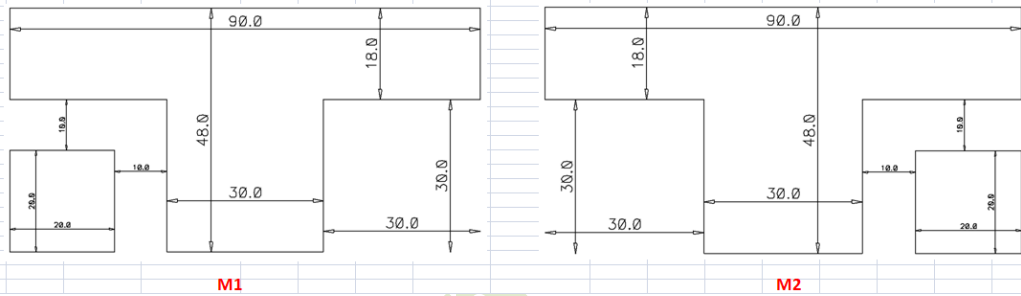


Symbol	Item	Size
E	Bump Width	13.5 μm
F	Bump Gap1	14.5 μm
G	Bump Hight (S1~S720)	71 μm
	Bump Hight (G1~G320)	60 μm
H	Bump Gap2 (S1~S720)	20 μm
	Bump Gap2 (G1~G320)	31 μm

5.3.Alignment Mark Dimension



ALIGNMENT		
M1	7480	226.5
M2	7480	226.5



6. Pin Description

6.1. Power Supply Pins

Pin Name	I/O	Type	Descriptions
IOVCC	I	Digital Power	Power supply for interface logic circuits(1.65~3.3V)
VCI	I	Analog Power	Power supply for analog circuit blocks(2.6~3.3V)
VGH	I	OTP Power	External high voltage pin used in OTP mode and operates at 8.3V. If not used, let this pin open.
VSSA/AVSS/VSSP	I	Analog Ground	System ground level for analog circuit blocks. Connect to VSSA on the FPC to prevent noise.
VSSD	I	Digital Ground	System ground level for Digital circuit blocks. Connect to VSSD on the FPC to prevent noise.

6.2.Interface Logic Pins

Pin Name	I/O	Type	Descriptions																																																		
IM[3:0]	I	(IOVCC/GND)	-Select the MCU interface mode																																																		
			<table><tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU-Interface</th><th>Data Pin</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 8-bit parallel Interface I</td><td>DB[7:0]</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 9-bit parallel Interface I</td><td>DB[8:0]</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Quad serial interface</td><td>SDA: in/out DB[2:0]: in</td></tr><tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9-bit serial interface I</td><td>SDA: in/out</td></tr><tr><td>2 data lane serial interface</td><td>SDA: in/out WRX: in</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8-bit serial interface I</td><td>SDA: in/out</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line 9-bit serial interface II</td><td>SDA: in/ SDO: out</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-line 8-bit serial interface II</td><td>SDA:in/ SDO: out</td></tr></table>	IM3	IM2	IM1	IM0	MCU-Interface	Data Pin	0	0	0	0	8080 8-bit parallel Interface I	DB[7:0]	0	0	1	0	8080 9-bit parallel Interface I	DB[8:0]	0	1	0	0	Quad serial interface	SDA: in/out DB[2:0]: in	0	1	0	1	3-line 9-bit serial interface I	SDA: in/out	2 data lane serial interface	SDA: in/out WRX: in	0	1	1	0	4-line 8-bit serial interface I	SDA: in/out	1	1	0	1	3-line 9-bit serial interface II	SDA: in/ SDO: out	1	1	1	0	4-line 8-bit serial interface II	SDA:in/ SDO: out
			IM3	IM2	IM1	IM0	MCU-Interface	Data Pin																																													
			0	0	0	0	8080 8-bit parallel Interface I	DB[7:0]																																													
			0	0	1	0	8080 9-bit parallel Interface I	DB[8:0]																																													
			0	1	0	0	Quad serial interface	SDA: in/out DB[2:0]: in																																													
			0	1	0	1	3-line 9-bit serial interface I	SDA: in/out																																													
							2 data lane serial interface	SDA: in/out WRX: in																																													
			0	1	1	0	4-line 8-bit serial interface I	SDA: in/out																																													
			1	1	0	1	3-line 9-bit serial interface II	SDA: in/ SDO: out																																													
1	1	1	0	4-line 8-bit serial interface II	SDA:in/ SDO: out																																																
MPU Parallel interface bus and serial interface select																																																					
If use RGB Interface must select serial interface.																																																					
RESX	I	MCU (IOVCC/GND)	-This signal will reset the device and must be applied to properly initialize the chip. -Signal is active low.																																																		
CSX	I	MCU (IOVCC/GND)	-Chip select input pin. Low enable. High disable. -If not used, this pin should be connected to IOVCC.																																																		
DCX_SCL	I	MCU (IOVCC/GND)	-Data/command selection pin in parallel interface. When DCX='1', data is selected. When DCX='0', command is selected. -This pin is used to be serial interface clock. -If not used, this pin should be connected to IOVCC.																																																		
RDX	I	MCU (IOVCC/GND)	-Read enable in 8080 MCU parallel interface. - If not used, this pin should be connected to IOVCC.																																																		
WRX	I	MCU (IOVCC/ GND)	-Write enable in MCU parallel interface. -Data/command selection pin in 4-line serial interface. -Second Data lane in 2 data lane serial interface. - If not used, this pin should be connected to IOVCC.																																																		
DB[8:0]	I/O	MCU (IOVCC/ GND)	-DB[8:0] are used as MCU parallel interface data bus. -DB[8:0] are used as RGB interface data bus. - If not used, this pin should be connected to IOVCC or GND.																																																		
SDA	I/O	MCU (IOVCC/ GND)	-When IM[3]:Low, Serial in/out signal in SPI interface. -When IM[3]:High, Serial input signal in SPI interface. -The data is latched on the rising edge of the SCL signal.																																																		

			- If not used, this pin should be connected to IOVCC or GND.
SDO	O	MCU (IOVCC/GND)	-Serial data output signal. -If not used, open this pin
TE	O	MCU (IOVCC/ GND)	-Tearing effect output pin to synchronize MPU to frame writing. If not used, open this pin.
LEDPWM	O	MCU (IOVCC/ GND)	-PWM output signal for backlight control. If not used, open this pin.
PCLK	I	MCU (IOVCC/GND)	-Dot clock signal for RGB interface operation. - If not used, this pin should be connected to IOVCC or GND.
VSYNC	I	MCU (IOVCC/GND)	-Frame synchronizing signal for RGB interface operation. - If not used, this pin should be connected to IOVCC or GND.
HSYNC	I	MCU (IOVCC/ GND)	-Line synchronizing signal for RGB interface operation. - If not used, this pin should be connected to IOVCC or GND.
DE	I	MCU (IOVCC/ GND)	-Data enable signal for RGB interface operation. - If not used, this pin should be connected to IOVCC or GND.

Note1. When CSX='1', there is no influence to the parallel and serial interface.

6.3.Driver Output Pins

Pin Name	I/O	Descriptions
S1~ S720	O	Source output signals.. Leave the pin to open when not in use.
G1~ G320	O	Gate output signals. Leave the pin to open when not in use.
AVDD	O	Analog positive power.
AVEE	O	Analog negative power.
VGH	O	Power supply for the gate driver (Positive).
VGL	O	Power supply for the gate driver (Negative).
VCOM_L VCOM_R	O	A power supply for the TFT-LCD common electrode.
T_VDDD	O	Digital power.
VGMP	O	Reference voltage for gamma circuit.
VGMN	O	Reference voltage for gamma circuit.
LEDPWM	O	Output pin for PWM(Pulse width Modulation) signal of LED driving. If not used, open this pad.
LEDON	O	-Output pad for enabling LED. -If not used, keep it open.

6.4.Other Pins

Pin Name	I/O	Descriptions
TESTI[2:0]	I	Test pin for internal function. If not used, let it open.
TEST_P	O	Test pin for internal function. If not used, let it open.
TEST_N	O	Test pin for internal function. If not used, let it open.
TEST_OSC	O	Test pin for internal function. If not used, let it open.
DUMMYR1 DUMMYR2	-	Test pin for measure ITO resistance. If not used, let it open.
DUMMY	-	Not used. Let it open.

6.5. Maximum layout resistance

Name	Pin Definition	Maximum series resistance	Unit
IOVCC, VCI	Power supply	5	Ω
VSSD, VSSA, AVSS, VSSP	Power supply	5	Ω
VPP	OTP Power supply	20	Ω
IM[3:0]	Input	100	Ω
RESX	Input	100	Ω
CSX, DCX_SCL, RESX	Input	100	Ω
WRX, RDX,	Input	100	Ω
VSYN, HSYN, DE, PCLK	Input	100	Ω
SDA , DB[8:0]	Input/ Output	100	Ω
SDO, TE, LEDPWM, LEDON	Output	100	Ω
TEST_P, TEST_N, TEST_OSC	Output	100	Ω
DUMMY, DUMMYR1, DUMMYR2	Output	100	Ω
T_VDDD	Output	5	Ω
VCOM	Output	5	Ω
AVDD, AVEE	Output	10	Ω
VGH, VGL,	Output	10	Ω

7. Interface setting

7.1. MCU interfaces

JD9853 provides the 8-/9-bit parallel system interface for 8080-I series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit format per pixel color order is selected by COLMOD(3Ah) register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	Interface	Data Bus Selection
0	0	0	0	8080 MCU 8-bit bus interface I	DB[7:0]
0	0	1	0	8080 MCU 9-bit bus interface I	DB[8:0]
0	1	0	1	3-wire 9-bit data serial interface I	SDA: in/out
				2 data lane serial interface	SDA: in/out, WRX:in
0	1	1	0	4-wire 8-bit data serial interface I	SDA: in/out
1	1	0	1	3-wire 9-bit data serial interface II	SDA: in/ SDO: out
1	1	1	0	4-wire 8-bit data serial interface II	SDA: in/ SDO: out

7.1.2. 8080-I Series Parallel Interface

JD9853 can be accessed via 8-/9-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable JD9853 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[8:0] is parallel data bus.

JD9853 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [8:0] bits are display RAM data or command's parameters. When D/CX='0', D[8:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-I Interface selection is done when IM3 pin is low state (VSSC level). Interface bus width can be selected by IM [3:0] bits.

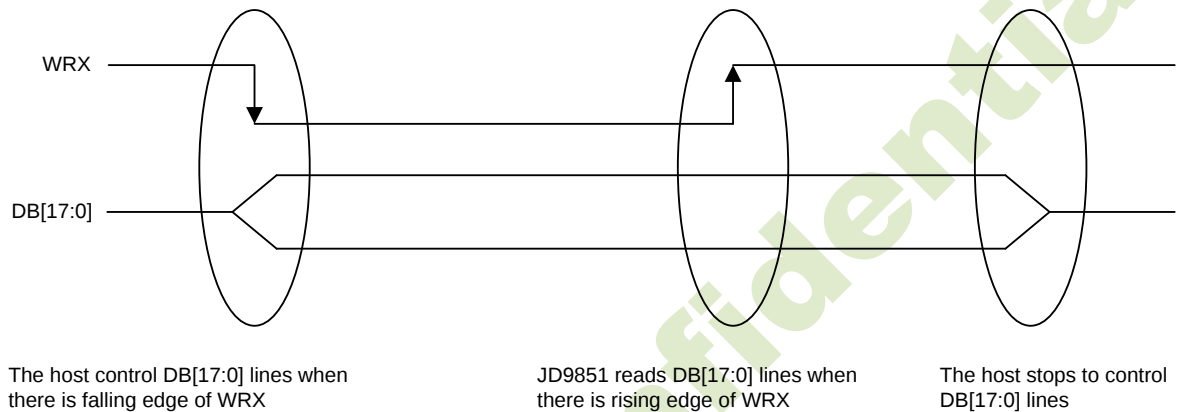
The selection of 8080-I series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	Interface	CSX	D/CX	RDX	WRX	Function
0	0	0	0	8-bit parallel	0	0	1	↑	Write 8-bit command (DB[7:0])
					0	1	1	↑	Write 8-bit display data or 8-bit parameter (DB[7:0])
					0	1	↑	1	Read 8-bit display data (DB[7:0])
					0	1	↑	1	Read 8-bit parameter or status (DB[7:0])
0	0	1	0	9-bit parallel	0	0	1	↑	Write 8-bit command (DB[7:0])
					0	1	1	↑	Write 9-bit display data or 8-bit parameter (DB[8:0])
					0	1	↑	1	Read 9-bit display data (DB[8:0])
					0	1	↑	1	Read 8-bit parameter or status (DB[7:0])

7.1.2.1. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is GRAM data or command's parameter.

The following figure shows a write cycle for the 8080-I MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure. 7.1 8080-Series WRX Protocol

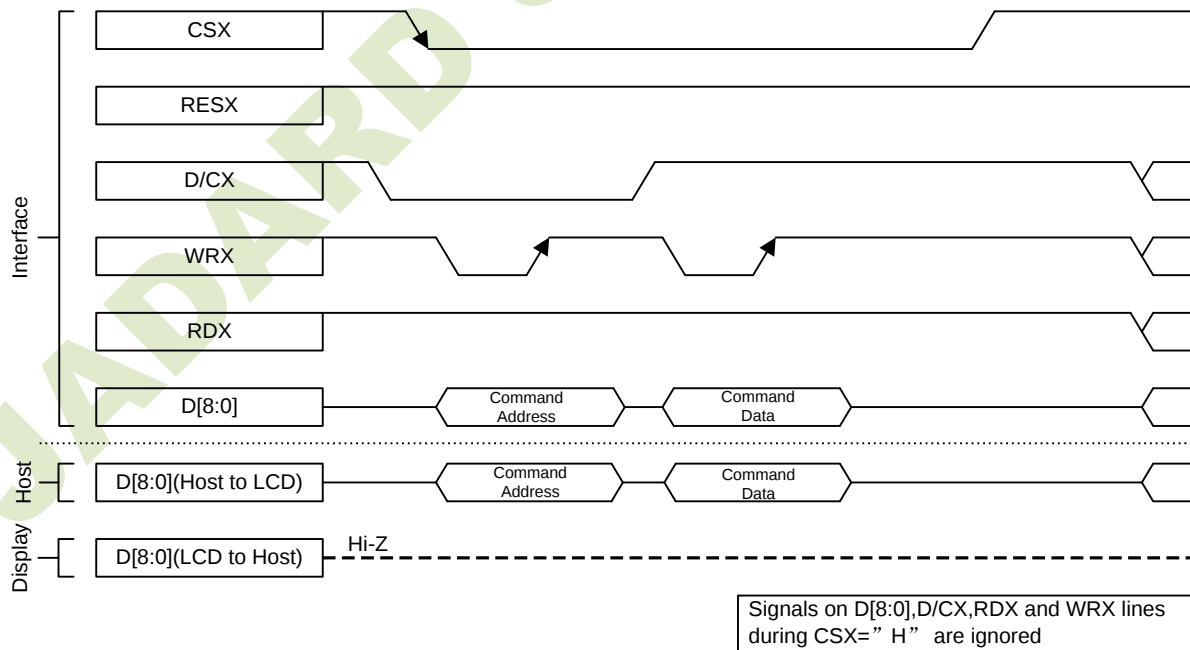
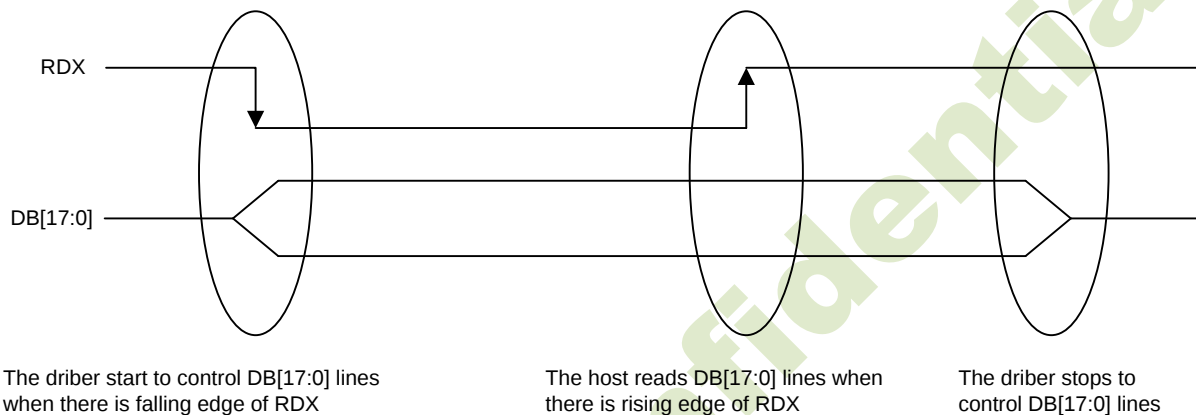


Figure. 7.2 8080-Series Parallel Bus Protocol, Write Register or Display RAM

7.1.2.2. Read Cycle Sequence

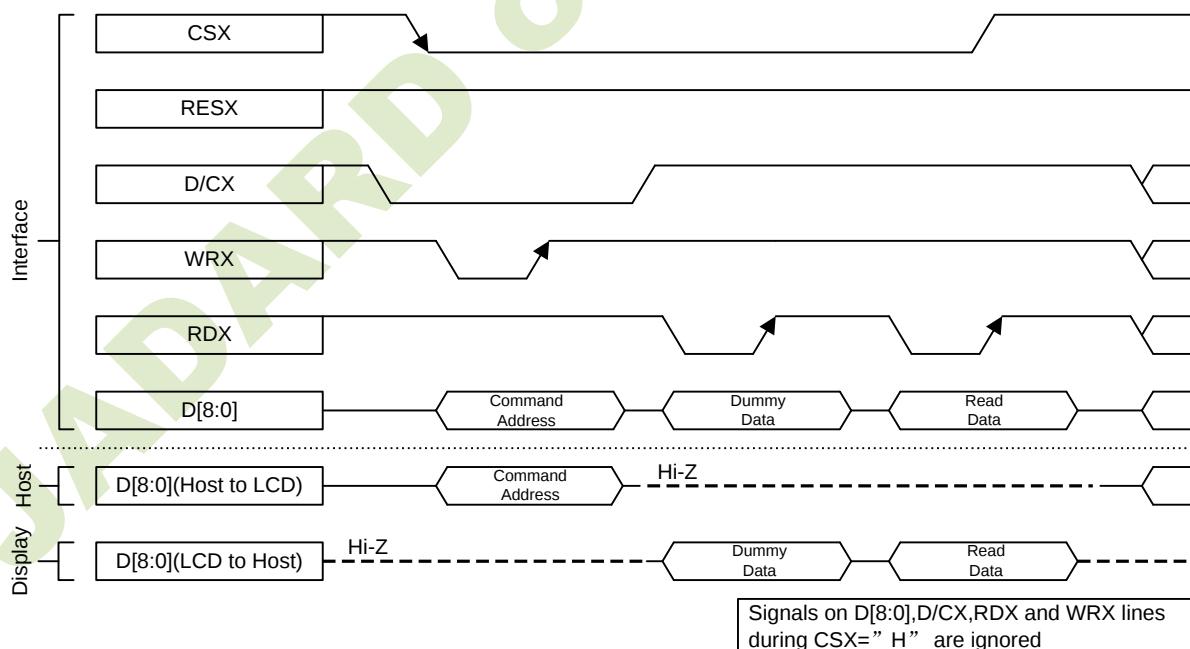
The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-I MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped)

Figure. 7.3 8080-Series RDX Protocol



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

Figure. 7.4 8080-Series Parallel Bus Protocol, Read Register or Display RAM

7.1.3. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	Read back selection
0	1	0	0	Quad serial interface	Via the read instruction
0	1	0	1	3-line serial interface	
0	1	1	0	4-line serial interface	
1	1	0	1	3-line serial interface	
1	1	1	0	4-line serial interface	

JD9853 supplies 3-lines/ 9-bit and 4-line/8-bit and Quad serial interfaces for communication between host and JD9853.

The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission.

The Quad serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA), input(DB[0],DB[1],DB[2]).

The data bus (D [8:0]), which are not used, must be connected to IOVCC or GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.3.1. Pin Description

3-line serial interface I

Pin Name	Description
CSX	Chip selection signal
DCX_SCL	Clock signal
SDA	Serial input/output data

4-line serial interface I

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high
DCX_SCL	Clock signal
SDA	Serial input/output data

3-line serial interface II

Pin Name	Description
CSX	Chip selection signal
DCX_SCL	Clock signal
SDA	Serial input data
SDO	Serial output data

4-line serial interface II

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high
DCX_SCL	Clock signal
SDA	Serial input data
SDO	Serial output data

Quad serial interface

Pin Name	Description
CSX	Chip selection signal
DCX_SCL	Clock signal
SDA	Serial input/output data
DB[2:0]	input data

7.1.3.2. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to JD9853. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to JD9853 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

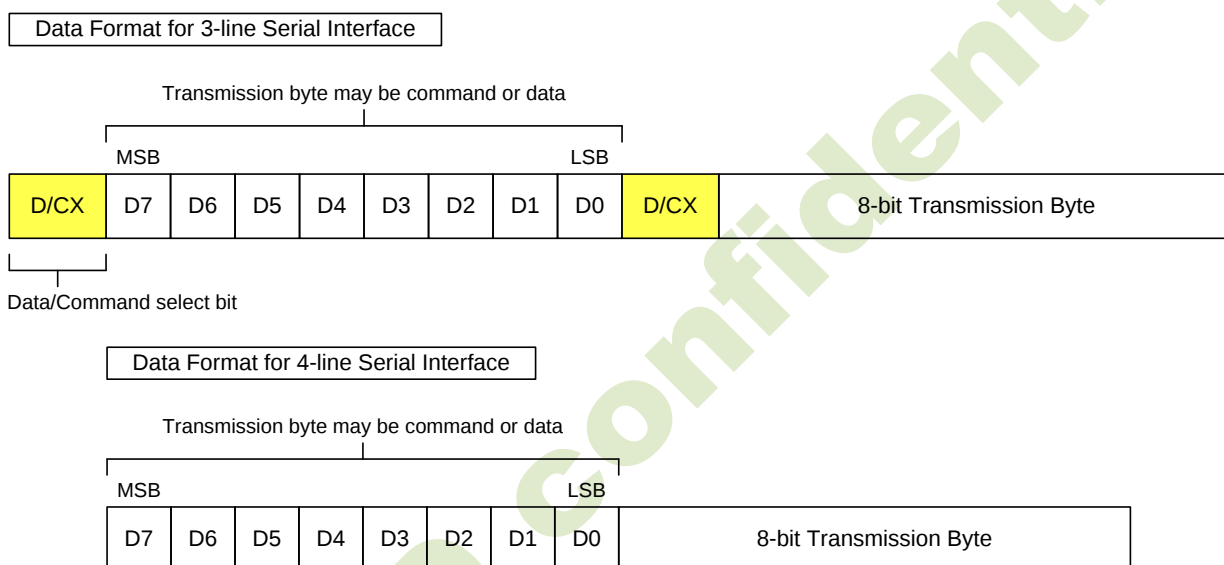


Figure. 7.5 Serial interface data stream format

Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by JD9853 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

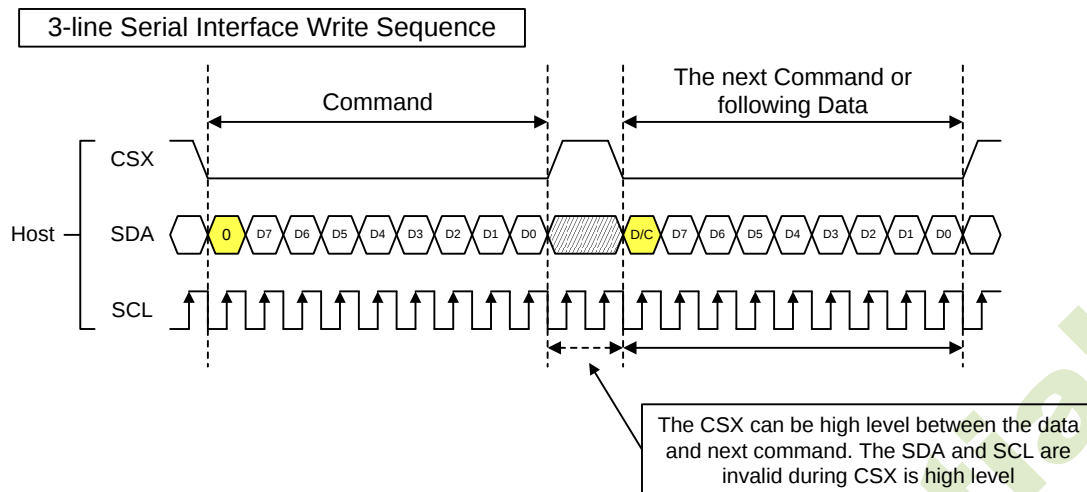


Figure. 7.6 3-line serial interface write protocol

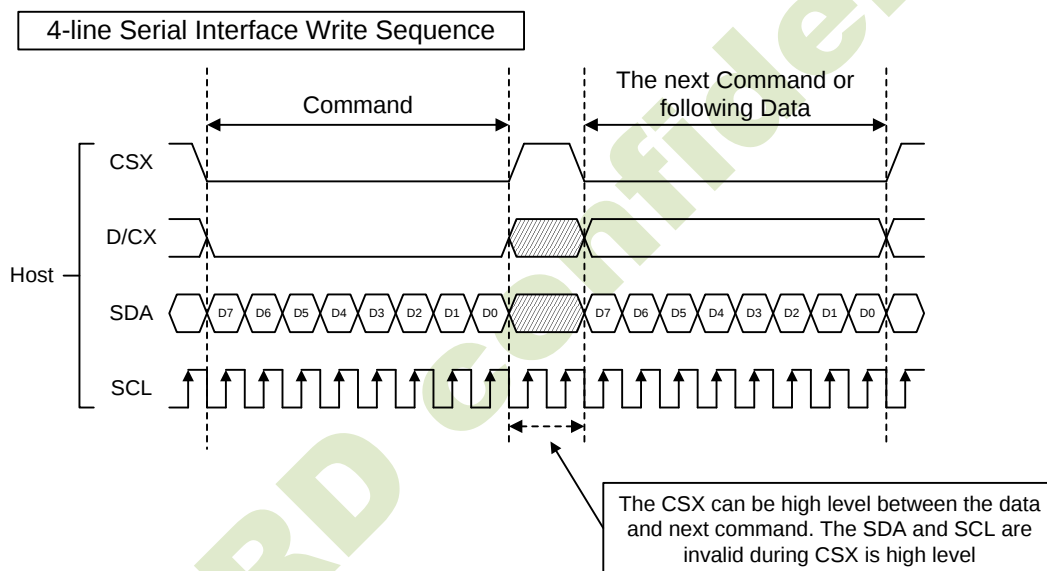


Figure. 7.7 4-line serial interface write protocol

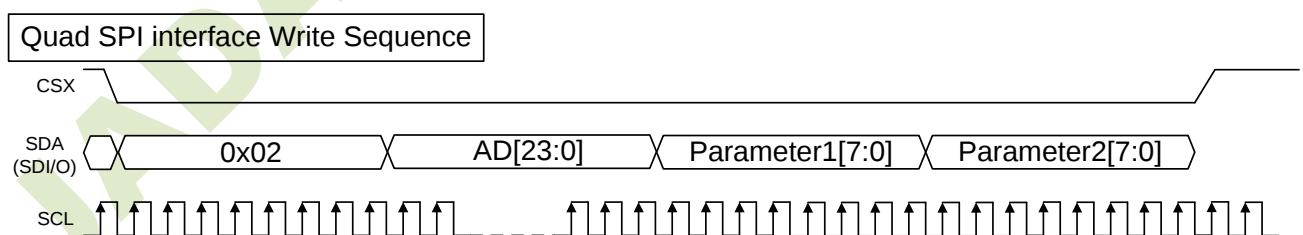


Figure. 7.8 Quad serial interface write protocol

7.1.3.3. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from JD9853. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. JD9853 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according to command code.

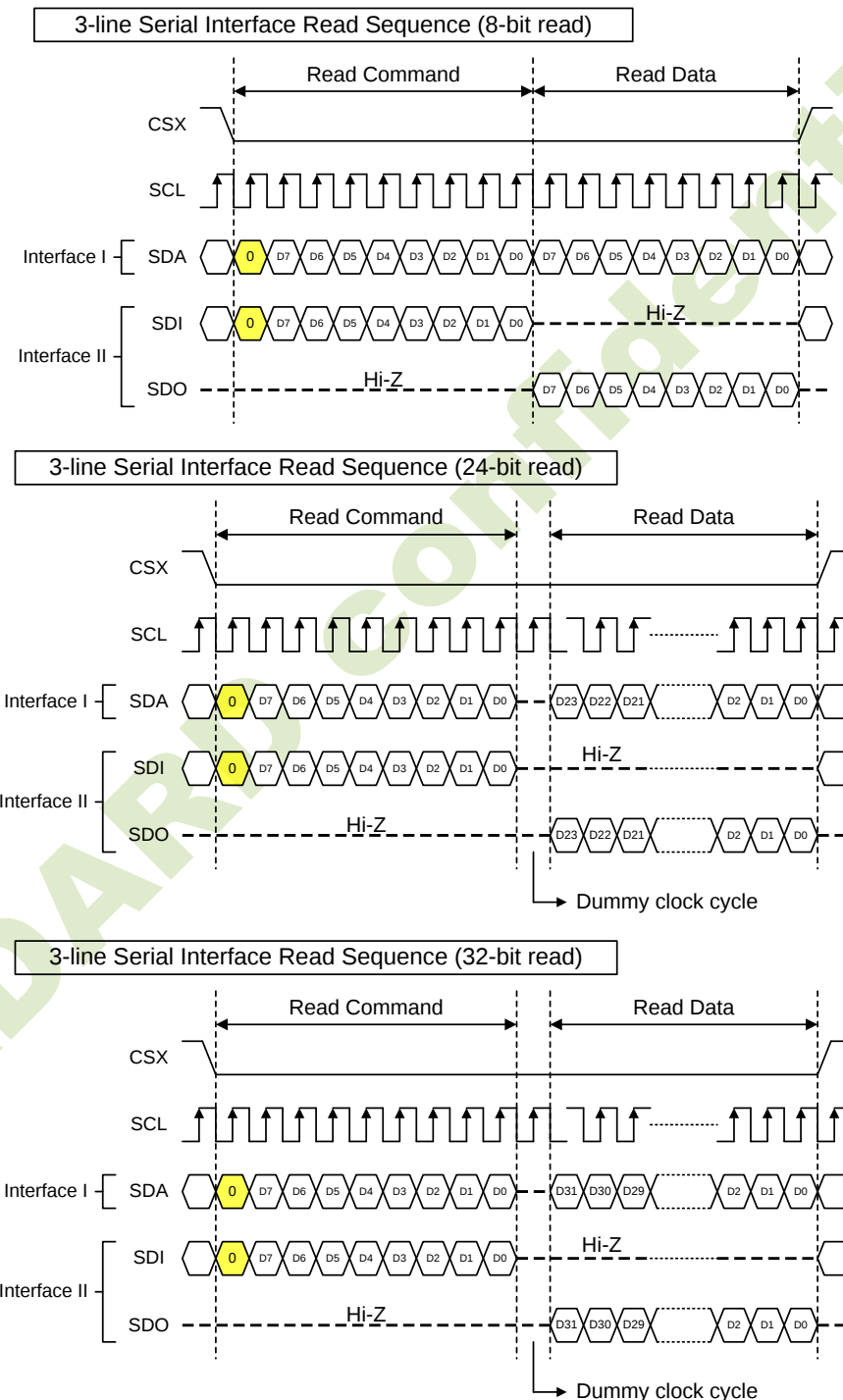


Figure. 7.9 3-line serial interface read protocol

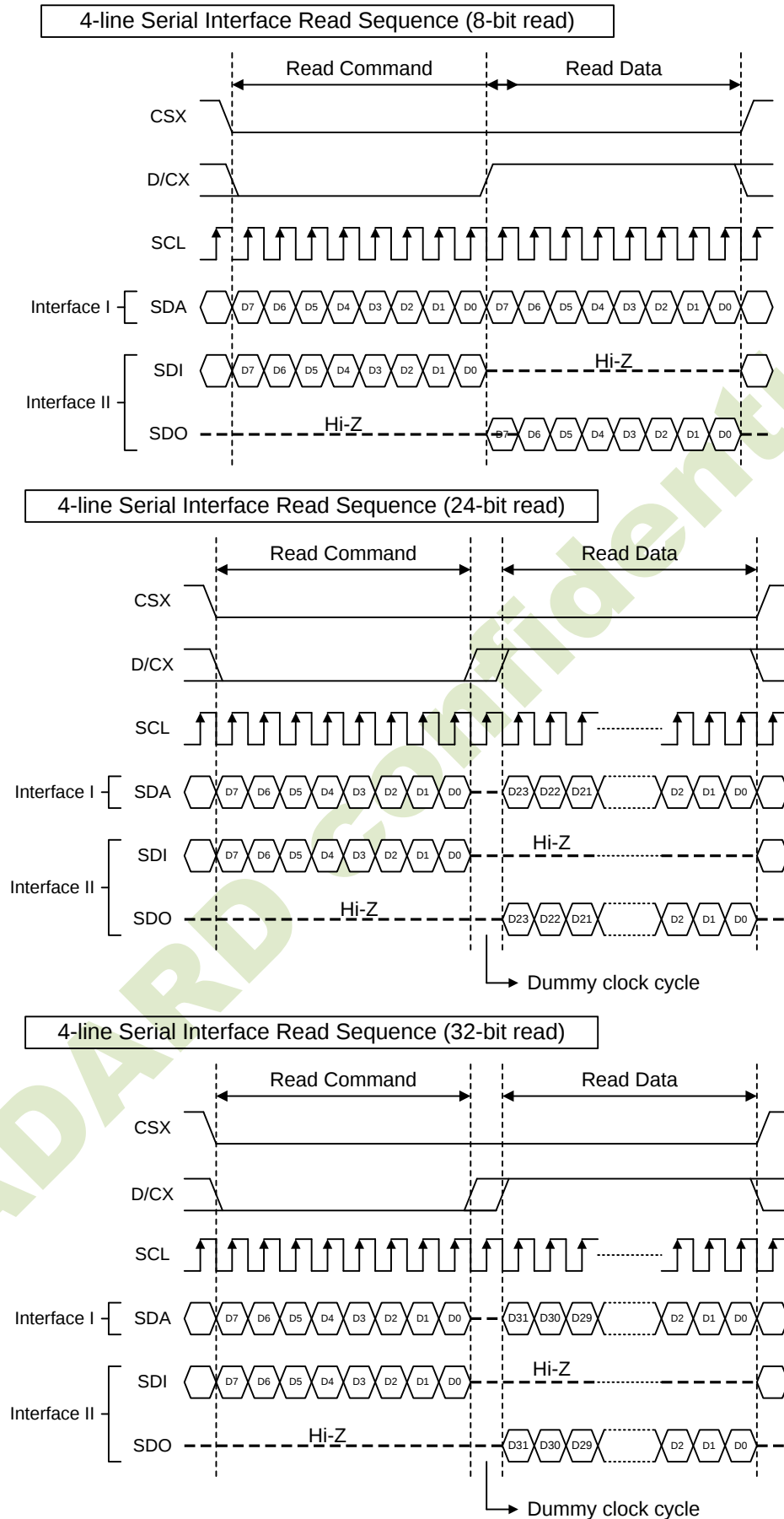


Figure. 7.10 4-line serial interface read protocol

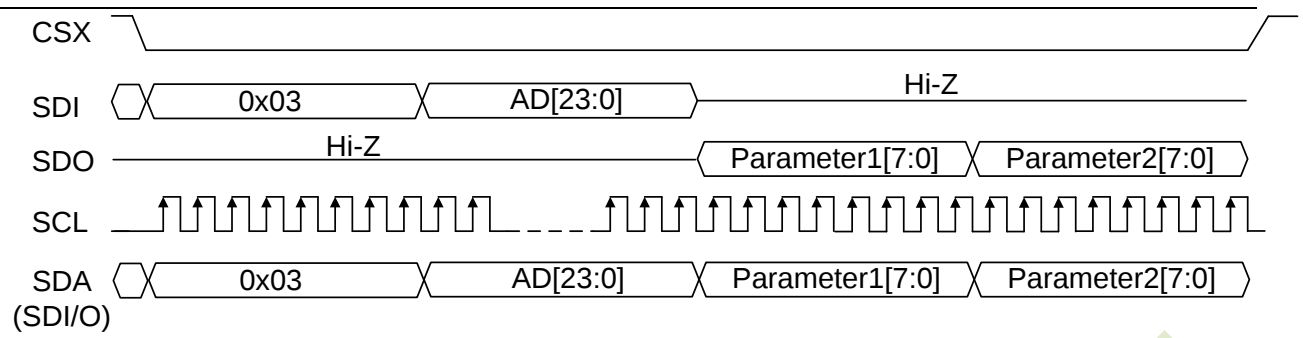


Figure. 7.11 Quad serial interface read protocol

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7.1.4. 2 Data Lane Interface

IM3	IM2	IM1	IM0	MCU-Interface Mode	Read back selection
0	1	0	1	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bitread)

To enter this interface, command D7h need set 20h.

7.1.4.1. Write Cycle Sequence

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of WRX.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

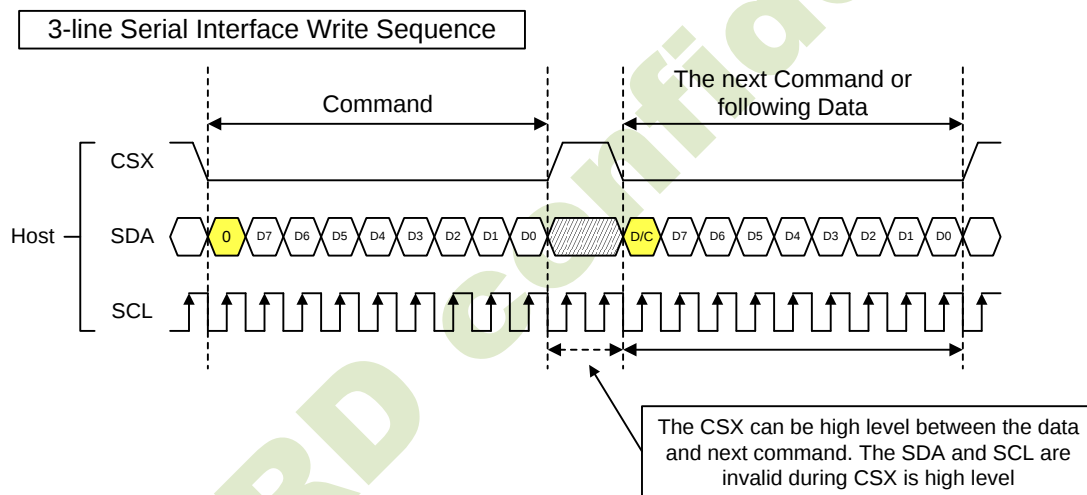


Figure. 7.12 3-line serial interface write protocol

7.1.4.2. Read Cycle Sequence

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and WRX pin can be ignored.

To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

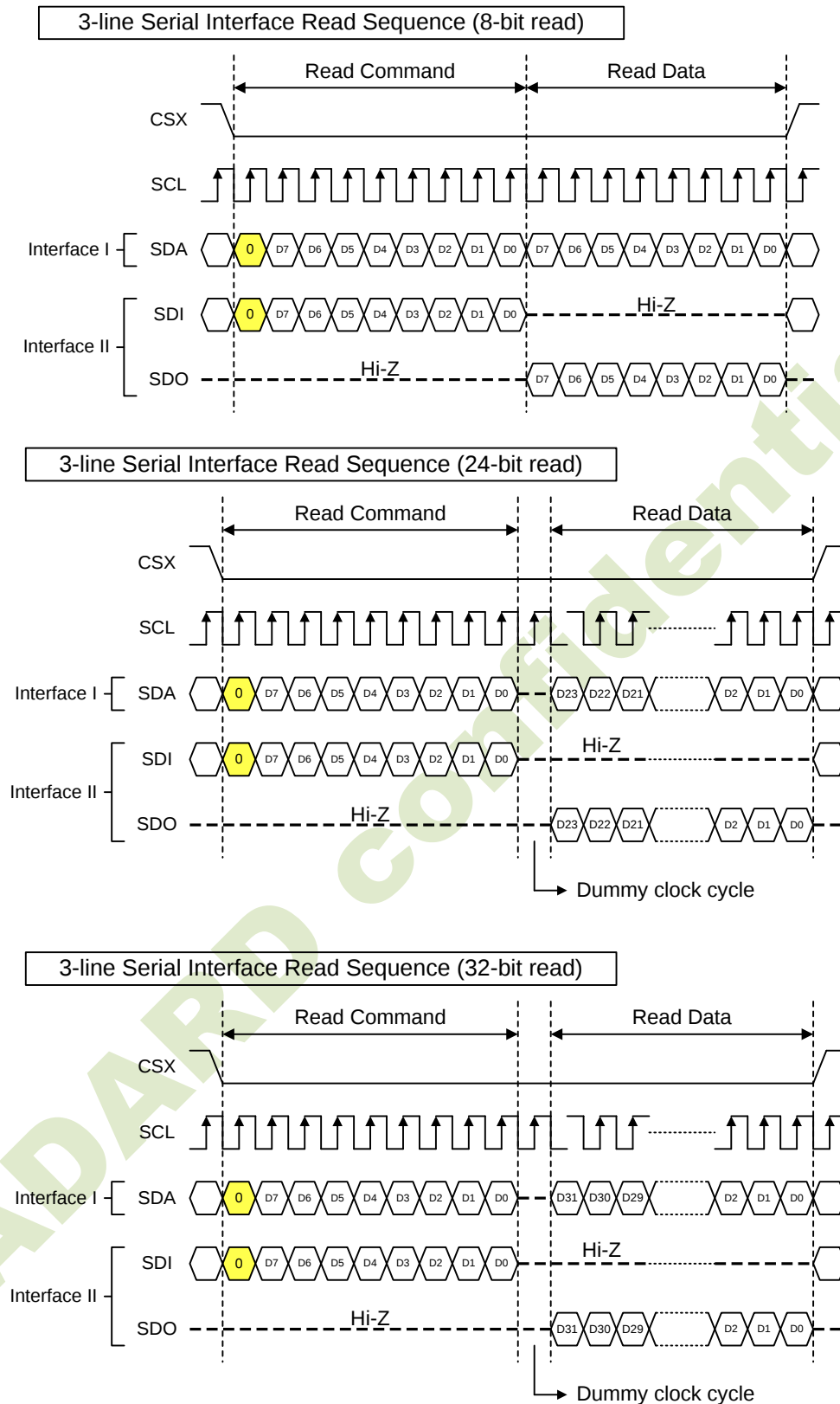
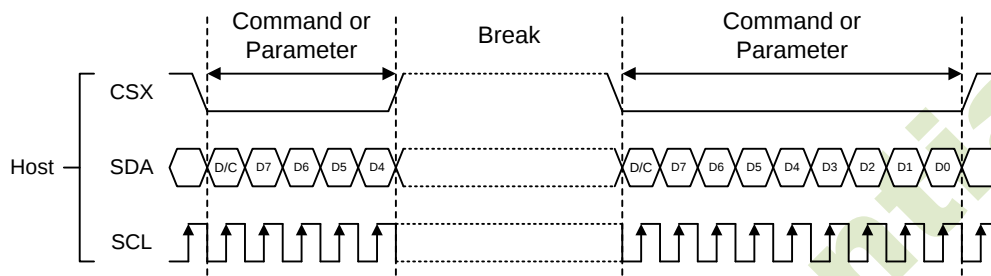


Figure. 7.13 3-line serial interface read protocol

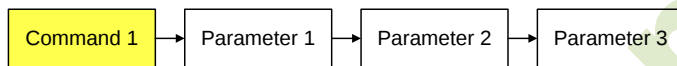
7.1.5.Data Transfer Break and Recovery

If there is a break in data transmission while transferring a Command or Parameter or Frame Memory Data before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (CSX) is next activated. See the following example:



If a 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

Without Break



With Break

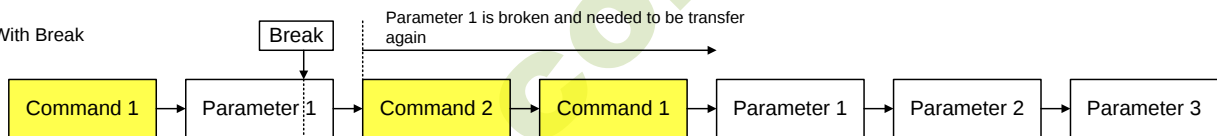


Figure. 7.14 Write interrupts recovery, case 1

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

With Break

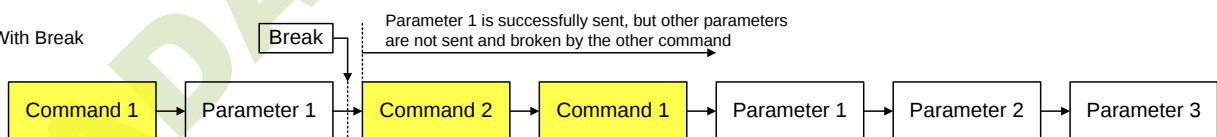


Figure. 7.15 Write interrupts recovery, case 2

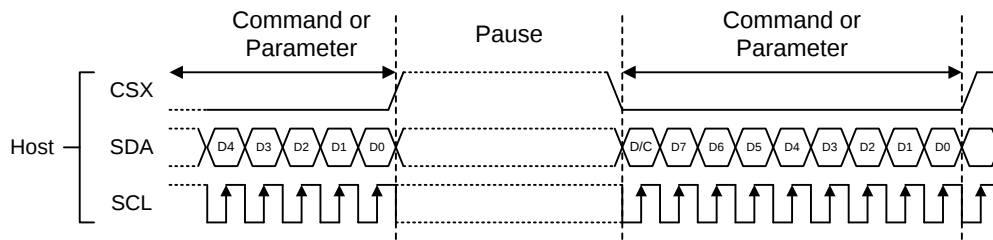
7.1.6.Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then JD9853 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

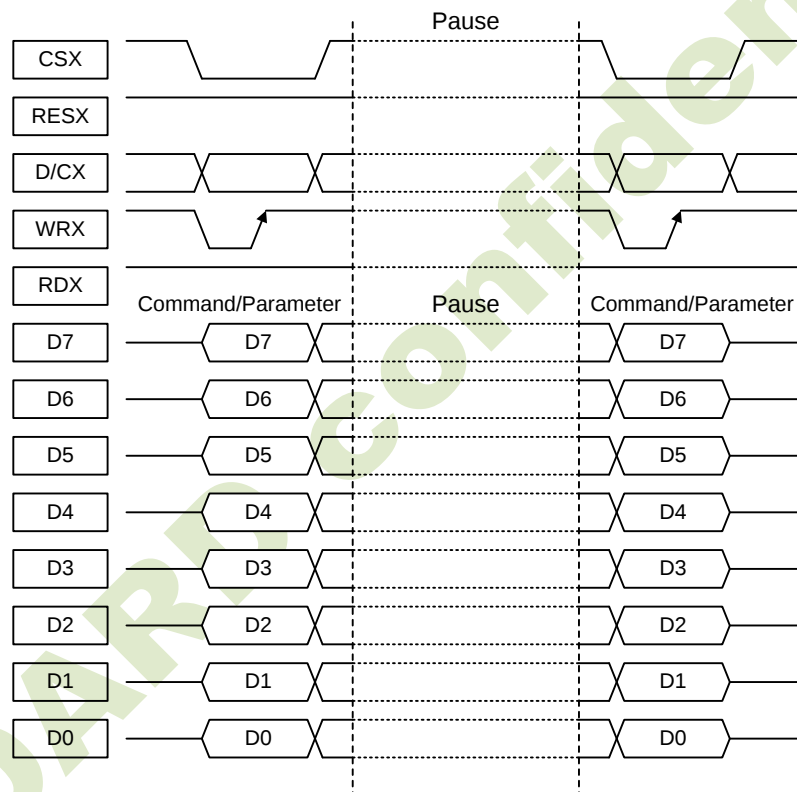
This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

7.1.6.1. Serial Interface Pause



7.1.6.2. Parallel Interface Pause

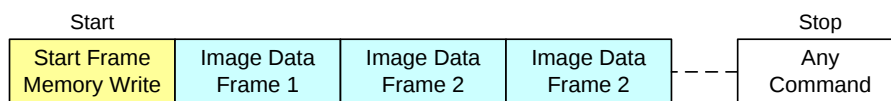


7.1.7.Data Transfer Mode

JD9853 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

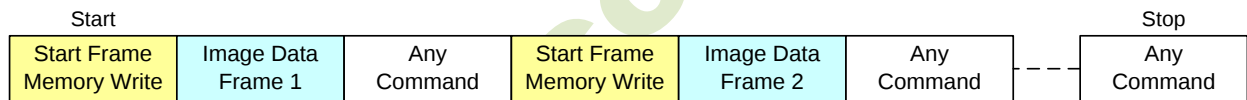
7.1.7.1. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.7.2. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.1.8. Display Module Data Color Coding

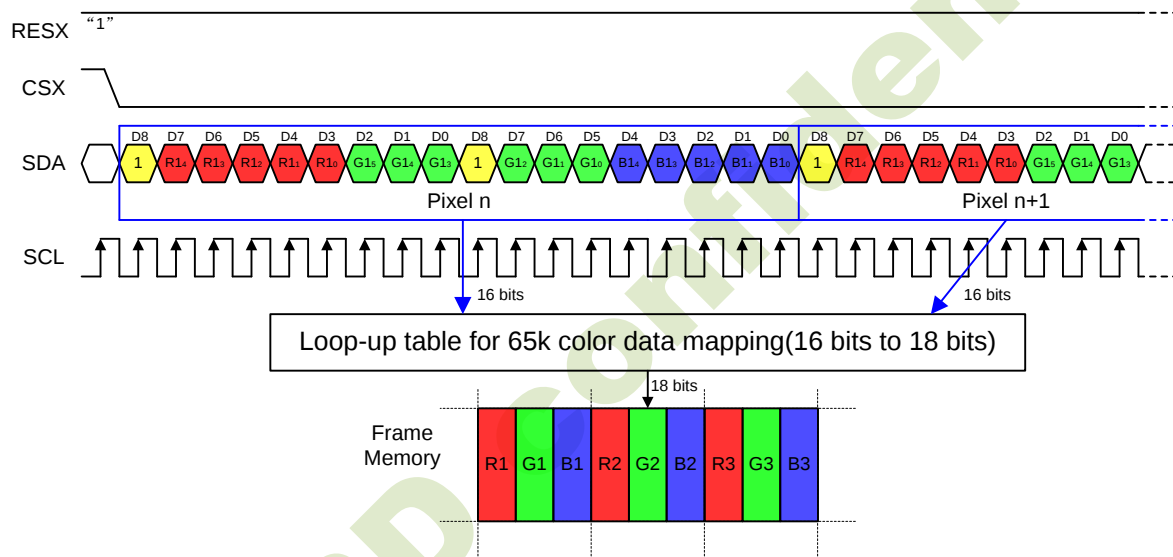
7.1.8.1. 3-Line Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

7.1.8.1.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

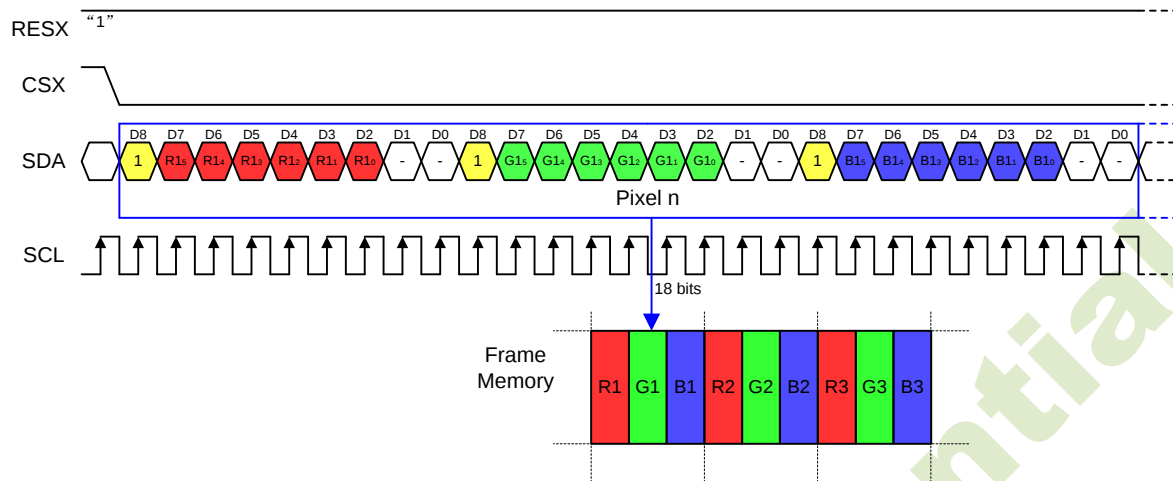


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.1.8.1.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h")



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

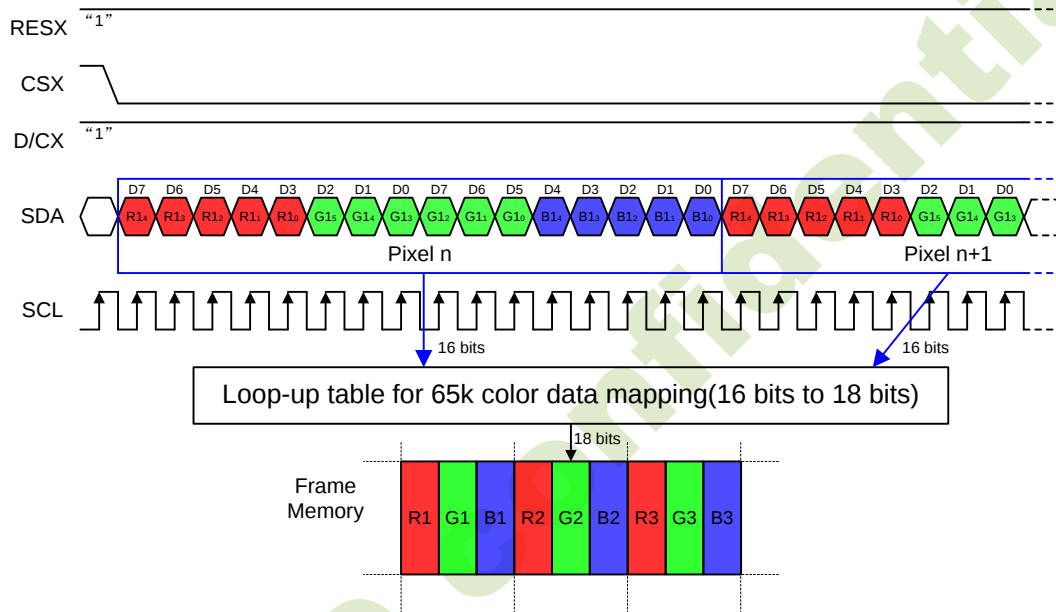
7.1.8.2. 4-Line Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

7.1.8.2.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

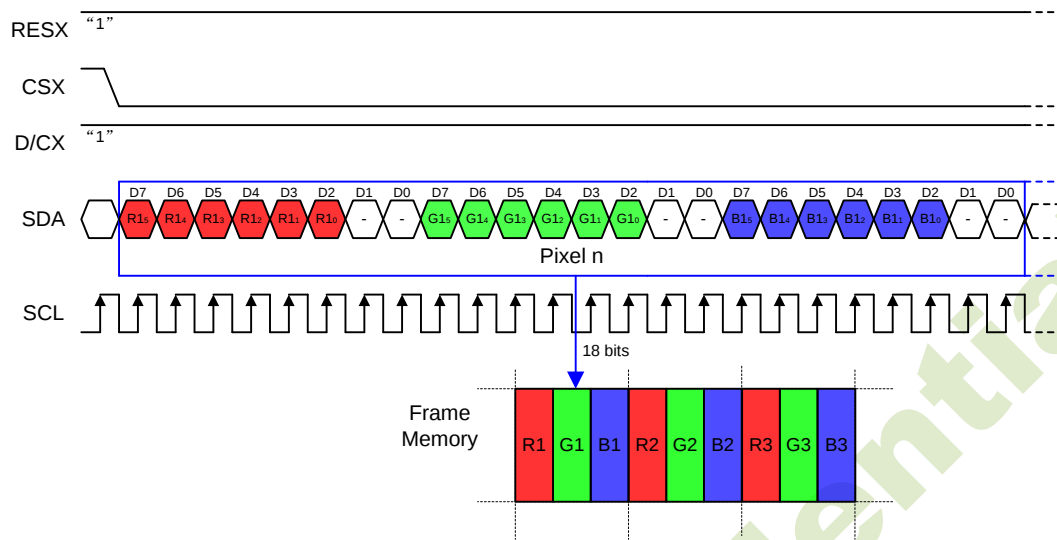


Note 1. pixel data with the 16-bit color depth information

Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

7.1.8.2.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h")



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

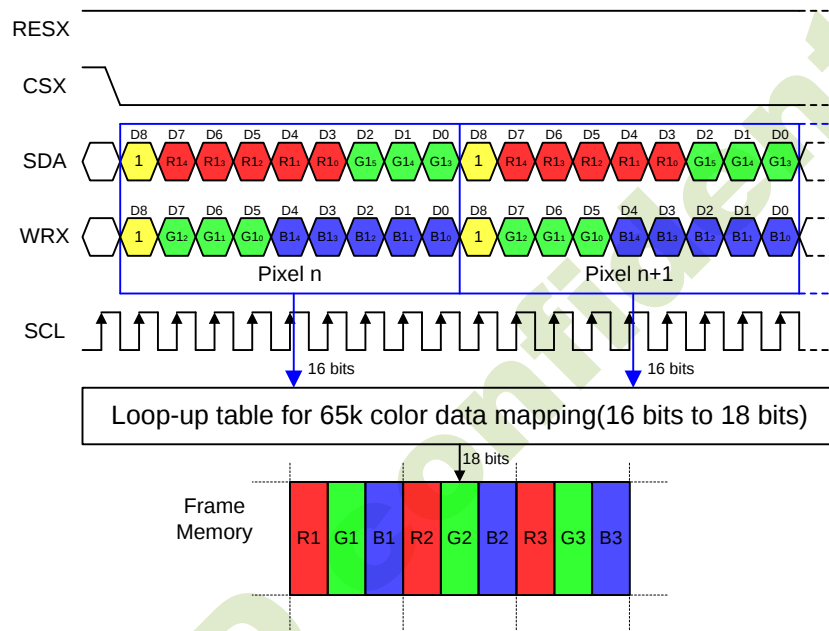
7.1.8.3. 2 Data Lane Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

7.1.8.3.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

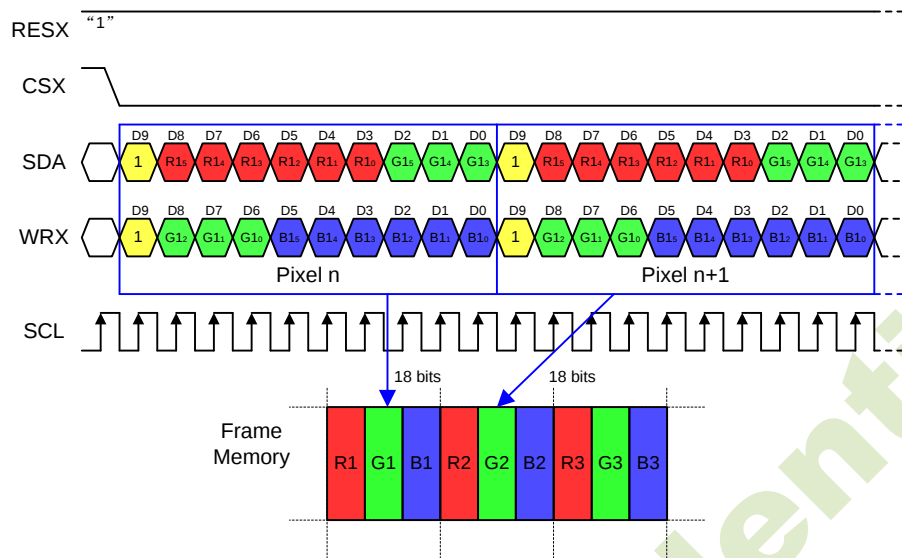


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.1.8.3.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h")



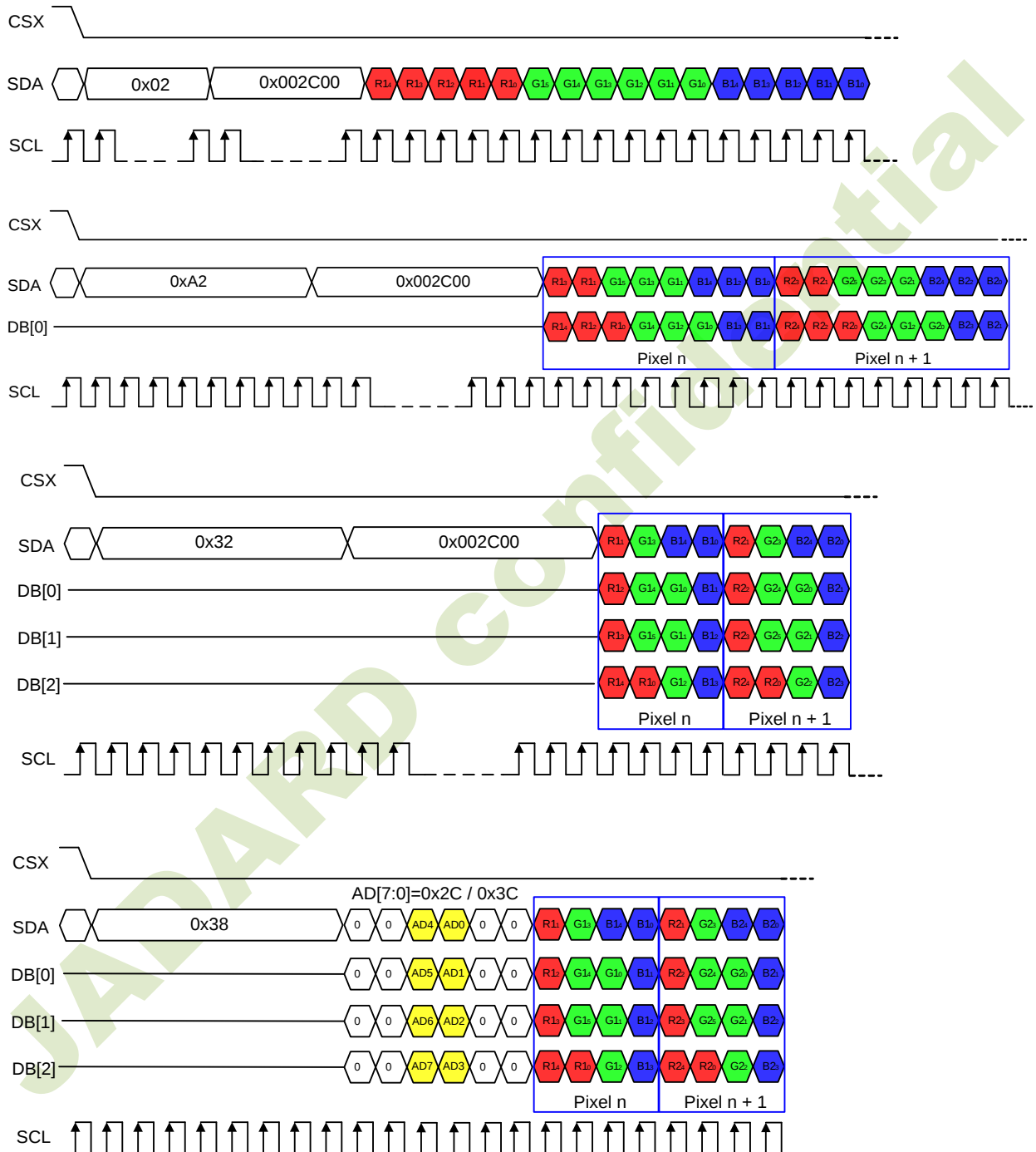
Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

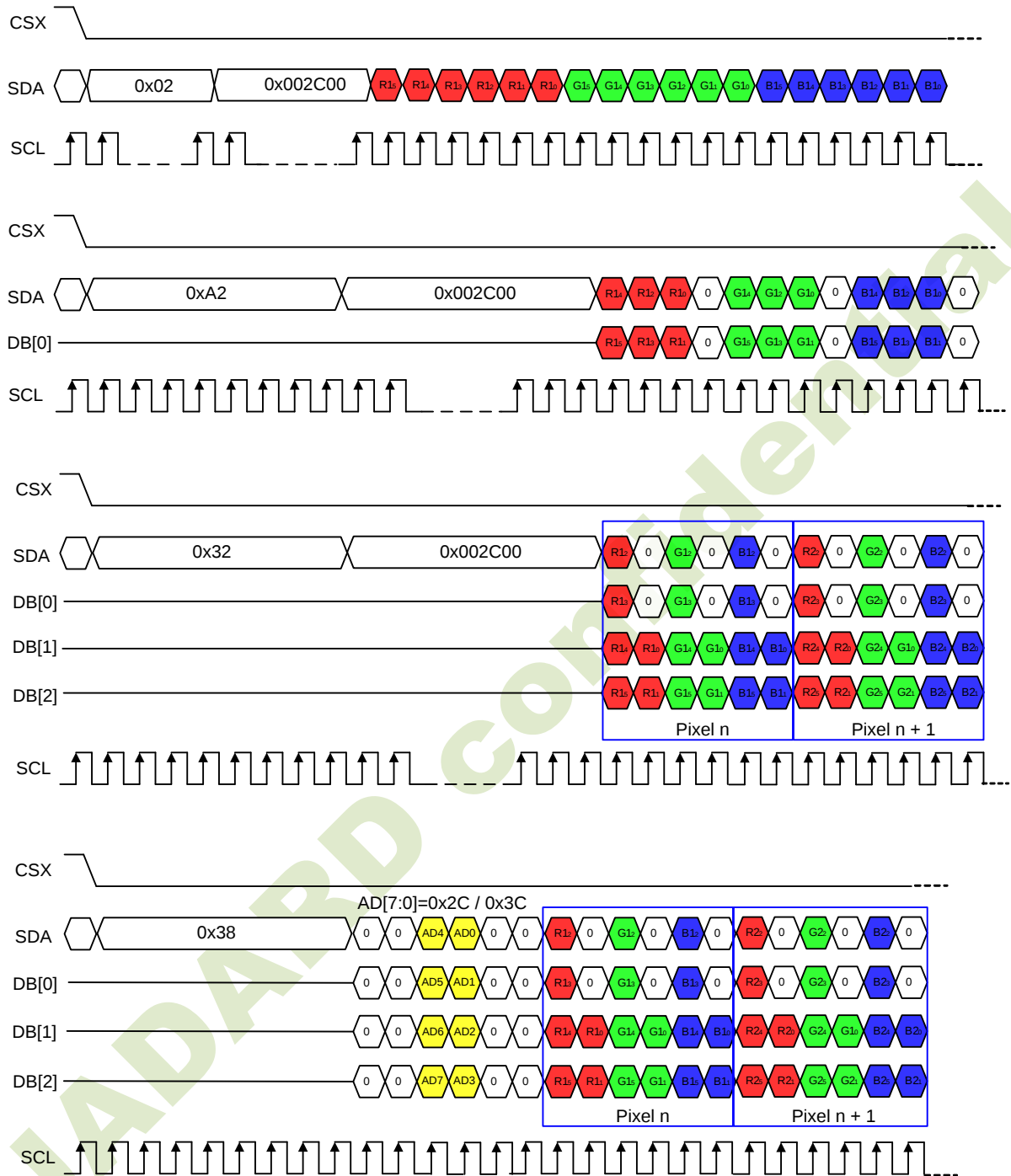
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.1.8.4. Quad SPI (QSPI) Data interface

7.1.8.4.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")



7.1.8.4.2. R 6-bit, G 6-bit, B 6-bit, 65,536 colors (3Ah="06h")

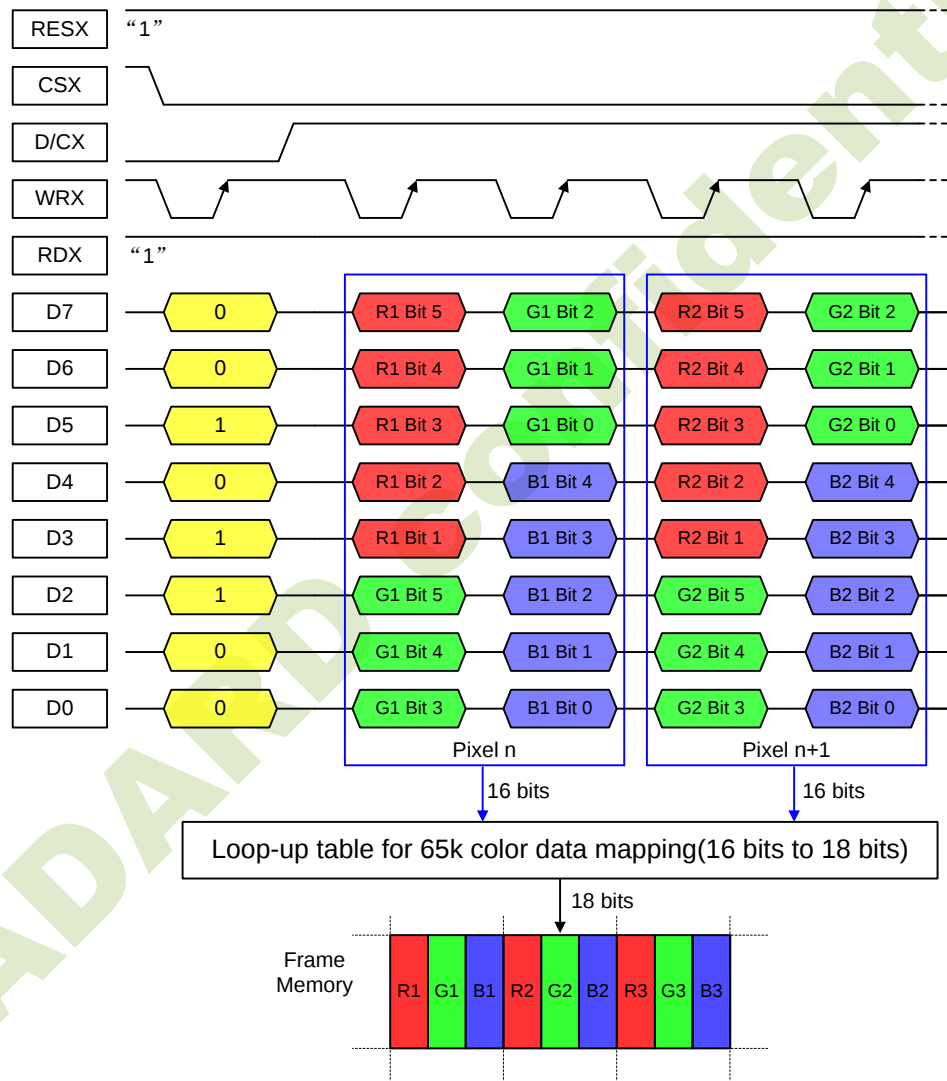


7.1.8.5. 8080-I series 8-bit Parallel Interface

The 8080-I series 8-bit parallel interface of JD9853 can be used by setting IM[3:0]="0000b". Different display data formats are available for three Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

7.1.8.5.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

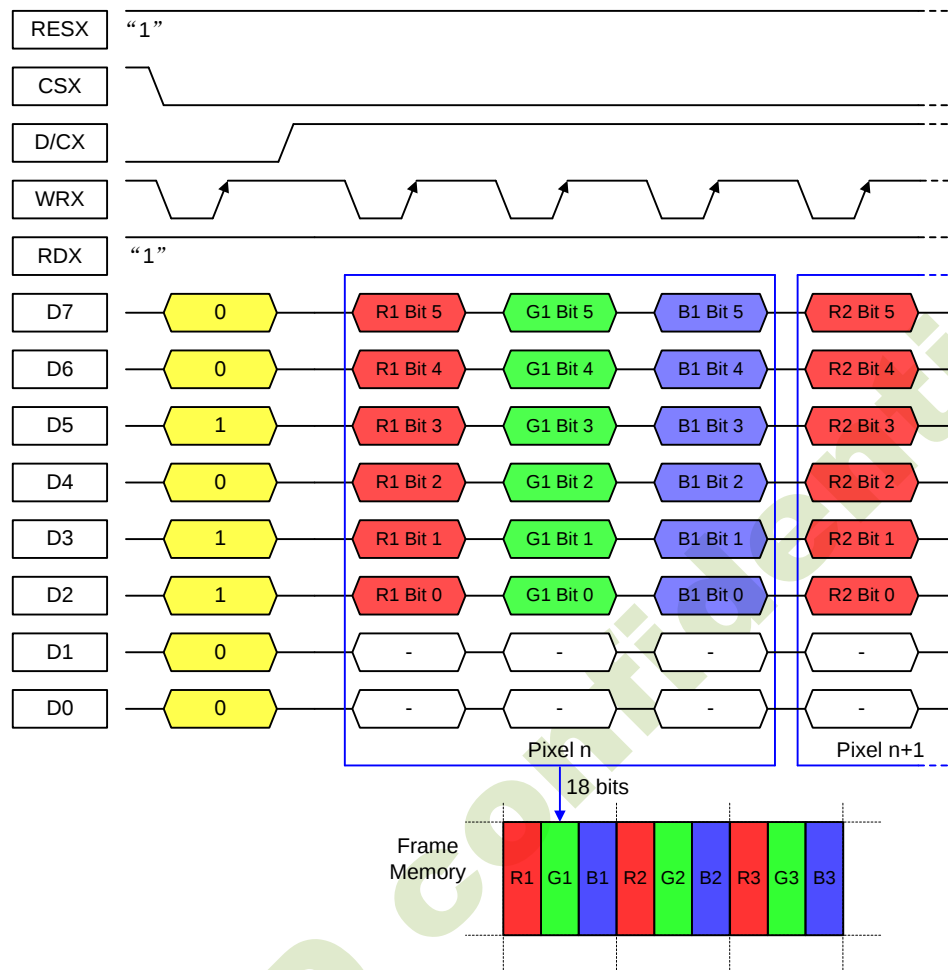


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.1.8.5.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h")



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

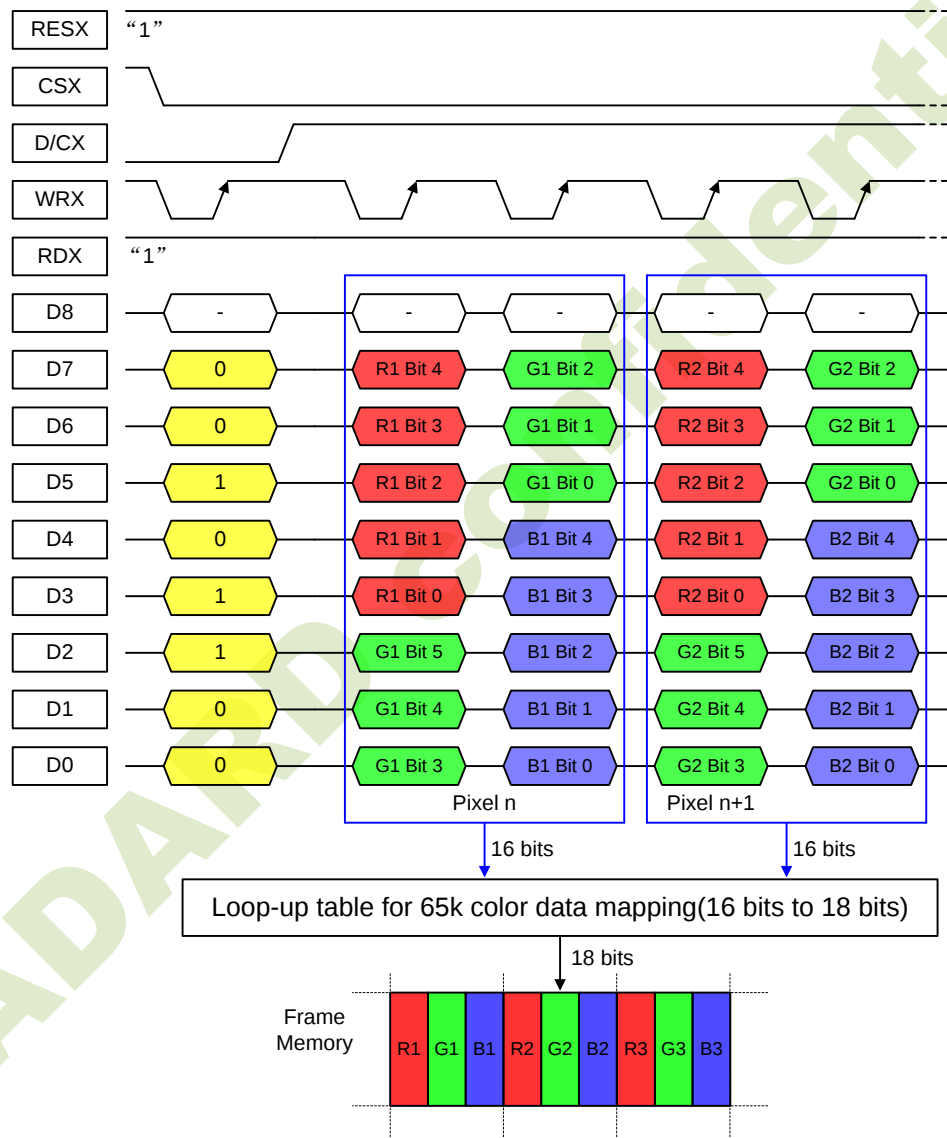
7.1.8.6. 8080-I series 9-Bit Parallel Interface

The 8080-I series 9-bit parallel interface of JD9853 can be used by setting IM[3:0]="0010b". Different display data formats are available for two colors depth supported by listed below.

65k colors, RGB 5,6,5-bit input

262k colors, RGB 6,6,6-bit input

7.1.8.6.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

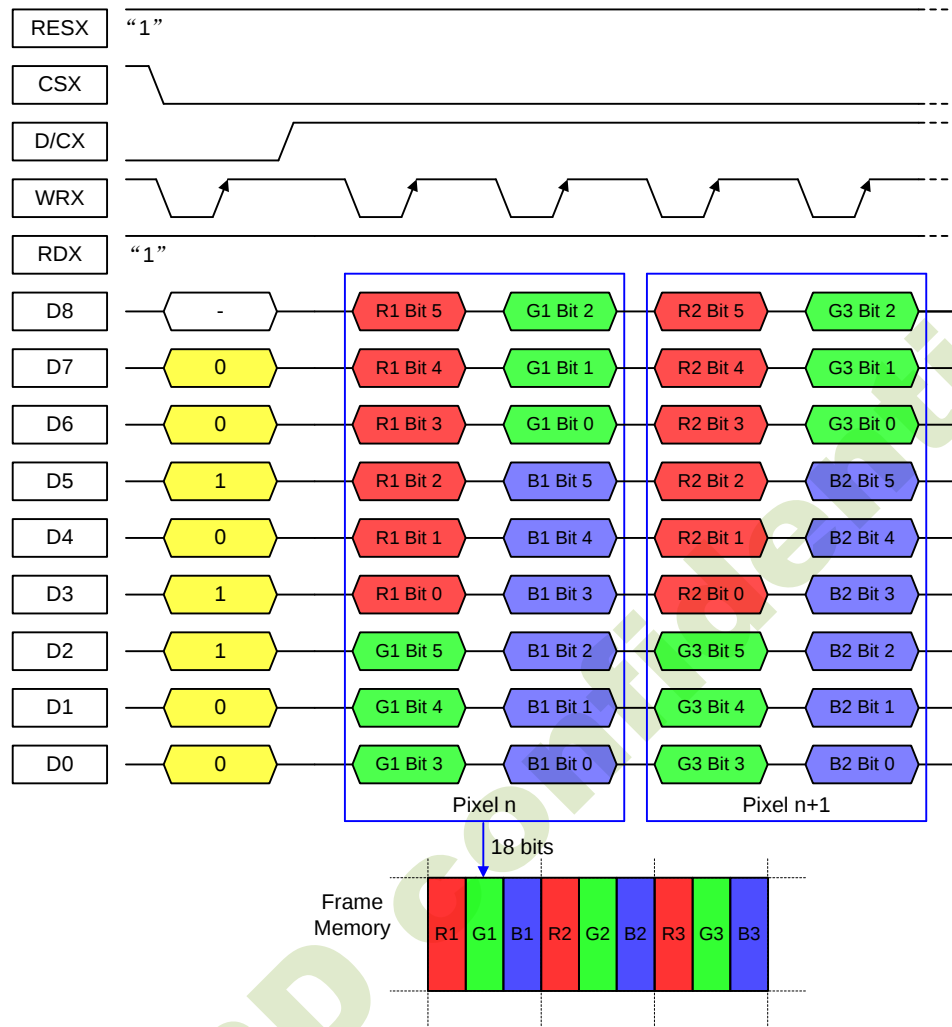


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.1.8.6.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h, MDT="00b")

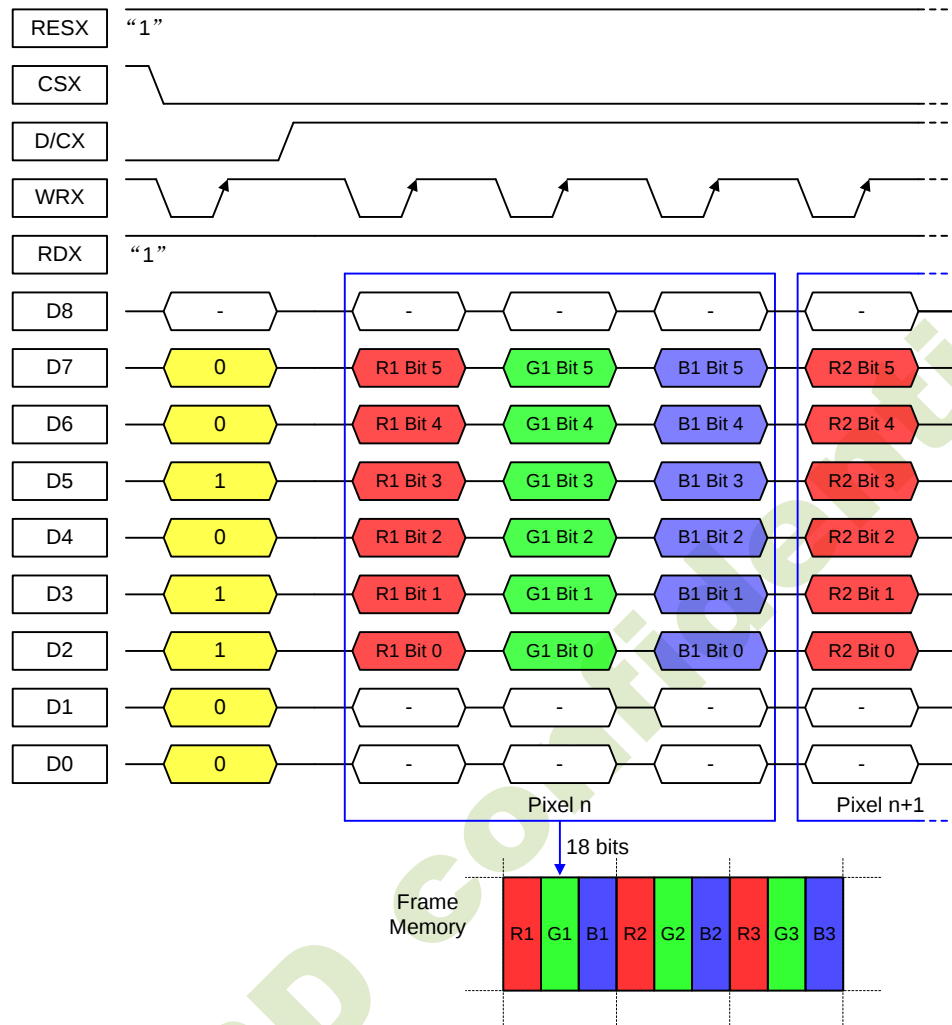


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.1.8.6.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h, MDT="01b")



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2. RGB Interface

7.2.1. RGB Interface Selection

The color format selection of RGB Interface for JD9853 is selected by setting the RGB_SEL[1:0] and command 3Ah, DB[6:4].

RGB_SEL[1:0]	3Ah, DB[6:4]	RGB Interface Mode	Data pins
11	110	6-bit 262K RGB Interface	DB[5:0]
11	101	6-bit 65K RGB Interface	DB[5:0]

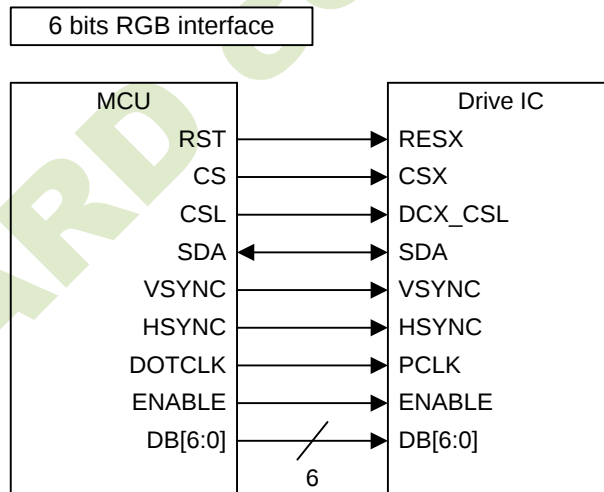
7.2.2. RGB Color Format

JD9853 supports two kinds of RGB interface, DE mode and HV mode, and 6bit/18bit data format.

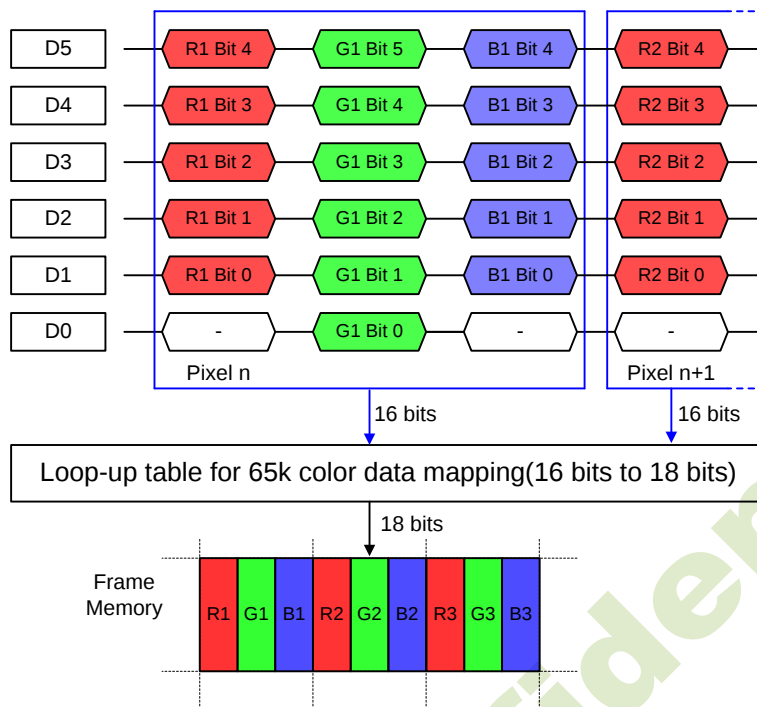
When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[8:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[8:0] pins can be used. When using RGB interface, only serial interface can be selected.

7.2.2.1. 6-bit RGB interface

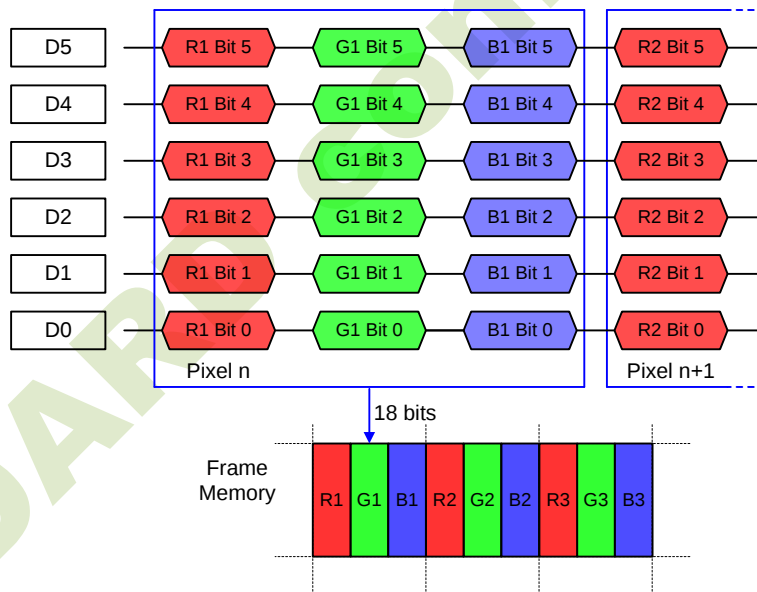
6-bit RGB interface hardware suggestion, IM[3:0]=0101, RGB_SEL[1:0]=11.



Write data for 6-bit/pixel (RGB 5-6-5-bit input), 65K-Colors

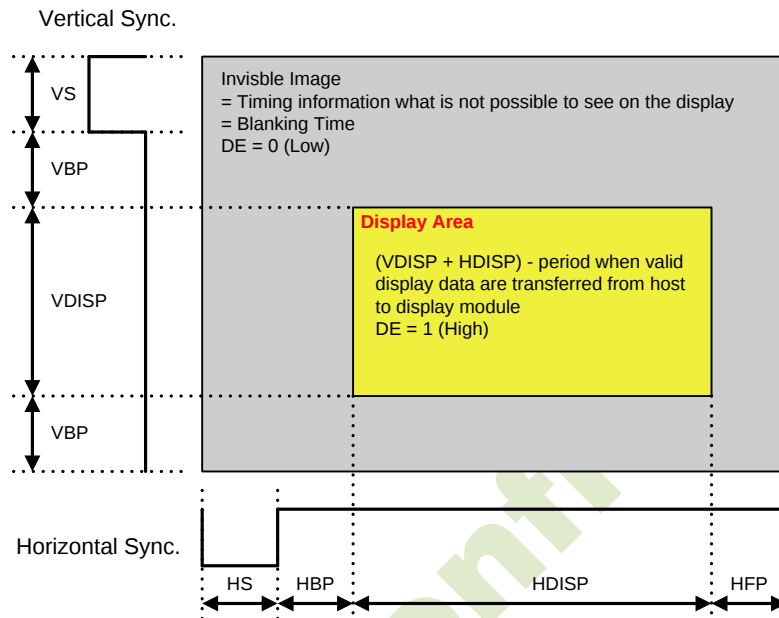


Write data for 6-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



7.2.3. RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



Please refer to the following table for the setting limitation of RGB interface signals.

6 bit RGB interface

Parameters	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	HS	6	12	HS+HBP=252	Clock
Horizontal Sync. Back Porch	HBP	12	24		Clock
Horizontal Sync. Front Porch	HFP	6	12	-	Clock
Vertical Sync. Width	VS	1	2	VS+VBP=126	Line
Vertical Sync. Back Porch	VBP	1	10		Line
Vertical Sync. Front Porch	VFP	1	10	-	Line

Note: HS/HBP/HFP must be (Min + n*3) Clock

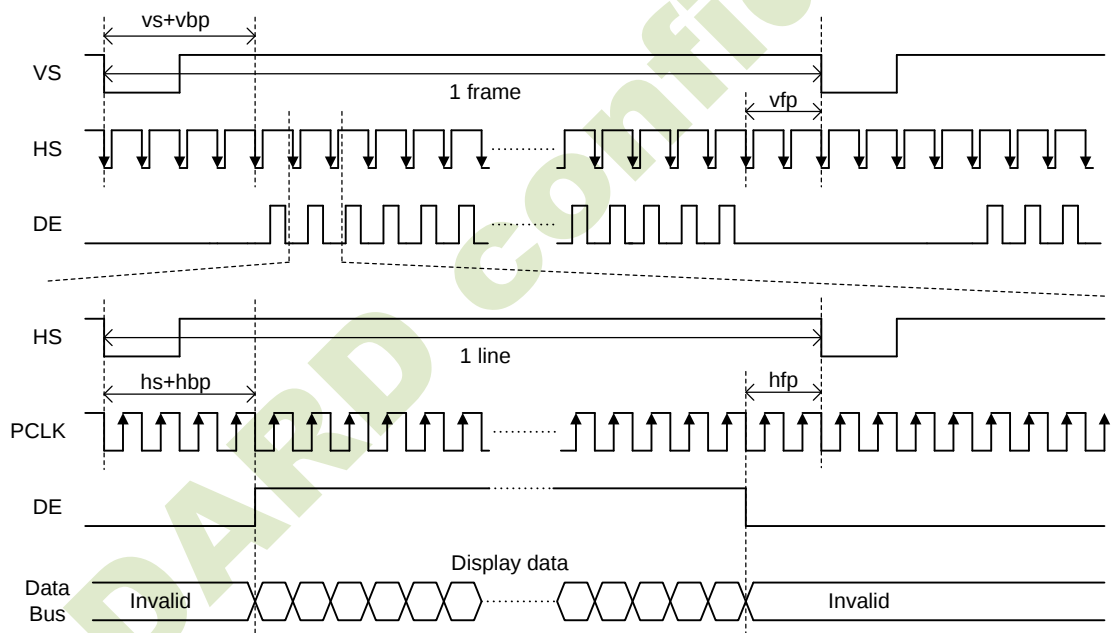
7.2.4. RGB Mode Selection

JD9853 supports two kinds of RGB interface, DE mode and HV mode. Each mode also can select with ram and without ram. The table shown below uses command B1h to select RGB interface mode.

DEM	DM[1:0]	RGB mode	Data Path
0	00	DE mode	Ram
0	11		Shift register (without Ram)
1	00	HV mode	Ram
1	11		Shift register (without Ram)

7.2.5. RGB Interface Timing

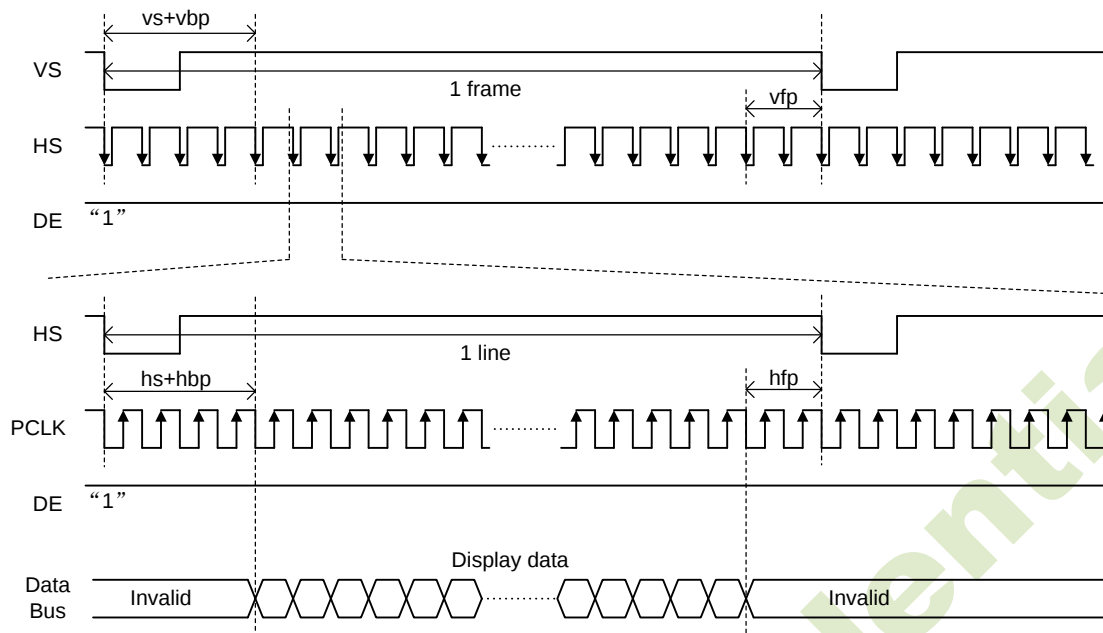
The timing chart of RGB interface DE mode is shown as follows



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure. 7.16 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure. 7.17 Timing chart of RGB interface HV mod

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals.

In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

7.3. VSYNC Interface

JD9853 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-I/8080-II system interface. When the VSYNC interface is selected to display a moving picture, the minimum RAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "1".

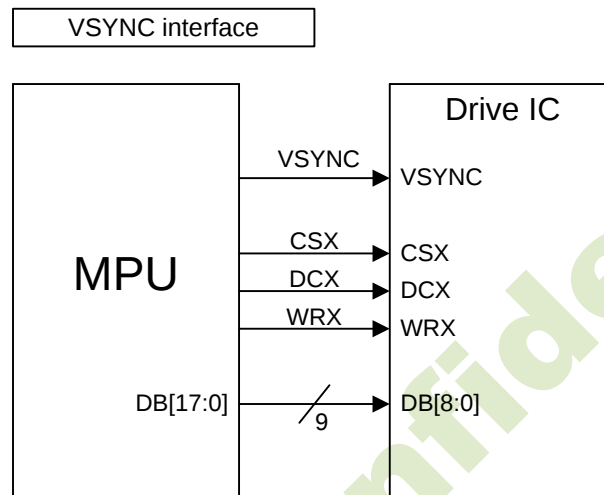


Figure. 7.18 Data transmission through VSYNC interface

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

7.3.1.VSYNC Interface Mode

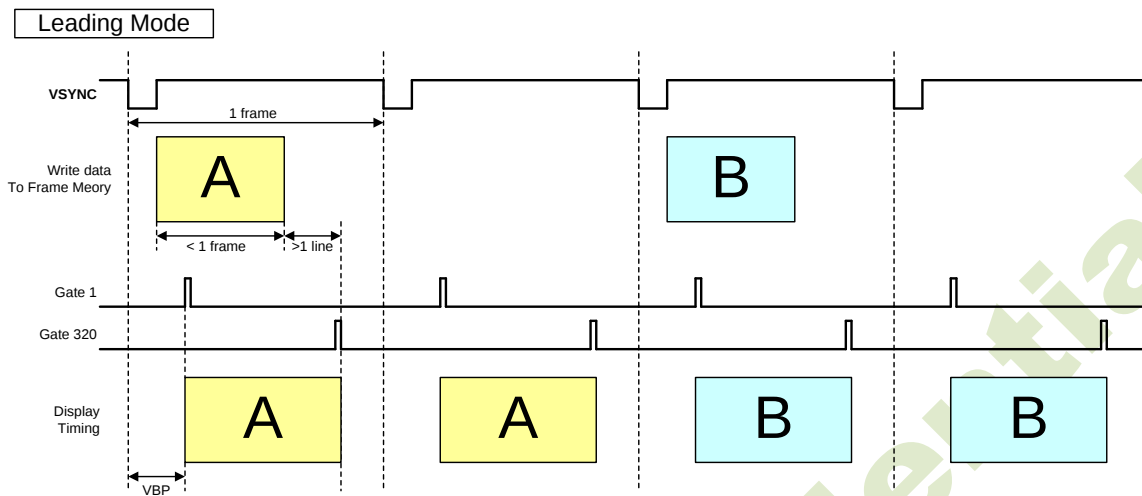


Figure. 7.19 Operation for Leading Mode of VSYNC Interface

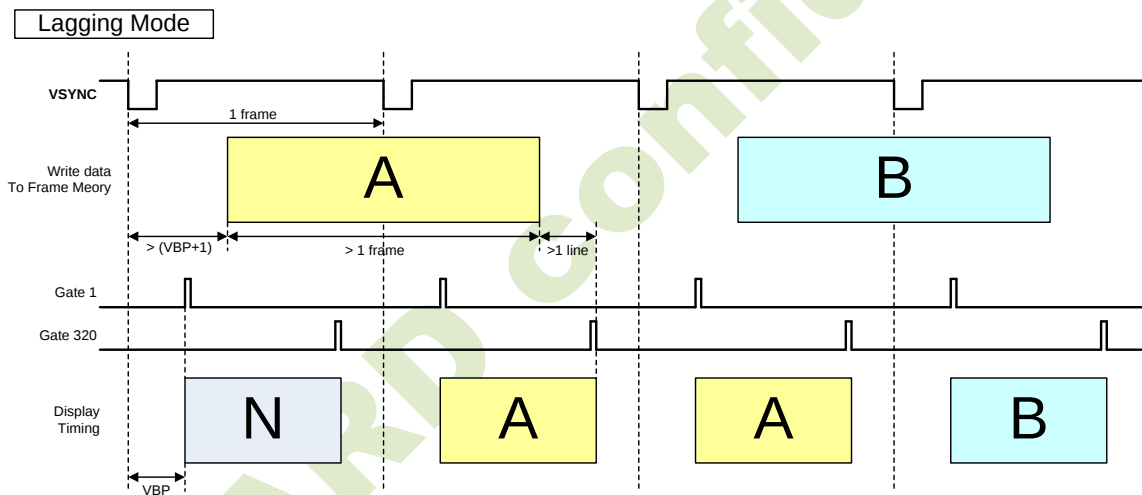


Figure. 7.20 Operation for Lagging Mode of VSYNC Interface

Notes:

1. The minimum RAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll are not available in VSYNC interface mode.

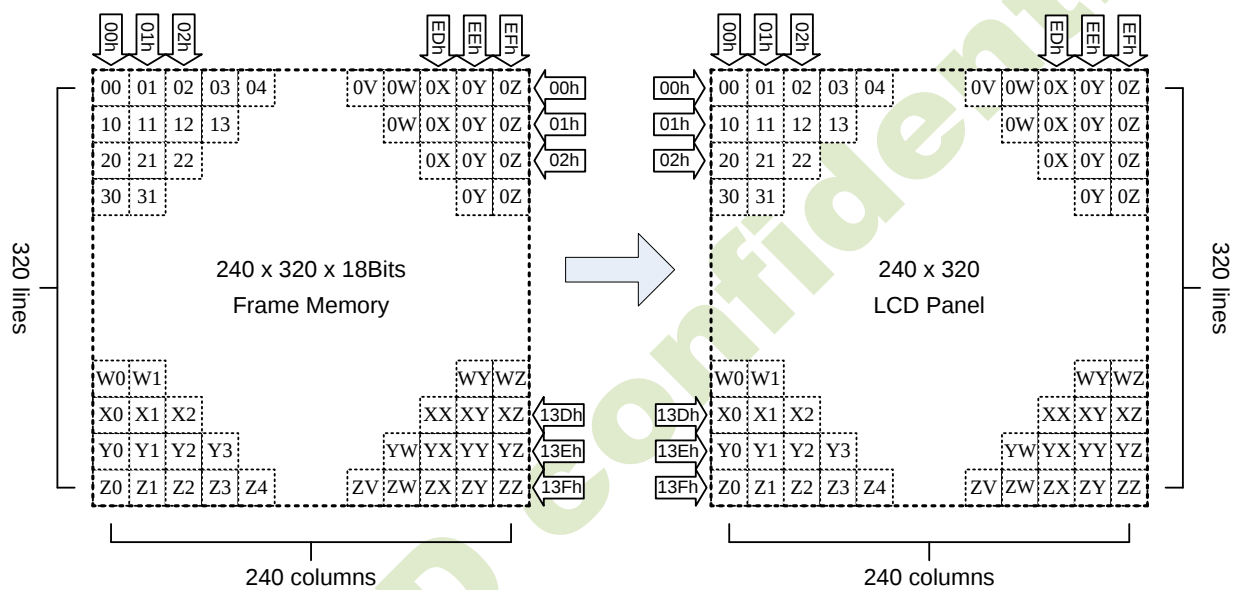
8. Function Description

8.1. Memory to Display Address Mapping

8.1.1. Normal Display On or Partial Mode On, Vertical Scroll Off

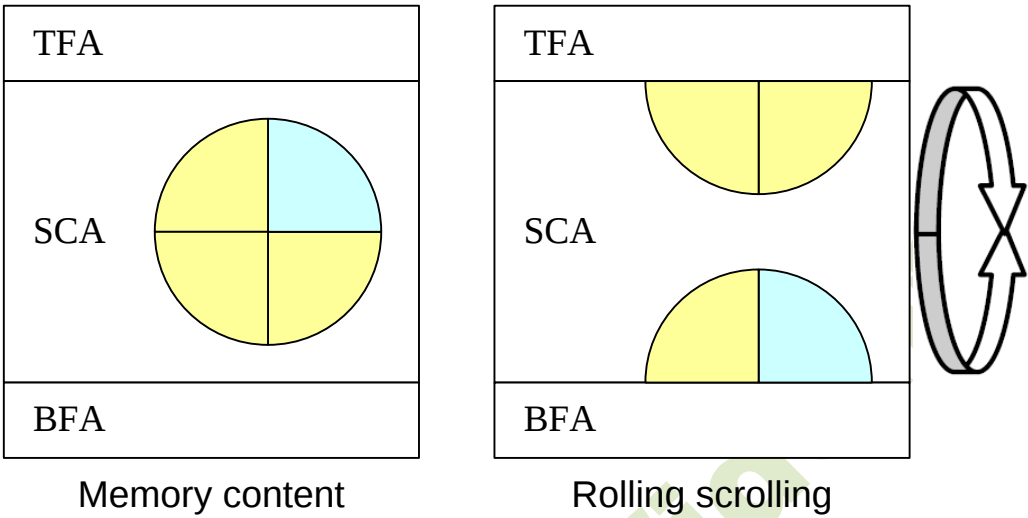
In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).

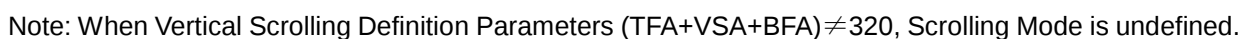
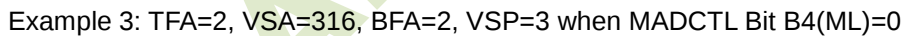
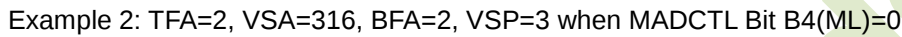


8.1.2.Vertical Scroll mode

There are one type of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).



Example 1: TFA=2, VSA=316, BFA=2, VSP=2 when MADCTL Bit B4(ML)=0



8.1.3. Vertical Scroll exaple

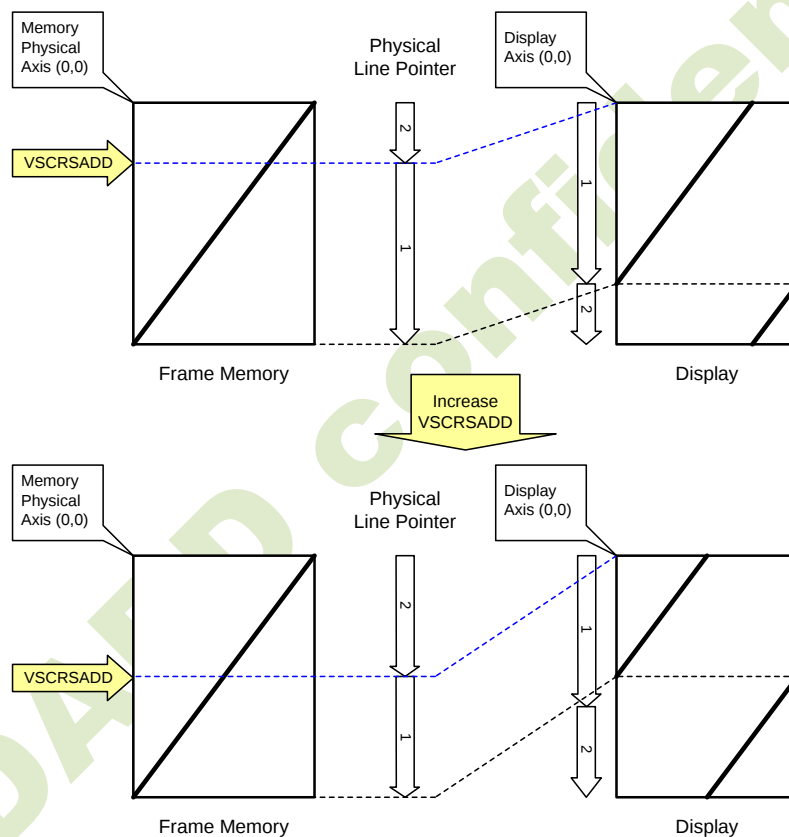
8.1.3.1. Case1: TFA+VSA+BFA≠320

N/A. Do not set TFA+VSA+BFA≠320, unless unexpected picture will be shown.

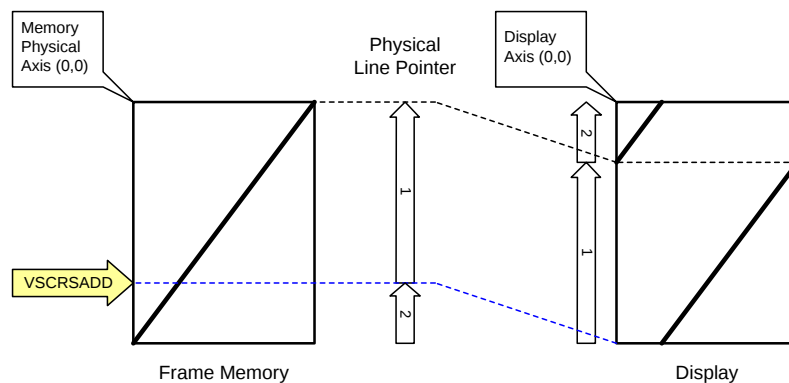
8.1.3.2. Case2: TFA+VSA+BFA = 320

Example 1. When TFA=0, VSA=320, BFA=0 and VSCRSADD=80.

MADCTL B4(ML) = "0"

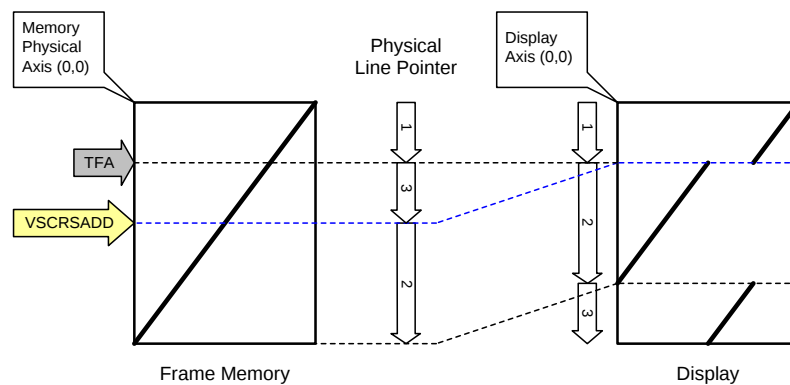


MADCTL B4(ML) = "1"

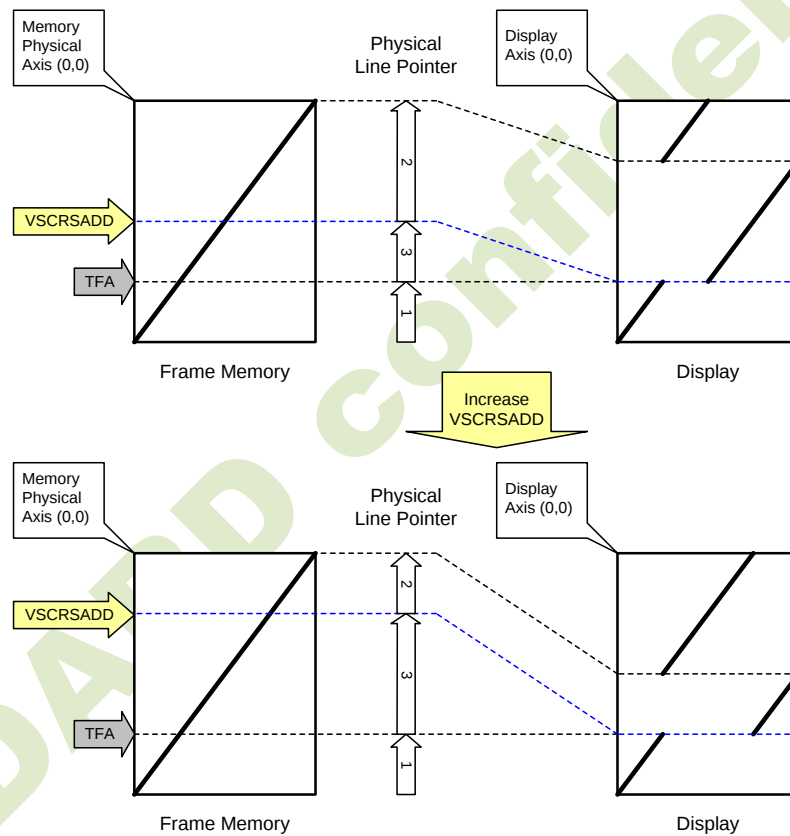


Example 2. When TFA=80, VSA=240, BFA=0 and VSCRSADD=160.

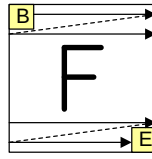
MADCTL B4(ML) = "0"



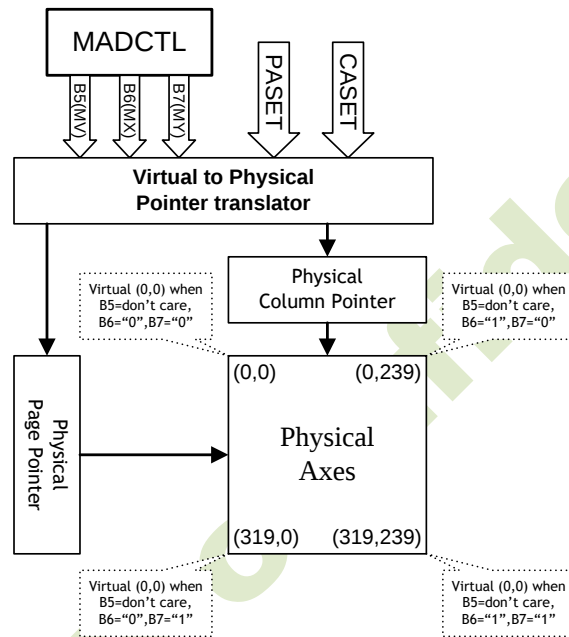
MADCTL B4(ML) = "1"



8.2.MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command(36h), Bits B5, B6, B7(MV, MX, MY) as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End column.”	Return to “Start Column”	Increment by 1
The Column counter value is larger than “End column” and the Page counter value is larger than “End page”.	Return to “Start Column”	Return to “Start Page”

The resultant image for each setting is illustrated below:

Display Data Direction	MADCTL			Image in the Host	Image in Frame Memory
	MV	MX	MY		
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-Invert	1	0	1		
X-Y exchange X-Invert	1	1	0		
X-Y exchange X-Invert Y-Invert	1	1	1		

Gggg

8.3. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

8.3.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:

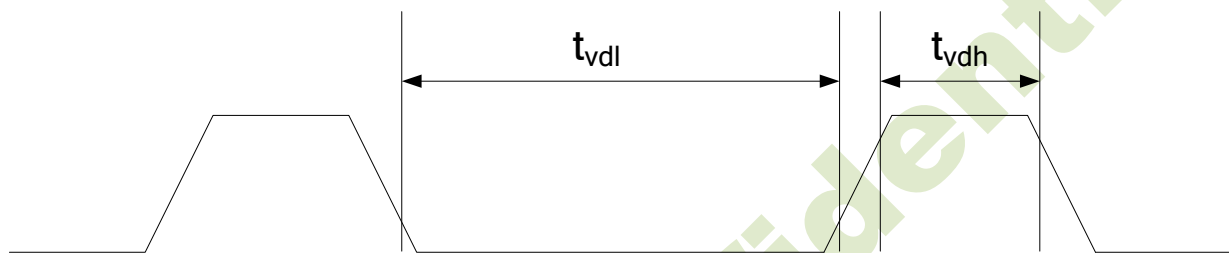


Figure. 8.1 Tearing Effect Line mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdI= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-sync and H-sync Information, there is one V-sync and N H-sync pulses per field.

N: If the resolution is 240 RGB X 320, the N=320.

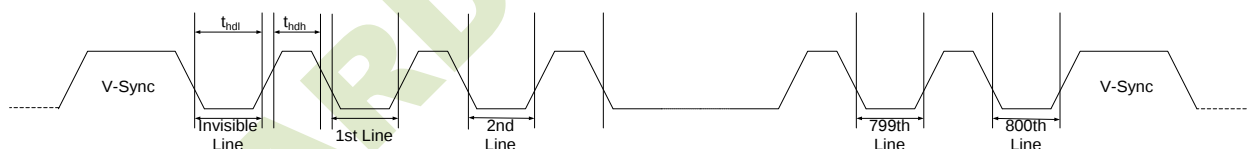


Figure. 8.2 Tearing Effect Line mode 2

thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

8.3.2. Tearing effect line timing

The Tearing Effect signal is described below.

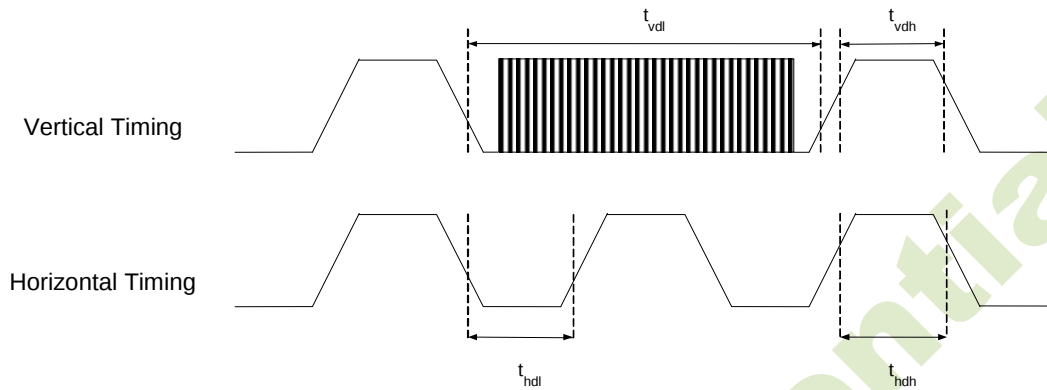


Figure. 8.3 Tearing Effect Line timing

Idle Mode Off/On (Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	TBD	-	ms
tvdh	Vertical Timing High Duration	1000	-	us
thdl	Horizontal Timing Low Duration	TBD	-	us
thdh	Horizontal Timing High Duration	TBD	500	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	ns

The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

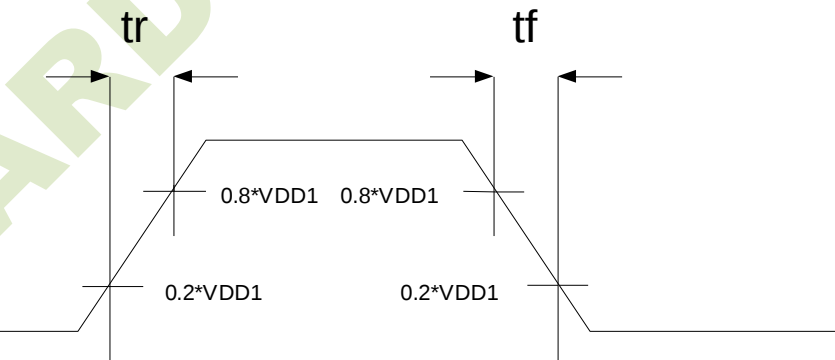
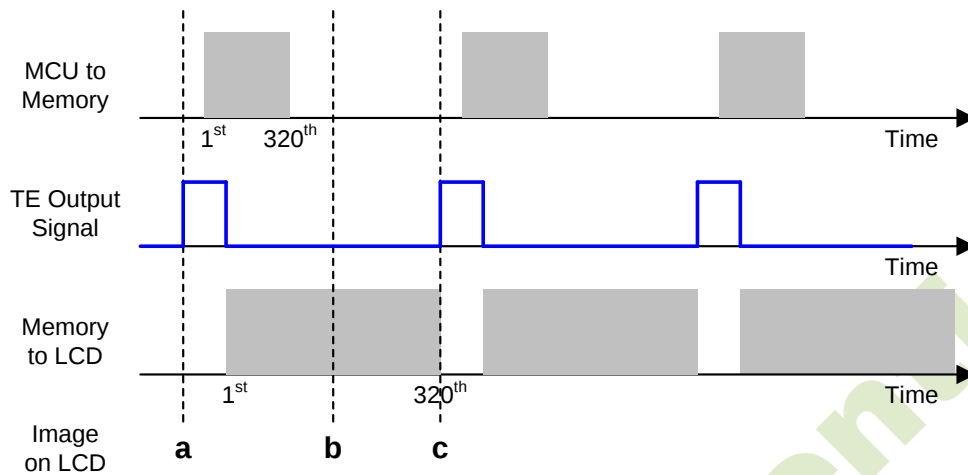
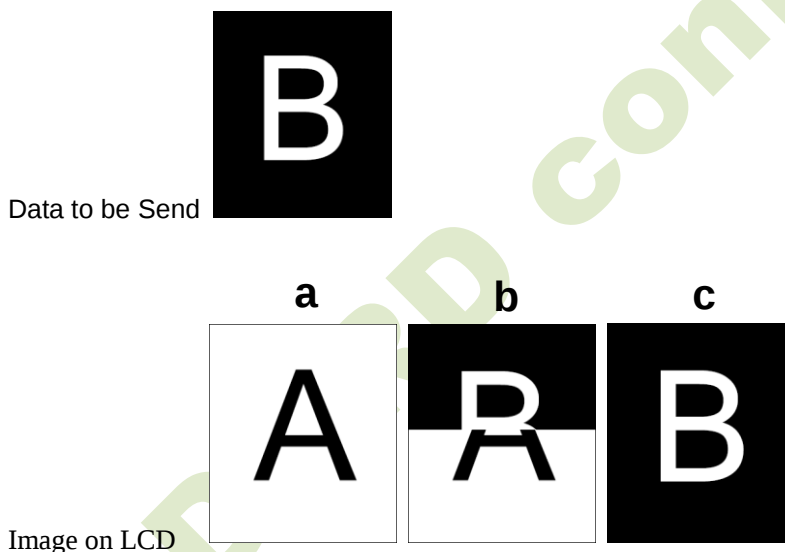


Figure. 8.4 Tearing Effect Line definition of t_f , t_r

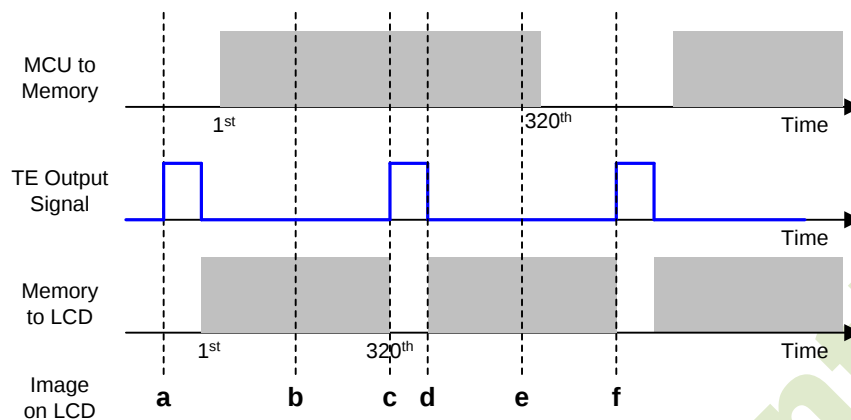
8.3.3. Example1: MCU Write is faster than panel read



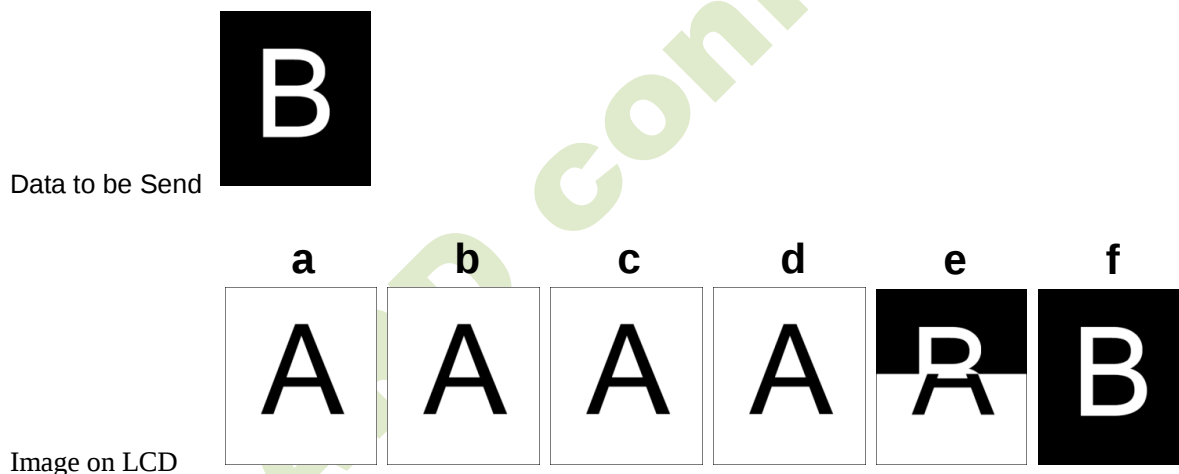
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



8.3.4. Example2: MCU Write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



8.4. Oscillator

The JD9853 has an internal R-C oscillator. The oscillator frequency is 10MHz and tolerance is 5% (at 25°C). The oscillation frequency can be adjusted according to internal register setting.

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8.5. Gamma Structure Description

8.5.1. Adjustable gamma

The JD9853 includes gamma adjustment function for the 262k colors display (64 grayscale for R-/G-/B-color). Gamma adjustment operation is implemented by 16 gamma adjustment control registers to meet the characteristic of LCD panel. Then total 64 grayscale levels are generated in Positive-/Negative-grayscale voltage. These registers are available for both polarities.

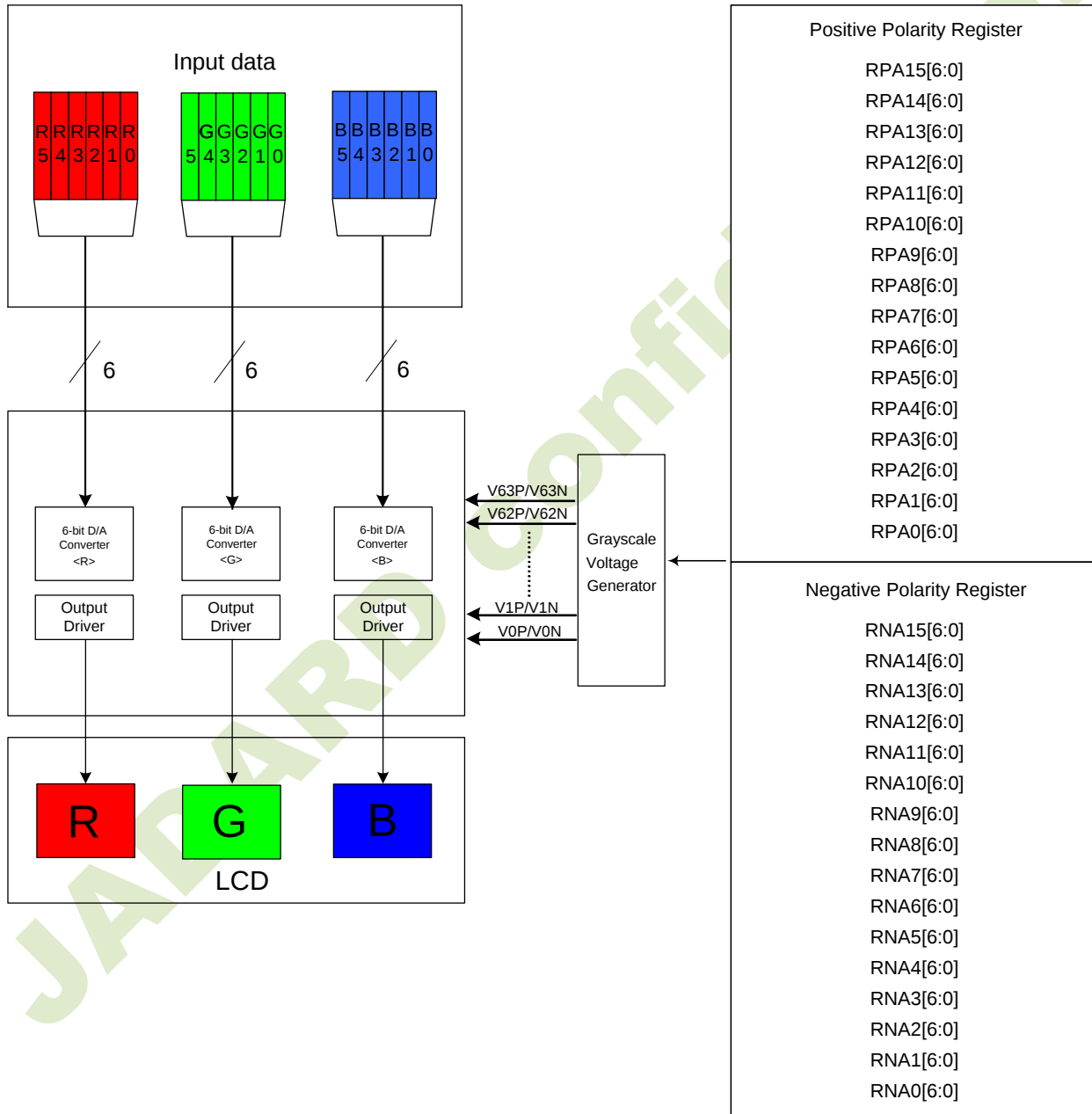


Figure 8.5 Grayscale control

8.5.2. Grayscale-Level adjustment control

The JD9853 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are belong amplitude adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

Amplitude adjustment registers

The amplitude adjustment variable registers are used to adjust the amplitude of the grayscale voltage. his function is implemented by controlling the 63-to-1 selectors (RPA/RNA0~15), each one of whole has 6 bits and generates one reference voltage output (VO(P/N)0, 1, 2, 4, 6, 13, 20, 27, 36, 43, 50, 57, 59, 61, 62, 63). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
	RPA15 5-0	RNA15 5-0	Variable resistor(RPA/RNA15) for VO(P/N)63
	RPA14 5-0	RNA14 5-0	Variable resistor(RPA/RNA14) for VO(P/N)62
	RPA13 5-0	RNA13 5-0	Variable resistor(RPA/RNA13) for VO(P/N)61
	RPA12 5-0	RNA12 5-0	Variable resistor(RPA/RNA12) for VO(P/N)59
	RPA11 5-0	RNA11 5-0	Variable resistor(RPA/RNA11) for VO(P/N)57
	RPA10 5-0	RNA10 5-0	Variable resistor(RPA/RNA10) for VO(P/N)50
	RPA9 5-0	RNA9 5-0	Variable resistor(RPA/RNA9) for VO(P/N)43
	RPA8 5-0	RNA8 5-0	Variable resistor(RPA/RNA8) for VO(P/N)36
	RPA7 5-0	RNA7 5-0	Variable resistor(RPA/RNA7) for VO(P/N)27
	RPA6 5-0	RNA6 5-0	Variable resistor(RPA/RNA6) for VO(P/N)20
	RPA5 5-0	RNA5 5-0	Variable resistor(RPA/RNA5) for VO(P/N)13
	RPA4 5-0	RNA4 5-0	Variable resistor(RPA/RNA4) for VO(P/N)6
	RPA3 5-0	RNA3 5-0	Variable resistor(RPA/RNA3) for VO(P/N)4
	RPA2 5-0	RNA2 5-0	Variable resistor(RPA/RNA2) for VO(P/N)2
	RPA1 5-0	RNA1 5-0	Variable resistor(RPA/RNA1) for VO(P/N)1
	RPA0 5-0	RNA0 5-0	Variable resistor(RPA/RNA0) for VO(P/N)0

Table 8.1 Gamma-Adjustment registers

Gamma resistor stream and 63 to 1 selector

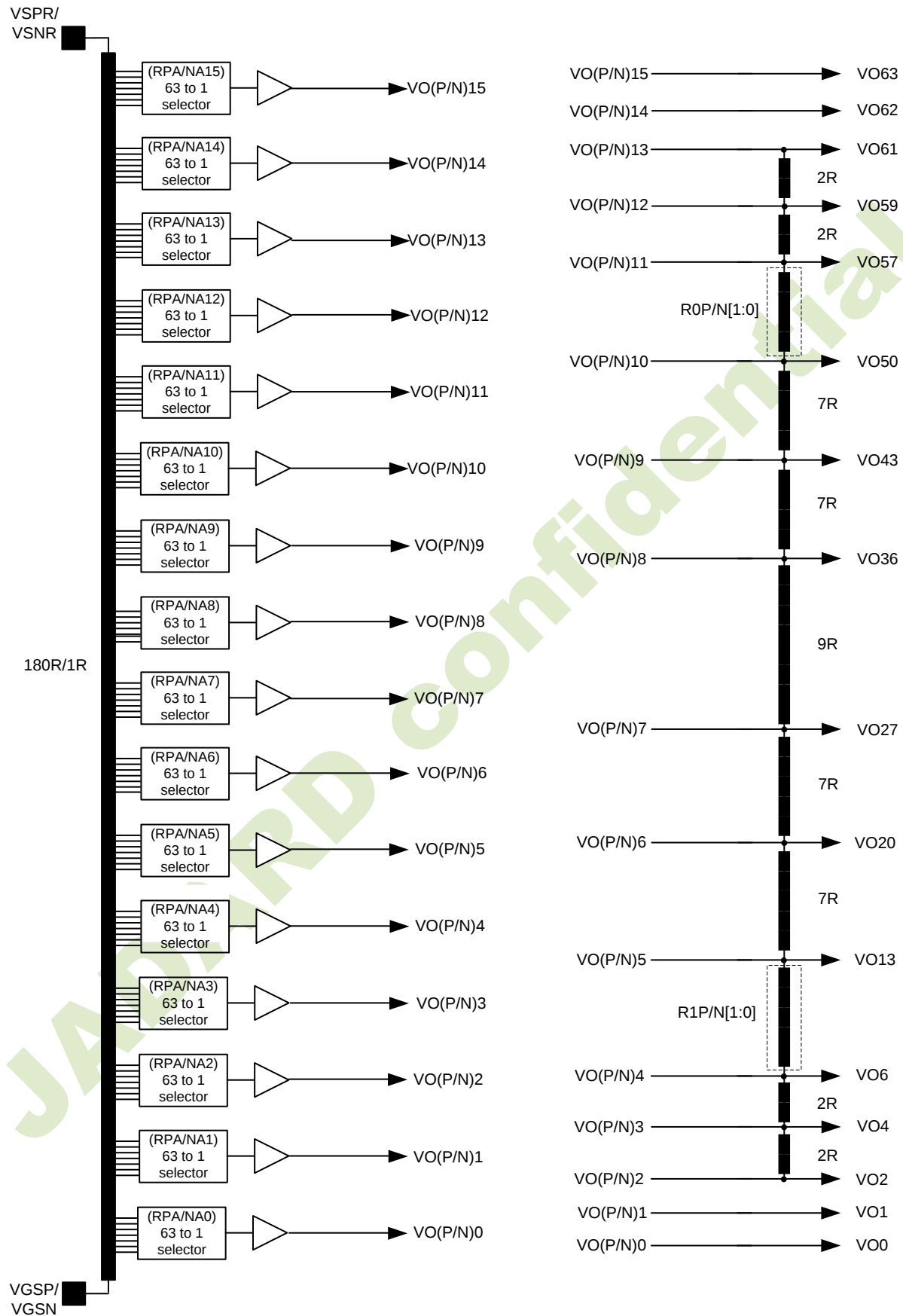


Figure. 8.6 Gamma resistor stream and gamma reference voltage

8.5.3. Variable resister ratio & Voltage levels

The resistances are decided by setting values in the Amplitude adjustment register.

The relationships are the same for RPA/RNA 0 ~15, shown below.

Value in Register RPA/RNA 0~15 (5-0)	Resistance RPA/RNA 0~15
000000	0R
000001	1R
000010	2R
000011	3R
:	:
100000	32R
100001	33R
100010	34R
100011	35R
:	:
111100	60R
111101	61R
111110	62R
111111	63R

VOP voltage levels are determined by the following formulas:

Reference voltage	Register	Amplitude adjustment value	Formula
VOP13~15	RPA13~15[5:0]	000000	$((180R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((180R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((180R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((180R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((180R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((180R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((180R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((180R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((180R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP12	RPA12[5:0]	000000	$((172R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((172R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((172R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((172R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((172R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((172R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((172R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((172R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((172R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP11	RPA11[5:0]	000000	$((162R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((162R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((162R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((162R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((162R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((162R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((162R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((162R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((162R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP10	RPA10[5:0]	000000	$((140R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((140R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((140R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((140R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((140R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((140R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((140R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((140R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((140R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP9	RPA9[5:0]	000000	$((132R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((132R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((132R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((132R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((132R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((132R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((132R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((132R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((132R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP8	RPA8[5:0]	000000	$((122R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((122R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((122R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((122R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((122R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((122R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((122R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((122R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((122R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP7	RPA7[5:0]	000000	$((112R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((112R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((112R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((112R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((112R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((112R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((112R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((112R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((112R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP6	RPA6[5:0]	000000	$((104R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((104R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((104R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((104R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((104R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((104R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((104R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((104R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((104R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP5	RPA5[5:0]	000000	$((96R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((96R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((96R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((96R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((96R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((96R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((96R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((96R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((96R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP4	RPA4[5:0]	000000	$((90R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((90R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((90R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((90R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((90R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((90R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((90R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((90R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((90R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP3	RPA3[5:0]	000000	$((86R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((86R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((86R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((86R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((86R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((86R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((86R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((86R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((86R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP2	RPA2[5:0]	000000	$((80R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((80R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((80R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((80R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((80R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((80R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((80R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((80R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((80R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP1	RPA1[5:0]	000000	$((76R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((76R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((76R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((76R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((76R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((76R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((76R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((76R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((76R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

Reference voltage	Register	Amplitude adjustment value	Formula
VOP0	RPA0[5:0]	000000	$((64R - 64R) / 180R) * (VGMP - VGSP) + VGSP$
		000001	$((64R - 63R) / 180R) * (VGMP - VGSP) + VGSP$
		000010	$((64R - 62R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		100000	$((64R - 32R) / 180R) * (VGMP - VGSP) + VGSP$
		100001	$((64R - 31R) / 180R) * (VGMP - VGSP) + VGSP$
		100010	$((64R - 30R) / 180R) * (VGMP - VGSP) + VGSP$
		:	:
		111101	$((64R - 3R) / 180R) * (VGMP - VGSP) + VGSP$
		111110	$((64R - 2R) / 180R) * (VGMP - VGSP) + VGSP$
		111111	$((64R - 1R) / 180R) * (VGMP - VGSP) + VGSP$

VON voltage levels are determined by the following formulas:

Reference voltage	Register	Amplitude adjustment value	Formula
VON13~15	RNA13~15[5:0]	000000	$((180R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((180R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((180R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((180R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((180R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((180R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((180R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((180R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((180R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON12	RNA12[5:0]	000000	$((172R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((172R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((172R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((172R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((172R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((172R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((172R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((172R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((172R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON11	RNA11[5:0]	000000	$((162R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((162R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((162R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((162R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((162R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((162R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((162R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((162R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((162R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON10	RNA10[5:0]	000000	$((140R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((140R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((140R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((140R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((140R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((140R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((140R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((140R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((140R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON9	RNA9[5:0]	000000	$((132R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((132R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((132R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((132R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((132R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((132R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((132R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((132R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((132R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON8	RNA8[5:0]	000000	$((122R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((122R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((122R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((122R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((122R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((122R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((122R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((122R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((122R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON7	RNA7[5:0]	000000	$((112R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((112R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((112R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((112R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((112R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((112R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((112R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((112R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((112R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON6	RNA6[5:0]	000000	$((104R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((104R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((104R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((104R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((104R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((104R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((104R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((104R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((104R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON5	RNA5[5:0]	000000	$((96R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((96R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((96R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((96R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((96R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((96R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((96R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((96R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((96R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON4	RNA4[5:0]	000000	$((90R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((90R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((90R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((90R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((90R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((90R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((90R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((90R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((90R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON3	RNA3[5:0]	000000	$((86R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((86R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((86R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((86R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((86R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((86R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((86R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((86R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((86R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON2	RNA2[5:0]	000000	$((80R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((80R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((80R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((80R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((80R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((80R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((80R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((80R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((80R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON1	RNA1[5:0]	000000	$((76R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((76R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((76R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((76R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((76R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((76R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((76R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((76R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((76R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

Reference voltage	Register	Amplitude adjustment value	Formula
VON0	RNA0[5:0]	000000	$((64R - 64R) / 180R) * (VGMN - VGSN) + VGSN$
		000001	$((64R - 63R) / 180R) * (VGMN - VGSN) + VGSN$
		000010	$((64R - 62R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		100000	$((64R - 32R) / 180R) * (VGMN - VGSN) + VGSN$
		100001	$((64R - 31R) / 180R) * (VGMN - VGSN) + VGSN$
		100010	$((64R - 30R) / 180R) * (VGMN - VGSN) + VGSN$
		:	:
		111101	$((64R - 3R) / 180R) * (VGMN - VGSN) + VGSN$
		111110	$((64R - 2R) / 180R) * (VGMN - VGSN) + VGSN$
		111111	$((64R - 1R) / 180R) * (VGMN - VGSN) + VGSN$

8.6. Power Level Definition

8.6.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

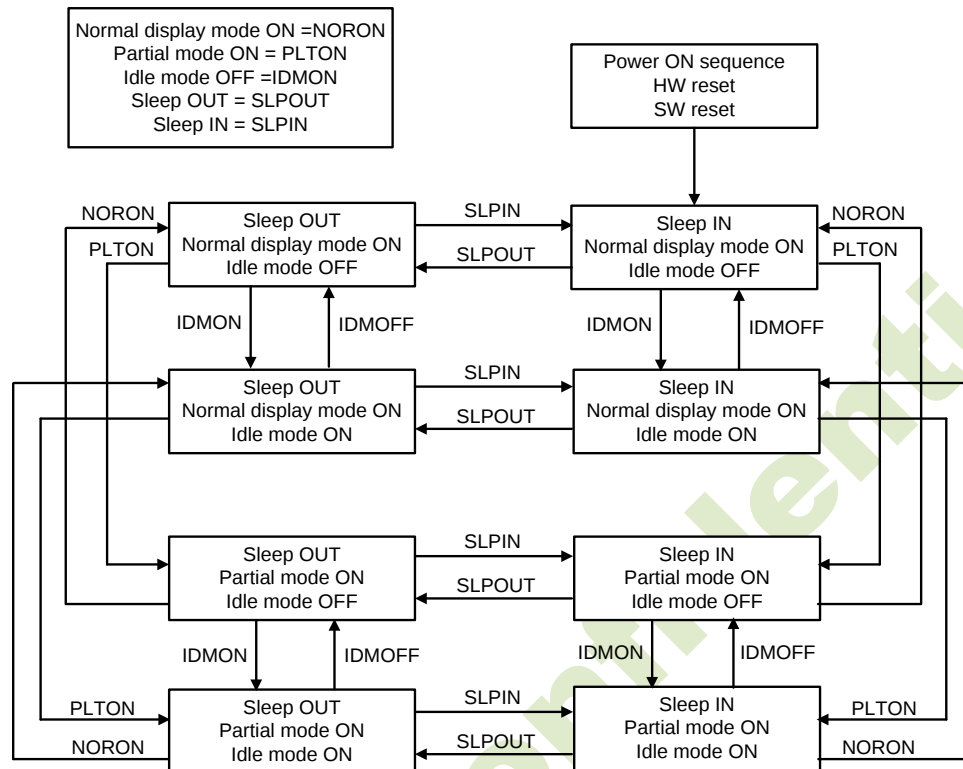
In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.

6. Power Off Mode.

In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

8.6.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

8.7. Power on/off sequence

8.7.1. General

IOVCC must be setup ready before analog power setup.

IOVCC must be power down after analog power down.

During power off, if the display module is in the SLPOUT mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if the display module is in the SLPIN mode, VCI and IOVCC can be powered down minimum 0msec after RESX has been released.

There will be no damage to the display module if the power sequences are not met.

There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display panel between end of Power On Sequence and before receiving SLPOUT command. Also, between receiving SLPOUT command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.7.1, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

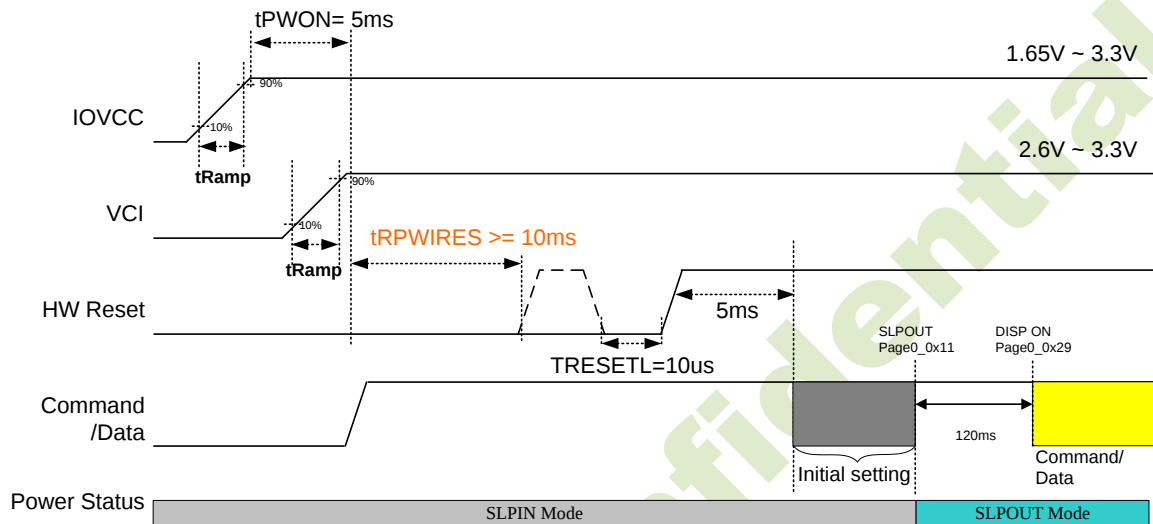
There is not a limit for Rise/Fall time on VCI, VCIP and IOVCC.

8.7.2. Power on/off sequence

Internal DC/DC power mode IOVCC=VCCH=1.65V ~ 3.3V, VCI=VCIP=2.6V ~ 3.3V.

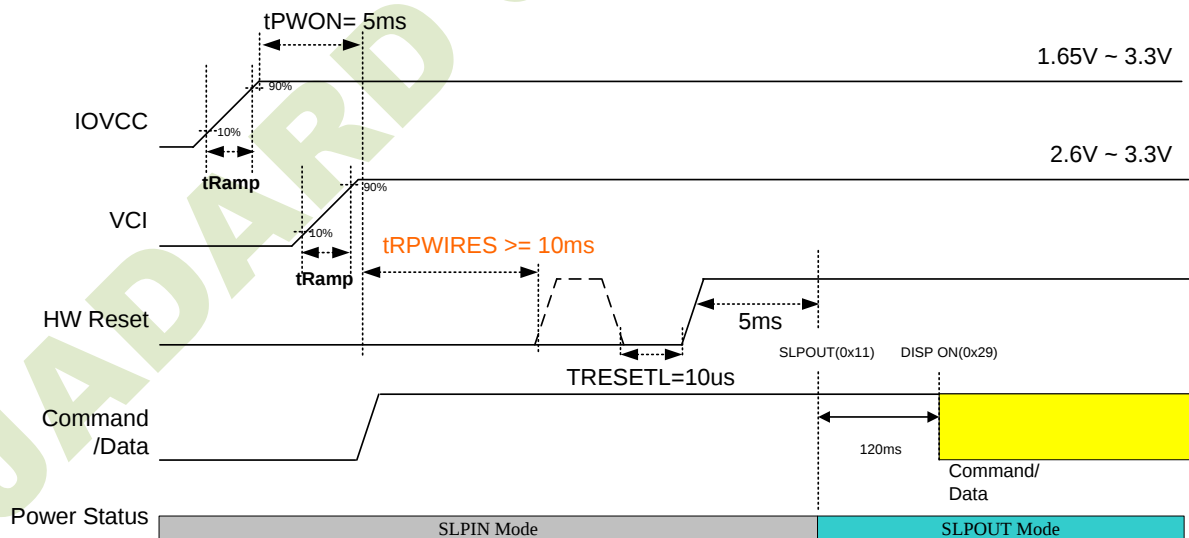
Option1: Host send initial setting than SLPOUT and DISP ON

Power on sequence

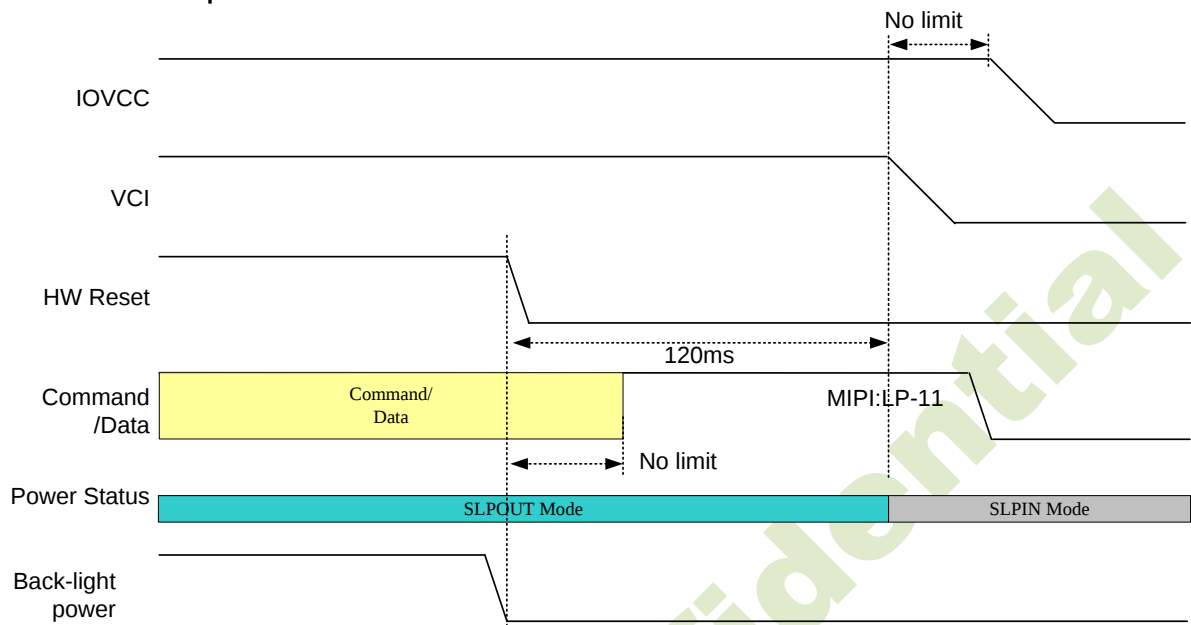
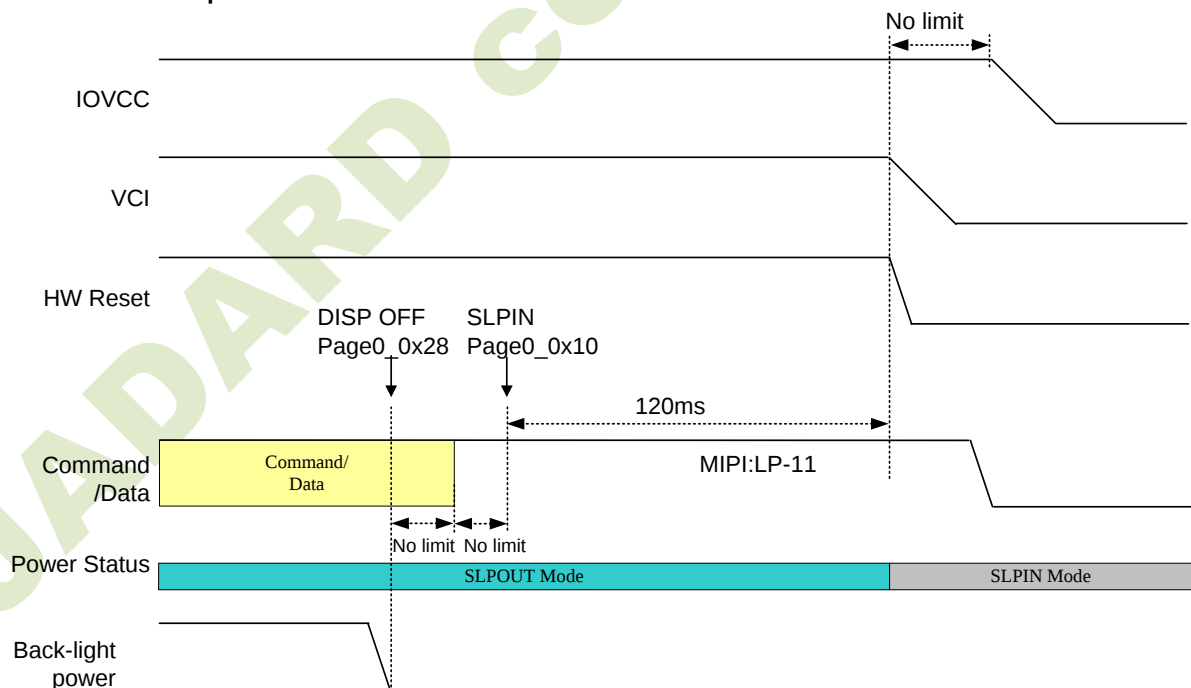


Option2: Host only send SLPOUT and DISP ON

Power on sequence



	Min	Typ	Max
Power up tRamp for VCI/IOVCC	0.2mS		20mS

Power Off Option1:**Power off sequence****Power Off Option2:****Power off sequence**

9. Command

9.1. Command List

9.1.1. Standard command

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	00h	No Operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	01h	
RDDIDIF	0	↑	1	-	0	0	0	0	0	1	0	0	04h	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	ID1[7:0]									ID1 read
	1	1	↑	-	ID2[7:0]									ID2 read
	1	1	↑	-	ID3[7:0]									ID3 read
RDRED	0	↑	1	-									06h	Read Red Color
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	R[7:0]									
RDGREEN	0	↑	1	-									07h	Read Green Color
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	G[7:0]									
RDBLUE	0	↑	1	-									08h	Read Blue Color
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	B[7:0]									
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	09h	Read Display Status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D[31:24]									
	1	1	↑	-	D[23:16]									
	1	1	↑	-	D[15:8]									
	1	1	↑	-	D[7:0]									
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	0Ah	Read display power mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0		
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	0Bh	Read display MADCTL
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	0Ch	Read display pixel format
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	0Dh	Read display image mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	0Eh	Read display signal mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	0Fh	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	0	0	0	0		
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	10h	Sleep In
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	11h	Sleep Out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	12h	Partial Mode On
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	13h	Normal display mode on
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	20h	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	21h	Display inversion on
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	28h	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	29h	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	2Ah	Column Address Set
	1	↑	1	-	SC[15:8]									Column address start
	1	↑	1	-	SC[7:0]									
	1	↑	1	-	EC[15:0]									Column address end
	1	↑	1	-	EC[7:0]									
PASET	0	↑	1	-	0	0	1	0	1	0	1	1	2Bh	Page address set
	1	↑	1	-	SP[15:0]									Page address start
	1	↑	1	-	SP[7:0]									
	1	↑	1	-	EP[15:0]									Page address end
	1	↑	1	-	EP[7:0]									
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	2Ch	Memory Write
	1	↑	1	D1[8]	D1[7:0]									Write data
	1	↑	1	Dx[8]	Dx[7:0]									
	1	↑	1	Dn[8]	Dn[7:0]									

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PLTAR	0	↑	1	-	0	0	1	1	0	0	0	0	30h	Partial Area
	1	↑	1	-	SR[15:0]									Start row
	1	↑	1	-	SR[7:0]									
	1	↑	1	-	ER[15:0]									End row
	1	↑	1	-	ER[7:0]									
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	33h	Vertical scrolling definition
	1	↑	1	-	TFA[15:8]									Top Fixed Area
	1	↑	1	-	TFA[7:0]									
	1	↑	1	-	VSA[15:8]									Vertical Scrolling Area
	1	↑	1	-	VSA[7:0]									
	1	↑	1	-	BFA[15:8]									Bottom Fixed Area
	1	↑	1	-	BFA[7:0]									
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	34h	Tearing Effect Line OFF
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	35h	Tearing Effect Line ON
	1	↑	1	-	-	-	-	-	-	-	-	M		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	36h	Memory Access Control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	37h	Vertical scrolling start address
	1	↑	1	-	VSP[15:8]									
	1	↑	1	-	VSP[7:0]									
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	38h	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	39h	Idle mode on
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	3Ah	Interface Pixel Format,
	1	↑	1	-	-	D6	D5	D4	-	D2	D1	D0		
RAMWRCON	0	↑	1	-	0	0	1	1	1	1	0	0	3Ch	Memory write continue
	1	↑	1	D1[8]	D1[7:0]									Write data
	1	↑	1	Dx[8]	Dx[7:0]									
	1	↑	1	Dn[8]	Dn[7:0]									
GETSCAN	0	↑	1	-	0	1	0	0	0	1	0	1	45h	Return the current scan line
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	SLN[15:8]									
	1	1	↑	-	SLN[15:8]									

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	68h	Read ABC Self-Diagnostic Result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D[7:6]									
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	DAh	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	module's manufacturer[7:0]									
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	DBh	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	LCD module/driver version [7:0]									
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	DCh	Read ID3
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	LCD module/driver ID[7:0]									

9.1.2. User command

TBD.

JADARD confidential

9.2. Command Description

9.2.1. NOP (00h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	0	0	0	0	0	00												
Parameter	No Parameter																								
Description	This command does not have any effect on the display module. The NOP command may be used to terminate a Frame Memory Read or Frame Memory Write.																								
Restriction																									
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></tbody></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart																									

9.2.2. SWRESET: Software Reset (01h)

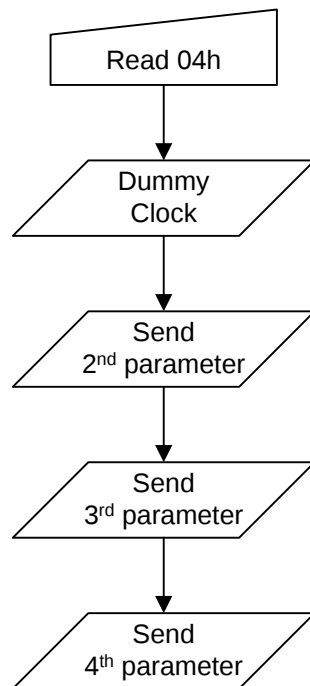
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	0	0	0	0	1	01												
Parameter	No Parameter																								
Description	The display module performs a software reset. Registers are written with their SW Reset default values. The Frame Memory contents are unaffected by this command																								
Restriction	The host processor must wait 5 milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time. If a SWRESET is sent when the display module is in SLPIN Mode, the host processor must wait 120 milliseconds before sending an SLPOUT command. SWRESET should not be sent when the display module is not in SLPIN mode																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></tbody></table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	SWRESET Blank Display Load S/W Defaults Sleep In Mode Legend Command Parameter Display Action Mode Sequential transfer																								

9.2.3. RDDIDIF: Read display identification information (04h)

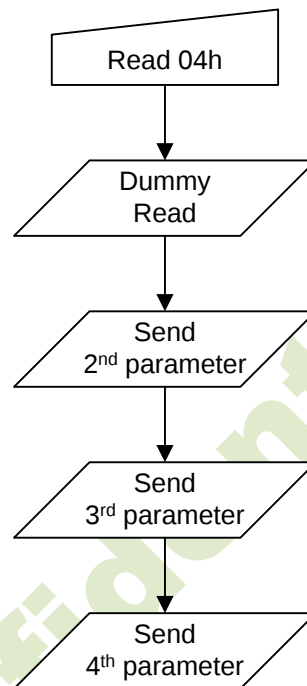
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	↑	1	-	0	0	0	0	0	1	0	0	04																			
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-																				
2 nd Parameter	1	1	↑	-	ID1[7:0]																											
3 rd Parameter	1	1	↑	-	ID2[7:0]																											
4 th Parameter	1	1	↑	-	ID3[7:0]																											
Description	This read byte returns 24-bit display identification information. The 1st Parameter is dummy read. The 2nd parameter: LCD module's manufacturer ID. The 3rd parameter: LCD module/driver version ID The 4th parameter: LCD module/driver ID.																															
Restriction	-																															
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table><thead><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID1</th><th>ID2</th><th>ID3</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>98h</td><td>51h</td><td>01h</td></tr><tr><td>SW Reset</td><td>98h</td><td>51h</td><td>01h</td></tr><tr><td>HW Reset</td><td>98h</td><td>51h</td><td>01h</td></tr></tbody></table>													Status	Default Value			ID1	ID2	ID3	Power On Sequence	98h	51h	01h	SW Reset	98h	51h	01h	HW Reset	98h	51h	01h
Status	Default Value																															
	ID1	ID2	ID3																													
Power On Sequence	98h	51h	01h																													
SW Reset	98h	51h	01h																													
HW Reset	98h	51h	01h																													

Flow Chart

Serial I/F Mode



Parallel I/F Mode



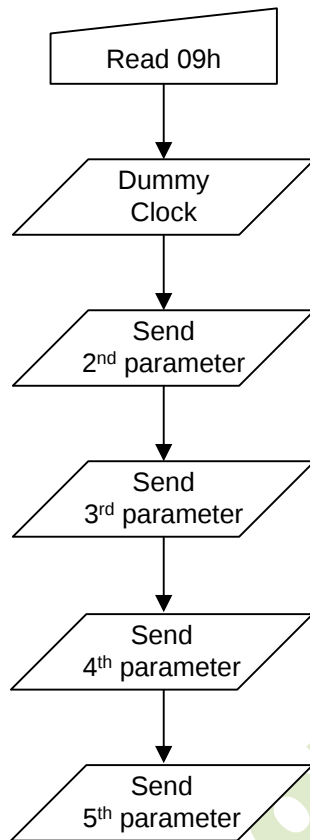
9.2.4. RDDST: Read Display Status (09h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	0	1	09
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2 nd Parameter	1	1	↑	-	D[31:24]								
3 rd Parameter	1	1	↑	-	D[23:16]								
4 th Parameter	1	1	↑	-	D[15:8]								
5 th Parameter	1	1	↑	-	D[7:0]								
Description	This command indicates the current status of the display as described in the table below												
	Bit	Description			Value								
	D31	Booster Voltage Status			'0' = Booster Off. '1' = Booster On.								
	D30	Page Address Order			'0' = Top to Bottom (MADCTL B7='0'). '1' = Bottom to Top (MADCTL B7='1').								
	D29	Column Address Order			'0' = Left to Right (MADCTL B6='0'). '1' = Right to Left (MADCTL B6='1')								
	D28	Page/Column Order			'0' = Normal Mode (When MADCTL B5='0'). '1' = Reverse Mode (When MADCTL B5='1').T								
	D27	Vertical Order			'0' = LCD Refresh Top to Bottom (When MADCTL B4='0'). '1' = LCD Refresh Bottom to Top (When MADCTL B4='1').								
	D26	RGB/BGR Order			'0' = RGB (MADCTL B3='0'). '1' = BGR (MADCTL B3='1').								
	D25	Horizontal Order			'0' = LCD Refresh Left to Right (When MADCTL B2='0'). '1' = LCD Refresh Right to Left (When MADCTL B2='1').								
	D24	For Future Use			This bit is not applicable for this project, set it to '0'								
	D23	For Future Use			This bit is not applicable for this project, set it to '0'								
	D22	Interface Color Pixel Format Definition			Interface Format			D22	D21	D20			
	Not Defined				0	0	0						
	Not Defined				0	0	1						
	Not Defined				0	1	0						
	12 Bit/Pixel				0	1	1						
	Not Defined				1	0	0						
	16 Bit/Pixel				1	0	1						
	18 Bit/Pixel				1	1	0						
	Not Defined			1	1	1							
	D19	Idle Mode On/Off			'0' = Idle Mode Off. '1' = Idle Mode On.								
	D18	Partial Mode On/Off			'0' = Partial Mode Off, '1' = Partial Mode On.								
	D17	Sleep In/Out			'0' = Sleep In Mode. '1' = Sleep Out Mode.								
	D16	Display Normal Mode On/Off			'0' = Partial or Scrolling Mode. '1' = Normal Mode.								
	D15	Vertical Scrolling Status			'0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On.								
	D14	Horizontal Scrolling Status			This bit is not applicable for this project, set it to '0'								
	D13	Inversion Status			'0' = Inversion is Off. '1' = Inversion is On.								
D12	All Pixels On			'0' = Normal mode. '1' = All Pixels On.									

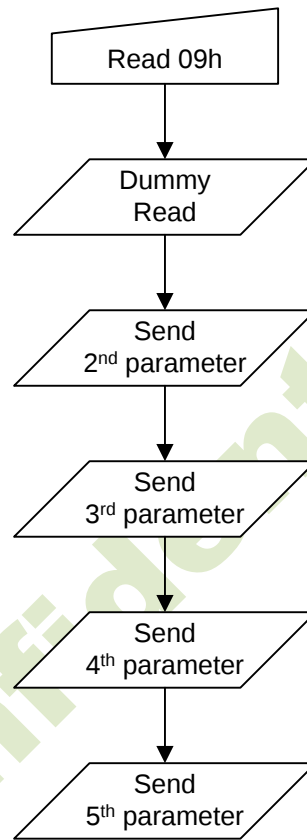
	D11	All Pixels Off	'0' = Normal mode. '1' = All Pixels Off.																						
	D10	Display On/Off	'0' = Display is Off. '1' = Display is On.																						
	D9	Tearing Effect Line On/Off	'0' =Tearing Effect Line Off. '1' = Tearing Effect On.																						
	D8	Gamma Curve Selection	Gamma Curve Selected	B8	B7	B6																			
	D7		Gamma Curve 1	0	0	0																			
			Gamma Curve 2	0	0	1																			
			Gamma Curve 3	0	1	0																			
			Gamma Curve 4	0	1	1																			
			Not Defined	1	0	0																			
			Not Defined	1	0	1																			
	D6		Not Defined	1	1	0																			
		Not Defined	1	1	1																				
	D5	Tearing Effect Output Line Mode	'0' = Mode 1, V-Blanking only. '1' = Mode 2, both H-Blanking and V-Blanking.																						
	D4	Horizontal Sync. (HSYNC, DPI I/F)	'0' = Horizontal Sync. line is Off ("Low"). '1' = Horizontal Sync. line is On ("High").																						
D3	Vertical Sync. (VSYNC, DPI I/F)	'0' = Vertical Sync. line is Off ("Low"). '1' = Vertical Sync. line is On ("High").																							
D2	Pixel Clock (DCK, DPI I/F)	'0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High").																							
D1	Data Enable (ENABLE, DPI I/F)	'0' = DE line is Off ("Low"). '1' = DE line is On ("High").																							
D0	Parity Error on DSI	'0'=No Parity Error. '1'=Parity Error.																							
Restriction	-																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>						Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID1</th><th>ID2</th><th>ID3</th></tr><tr><td>Power On Sequence</td><td>98h</td><td>51h</td><td>01h</td></tr><tr><td>SW Reset</td><td>98h</td><td>51h</td><td>01h</td></tr><tr><td>HW Reset</td><td>98h</td><td>51h</td><td>01h</td></tr></table>						Status	Default Value			ID1	ID2	ID3	Power On Sequence	98h	51h	01h	SW Reset	98h	51h	01h	HW Reset	98h	51h	01h
Status	Default Value																								
	ID1	ID2	ID3																						
Power On Sequence	98h	51h	01h																						
SW Reset	98h	51h	01h																						
HW Reset	98h	51h	01h																						

Flow Chart

Serial I/F Mode



Parallel I/F Mode

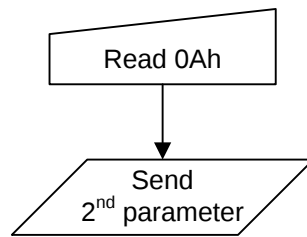


9.2.5. RDDPM: Read Display Power Mode (0Ah)

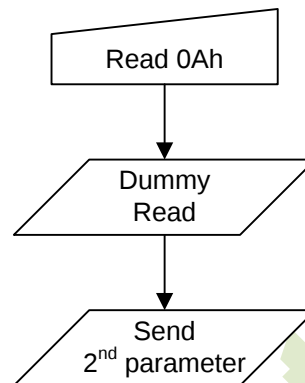
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	↑	1	-	0	0	0	0	1	0	1	0	0A																											
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-																												
2 nd Parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0																												
Description	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>D7</td><td>Booster Voltage Status</td><td>'0' = Booster Off. '1' = Booster On.</td></tr><tr><td>D6</td><td>Idle Mode On/Off</td><td>'0' = Idle Mode Off. '1' = Idle Mode On.</td></tr><tr><td>D5</td><td>Partial Mode On/Off</td><td>'0' = Partial Mode Off. '1' = Partial Mode On.</td></tr><tr><td>D4</td><td>Sleep In/Out</td><td>'0' = Sleep In Mode. '1' = Sleep Out Mode.</td></tr><tr><td>D3</td><td>Display Normal Mode On/Off</td><td>'0' = Display Normal Mode Off. '1' = Display Normal Mode On.</td></tr><tr><td>D2</td><td>Display On/Off</td><td>'0' = Display is Off. '1' = Display is On.</td></tr><tr><td>D1</td><td>Not Defined</td><td>Set to '0'</td></tr><tr><td>D0</td><td>Not Defined</td><td>Set to '0'</td></tr></table>													Bit	Description	Value	D7	Booster Voltage Status	'0' = Booster Off. '1' = Booster On.	D6	Idle Mode On/Off	'0' = Idle Mode Off. '1' = Idle Mode On.	D5	Partial Mode On/Off	'0' = Partial Mode Off. '1' = Partial Mode On.	D4	Sleep In/Out	'0' = Sleep In Mode. '1' = Sleep Out Mode.	D3	Display Normal Mode On/Off	'0' = Display Normal Mode Off. '1' = Display Normal Mode On.	D2	Display On/Off	'0' = Display is Off. '1' = Display is On.	D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
	Bit	Description	Value																																					
	D7	Booster Voltage Status	'0' = Booster Off. '1' = Booster On.																																					
	D6	Idle Mode On/Off	'0' = Idle Mode Off. '1' = Idle Mode On.																																					
	D5	Partial Mode On/Off	'0' = Partial Mode Off. '1' = Partial Mode On.																																					
	D4	Sleep In/Out	'0' = Sleep In Mode. '1' = Sleep Out Mode.																																					
	D3	Display Normal Mode On/Off	'0' = Display Normal Mode Off. '1' = Display Normal Mode On.																																					
	D2	Display On/Off	'0' = Display is Off. '1' = Display is On.																																					
	D1	Not Defined	Set to '0'																																					
	D0	Not Defined	Set to '0'																																					
Restriction	-																																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
	Status	Availability																																						
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																																						
	Normal Mode On, Idle Mode On, Sleep Out	Yes																																						
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																																						
	Partial Mode On, Idle Mode On, Sleep Out	Yes																																						
Sleep In	Yes																																							
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>08h</td></tr><tr><td>SW Reset</td><td>08h</td></tr><tr><td>HW Reset</td><td>08h</td></tr></table>													Status	Default Value	Power On Sequence	08h	SW Reset	08h	HW Reset	08h																			
	Status	Default Value																																						
	Power On Sequence	08h																																						
	SW Reset	08h																																						
HW Reset	08h																																							

Flow Chart

Serial I/F Mode



Parallel I/F Mode



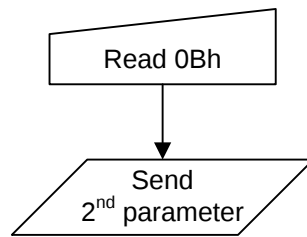
JADARD confidential

9.2.6. RDDMADCTL: Read Display MADCTL (0Bh)

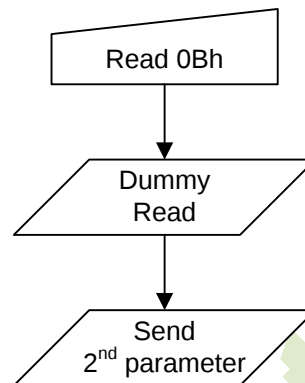
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	0	1	0	1	1	0B												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd Parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0													
Description	This command indicates the current status of the display as described in the table below:																								
	Bit	Description				Value																			
	D7	Page Address Order (MY)				'0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1').																			
	D6	Column Address Order (MX)				'0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1').																			
	D5	Page/Column Order (MV)				'0' = Normal Mode (When MADCTL B5='0'). '1' = Reverse Mode (When MADCTL B5='1').																			
	D4	Line Address Order				'0' = LCD Refresh Top to Bottom (When MADCTL B4='0'). '1' = LCD Refresh Bottom to Top (When MADCTL B4='1').																			
	D3	RGB/BGR Order				'0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').																			
	D2	Display Data Latch Order				'0' = LCD Refresh Left to Right (When MADCTL B2='0'). '1' = LCD Refresh Right to Left (When MADCTL B2='1').																			
	D1	Source scan sequence				'0' = Source output Left to Right (When MADCTL B1='0'). '1' = Source output Right to Left (When MADCTL B1='1').																			
	D0	Gate scan sequence				'0' = Gate output Top to Bottom (When MADCTL B1='0'). '1' = Gate output Bottom to Top (When MADCTL B1='1')																			
Restriction	-																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>No Change</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	No Change	HW Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
SW Reset	No Change																								
HW Reset	00h																								

Flow Chart

Serial I/F Mode



Parallel I/F Mode



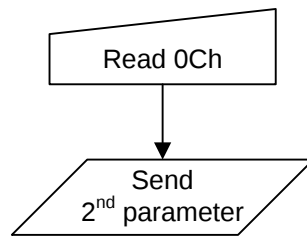
JADARD confidential

9.2.7. RDDCOLMOD: Read Display Pixel Format (0Ch)

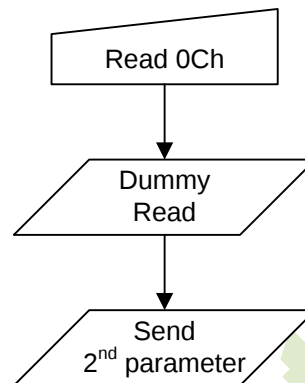
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	0	0C
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2 nd Parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description					Value						
	D7	-					Set to '0'						
	D6	RGB Interface Color Format					'011' = 12 bits/pixel						
	D5						'101' = 16 bits/pixel						
	D4						'110' = 18 bits/pixel						
	D3	-					Set to '0'						
	D2	Control Interface Color Format					'011' = 12 bits/pixel						
	D1						'101' = 16 bits/pixel						
	D0						'110' = 18 bits/pixel						
Others are no define and invalid													
“-“ Don't care													
Restriction	-												
Register Availability													
	Status							Availability					
	Normal Mode On, Idle Mode Off, Sleep Out							Yes					
	Normal Mode On, Idle Mode On, Sleep Out							Yes					
	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
	Partial Mode On, Idle Mode On, Sleep Out							Yes					
Default	Status							Default Value					
	Power On Sequence							06h (18 bits/pixel)					
	SW Reset							No Change					
	HW Reset							06h (18 bits/pixel)					

Flow Chart

Serial I/F Mode



Parallel I/F Mode



JADARD confidential

9.2.8. RDDIM: Read Display Image Mode (0Dh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX				
Command	0	↑	1	-	0	0	0	0	1	1	0	1	0D				
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-					
2 nd Parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0					
Description	This command indicates the current status of the display as described in the table below:																
	Bit	Description					Value										
	D7	Vertical Scrolling On/Off					'0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On.										
	D6	Horizontal Scrolling Status					This bit is not applicable for this project, set it to '0'										
	D5	Inversion On/Off					'0' = Inversion is Off. '1' = Inversion is On.										
	D4	All Pixels On					'0' = Normal Display '1' = White Display										
	D3	All Pixels Off					'0' = Normal Display '1' = Black Display										
	D2	Gamma Curve Selection					Gamma Curve Selected		D2	D1	D0	Gamma Set (26h)					
	Gamma Curve 1						0	0	0	CG0							
	Gamma Curve 2						0	0	1	CG1							
	Gamma Curve 3						0	1	0	CG2							
	Gamma Curve 4						0	1	1	CG3							
Not Defined							1	0	0								
Not Defined							1	0	1								
Not Defined							1	1	0								
D1	Gamma Curve Selection					Not Defined		1	0	0							
Not Defined						1	0	1									
Not Defined						1	1	0									
Not Defined						1	1	1									
D0						Gamma Curve Selection					Not Defined		1	1	1		
Not Defined											1	1	1				
Not Defined											1	1	1				
Not Defined											1	1	1				
Not Defined		1	1	1													
Not Defined		1	1	1													
Not Defined		1	1	1													
Not Defined		1	1	1													
Restriction	-																
Register Availability																	

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>	Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h
Status	Default Value								
Power On Sequence	00h								
SW Reset	00h								
HW Reset	00h								
Flow Chart	Serial I/F Mode <pre>graph TD; A[Read 0Dh] --> B[/Send 2nd parameter/];</pre> Parallel I/F Mode <pre>graph TD; A[Read 0Dh] --> B[/Dummy Read/]; B --> C[/Send 2nd parameter/];</pre>								

9.2.9. RDDSM: Read Display Signal Mode (0Eh)

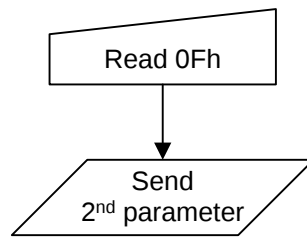
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	0	1	1	1	0	0E												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd Parameter	1	1	↑	-	TEON	TEM	0	0	0	0	0	0													
Description	This command indicates the current status of the display as described in the table below: <table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>'0' = Tearing Effect Line Off. '1' = Tearing Effect On.</td></tr><tr><td>D6</td><td>Tearing Effect Line Output Mode</td><td>'0' = Mode 1. '1' = Mode 2</td></tr></table>													Bit	Description	Value	D7	Tearing Effect Line On/Off	'0' = Tearing Effect Line Off. '1' = Tearing Effect On.	D6	Tearing Effect Line Output Mode	'0' = Mode 1. '1' = Mode 2			
Bit	Description	Value																							
D7	Tearing Effect Line On/Off	'0' = Tearing Effect Line Off. '1' = Tearing Effect On.																							
D6	Tearing Effect Line Output Mode	'0' = Mode 1. '1' = Mode 2																							
Restriction	-																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
SW Reset	00h																								
HW Reset	00h																								
Flow Chart	Serial I/F Mode <pre>graph TD; A[Read 0Eh] --> B[/Send 2nd parameter/];</pre> Parallel I/F Mode <pre>graph TD; A[Read 0Eh] --> B[/Dummy Read/]; B --> C[/Send 2nd parameter/];</pre>																								

9.2.10. RDDSDR: Read Display Self-Diagnostic Result (0Fh)

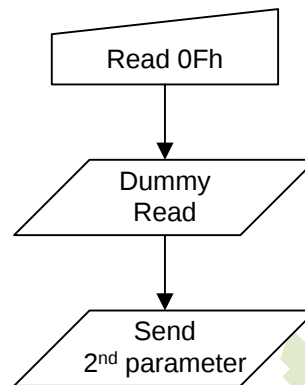
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	1	0F
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2 nd Parameter	1	1	↑	-	D7	D6	D5	D4	0	0	0	0	
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description					Value						
	D7	Register Loading Detection					See section “Sleep Out –command and self-diagnostic functions of the display module”						
	D6	Functionality Detection											
	D5	Chip Attachment Detection					Set to '0' if feature unimplemented.						
	D4	Display Glass Break Detection					Set to '0' if feature unimplemented.						
	D3	Reserved					Set to '0'.						
	D2						Set to '0'.						
	D1						Set to '0'.						
	D0						Set to '0'.						
Restriction	-												
Register Availability													
	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default													
	Status					Default Value							
	Power On Sequence					00h							
	SW Reset					00h							
	HW Reset					00h							

Flow Chart

Serial I/F Mode

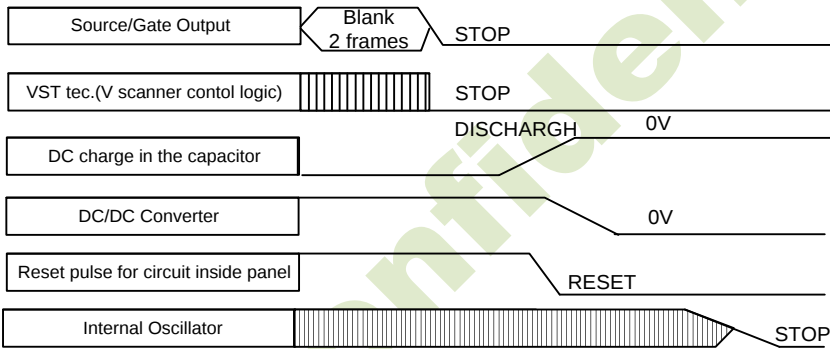


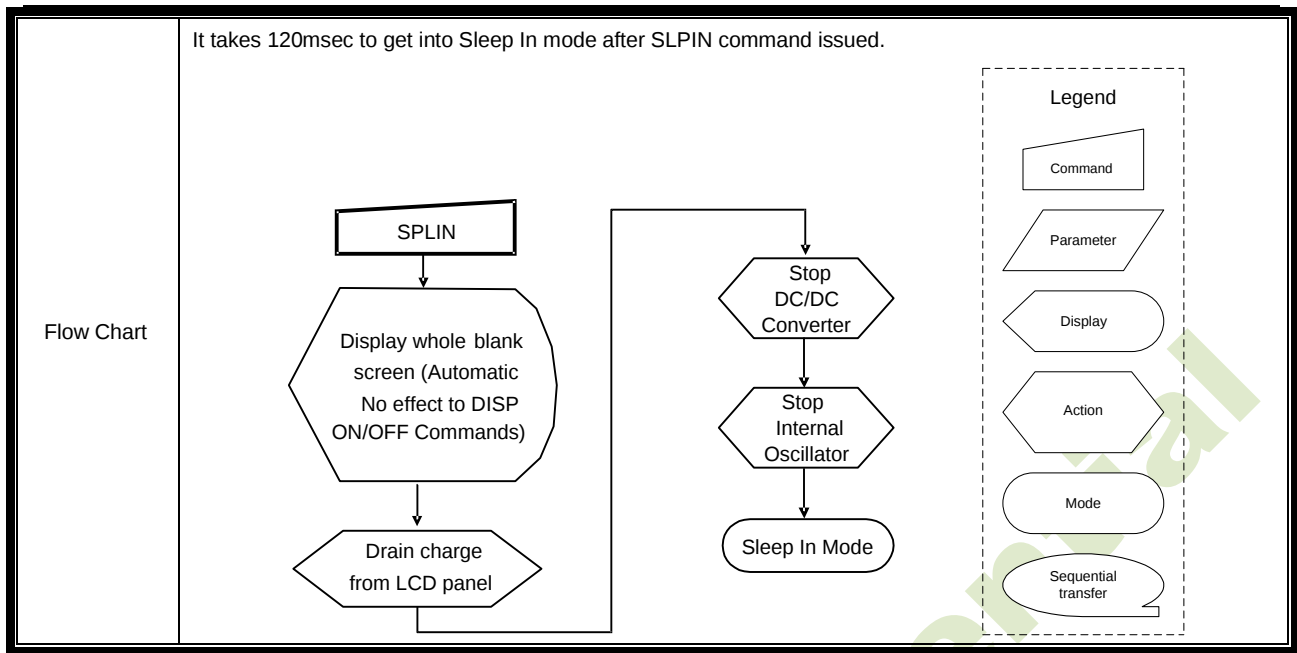
Parallel I/F Mode



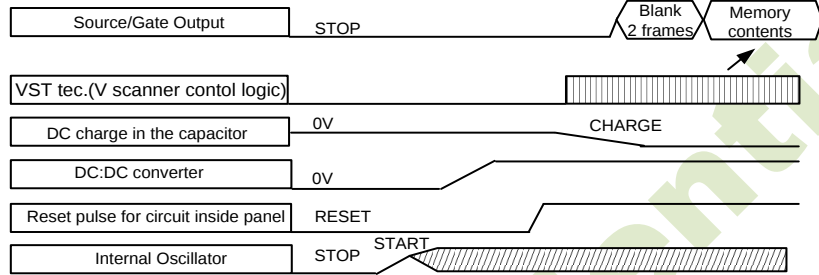
JADARD confidential

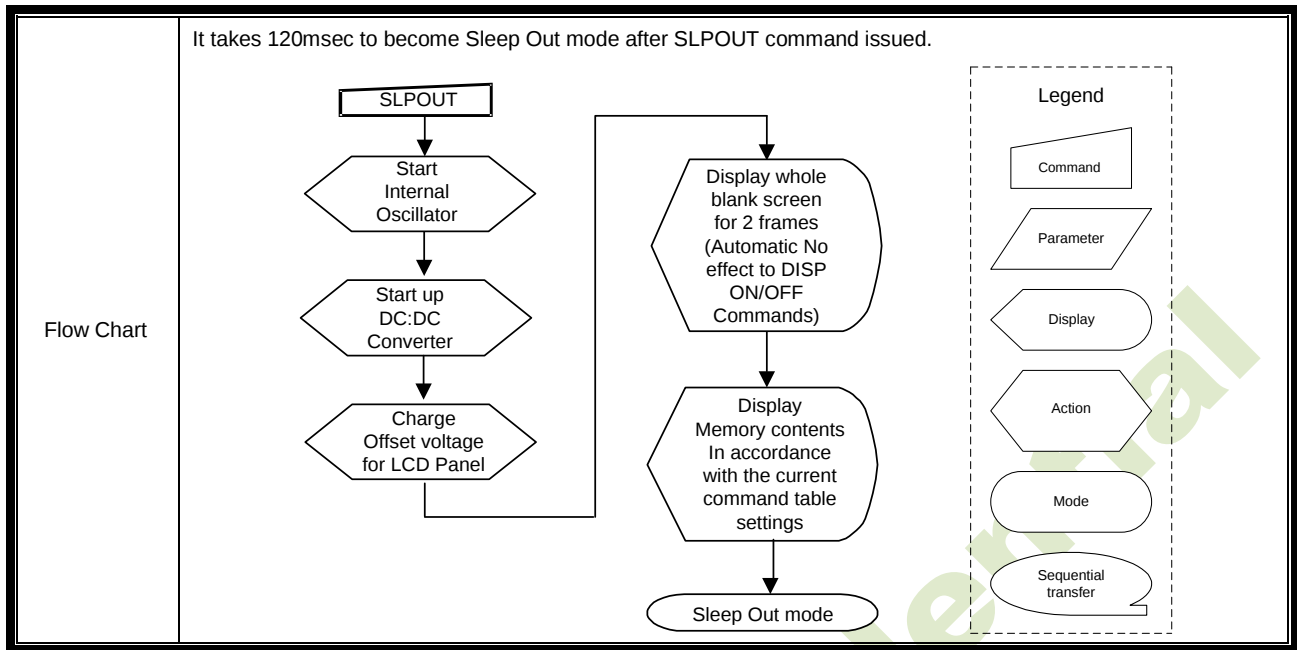
9.2.11. SLPIN: Sleep In (10h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	1	0	0	0	0	10												
Parameter	No Parameter																								
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports. MCU interface and memory are still working and the memory keeps its contents. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. 																								
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>SW Reset</td><td>Sleep in mode</td></tr><tr><td>HW Reset</td><td>Sleep in mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep in mode	SW Reset	Sleep in mode	HW Reset	Sleep in mode				
Status	Default Value																								
Power On Sequence	Sleep in mode																								
SW Reset	Sleep in mode																								
HW Reset	Sleep in mode																								



9.2.12. SLPOUT: Sleep Out (11h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	1	0	0	0	1	11												
Parameter	No Parameter																								
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. 																								
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>SW Reset</td><td>Sleep in mode</td></tr><tr><td>HW Reset</td><td>Sleep in mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep in mode	SW Reset	Sleep in mode	HW Reset	Sleep in mode				
Status	Default Value																								
Power On Sequence	Sleep in mode																								
SW Reset	Sleep in mode																								
HW Reset	Sleep in mode																								



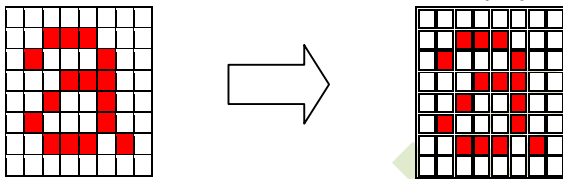
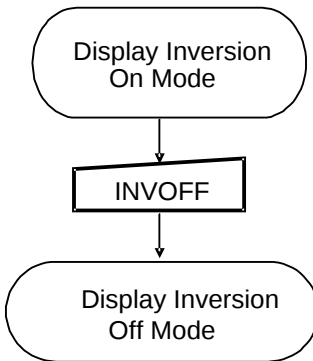
9.2.13. PTLON: Partial Mode ON (12h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	1	0	0	1	0	12												
Parameter	No Parameter																								
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.																								
Restriction	This command has no effect when Partial mode is active.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>SW Reset</td><td>Normal Mode On</td></tr><tr><td>HW Reset</td><td>Normal Mode On</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Normal Mode On	SW Reset	Normal Mode On	HW Reset	Normal Mode On				
Status	Default Value																								
Power On Sequence	Normal Mode On																								
SW Reset	Normal Mode On																								
HW Reset	Normal Mode On																								
Flow Chart	See Partial Area (30h)																								

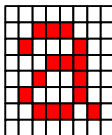
9.2.14. NORON: Normal Display Mode ON (13h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	0	1	0	0	1	1	13												
Parameter	No Parameter																								
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off. There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.																								
Restriction	This command has no effect when Normal Display mode is active.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>SW Reset</td><td>Normal Mode On</td></tr><tr><td>HW Reset</td><td>Normal Mode On</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Normal Mode On	SW Reset	Normal Mode On	HW Reset	Normal Mode On				
Status	Default Value																								
Power On Sequence	Normal Mode On																								
SW Reset	Normal Mode On																								
HW Reset	Normal Mode On																								
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.																								

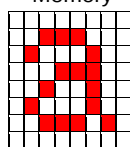
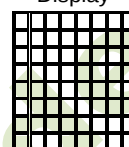
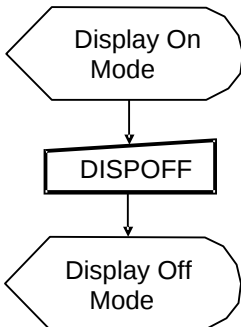
9.2.15. INVOFF: Display Inversion OFF (20h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	0	0	0	0	20												
Parameter	No Parameter																								
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. Memory (Example) Display 																								
Restriction	This command has no effect when module is already in inversion off mode.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>SW Reset</td><td>Display Inversion off</td></tr><tr><td>HW Reset</td><td>Display Inversion off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Display Inversion off	SW Reset	Display Inversion off	HW Reset	Display Inversion off				
Status	Default Value																								
Power On Sequence	Display Inversion off																								
SW Reset	Display Inversion off																								
HW Reset	Display Inversion off																								
Flow Chart	 <pre>graph TD A([Display Inversion On Mode]) --> B[INVOFF] B --> C([Display Inversion Off Mode])</pre>																								

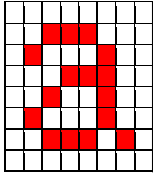
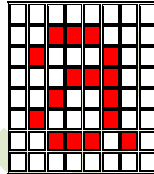
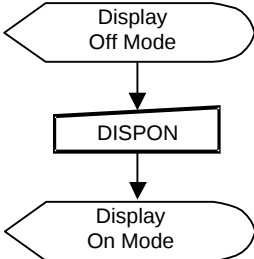
9.2.16. INVON: Display Inversion ON (21h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	0	0	0	1	21												
Parameter	No Parameter																								
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory  → display 																								
Restriction	This command has no effect when module is already in inversion on mode.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>SW Reset</td><td>Display Inversion off</td></tr><tr><td>HW Reset</td><td>Display Inversion off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Display Inversion off	SW Reset	Display Inversion off	HW Reset	Display Inversion off				
Status	Default Value																								
Power On Sequence	Display Inversion off																								
SW Reset	Display Inversion off																								
HW Reset	Display Inversion off																								
Flow Chart	Display Inversion OFF Mode ↓ INVON ↓ Display Inversion ON Mode																								

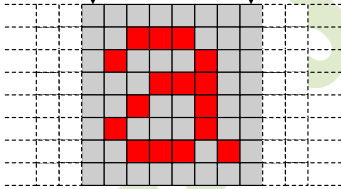
9.2.17. DISPOFF: Display Off (28h)

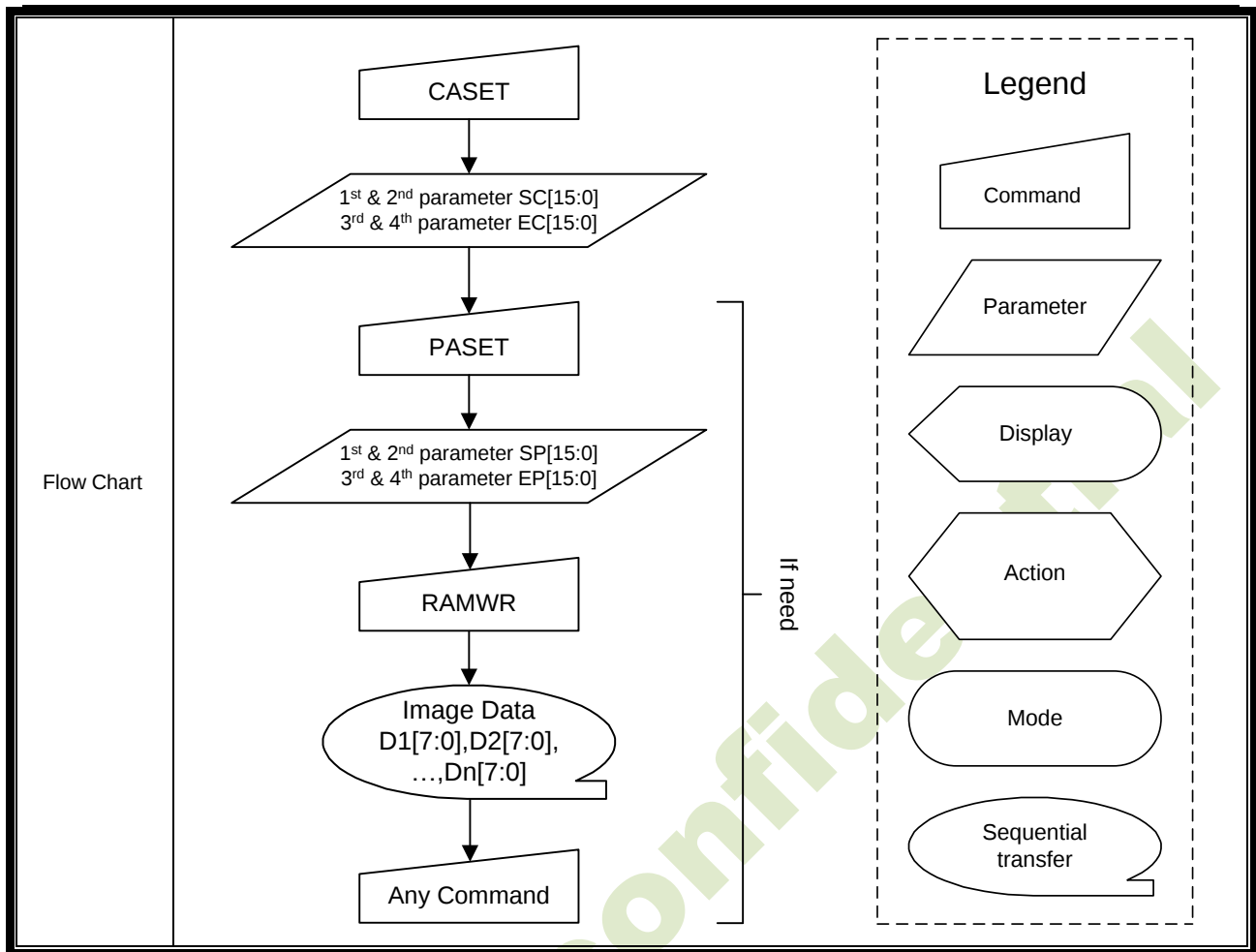
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	0	0	0	28												
Parameter	No Parameter																								
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Example Memory  → Display 																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>SW Reset</td><td>Display off</td></tr><tr><td>HW Reset</td><td>Display off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Display off	SW Reset	Display off	HW Reset	Display off				
Status	Default Value																								
Power On Sequence	Display off																								
SW Reset	Display off																								
HW Reset	Display off																								
Flow Chart																									

9.2.18. DISPON: Display On (29h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	0	0	1	29												
Parameter	No Parameter																								
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory  → Display 																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>SW Reset</td><td>Display off</td></tr><tr><td>HW Reset</td><td>Display off</td></tr></table>													Status	Default Value	Power On Sequence	Display off	SW Reset	Display off	HW Reset	Display off				
Status	Default Value																								
Power On Sequence	Display off																								
SW Reset	Display off																								
HW Reset	Display off																								
Flow Chart	 <pre>graph TD; A([Display Off Mode]) --> B[DISPON]; B --> C([Display On Mode]);</pre>																								

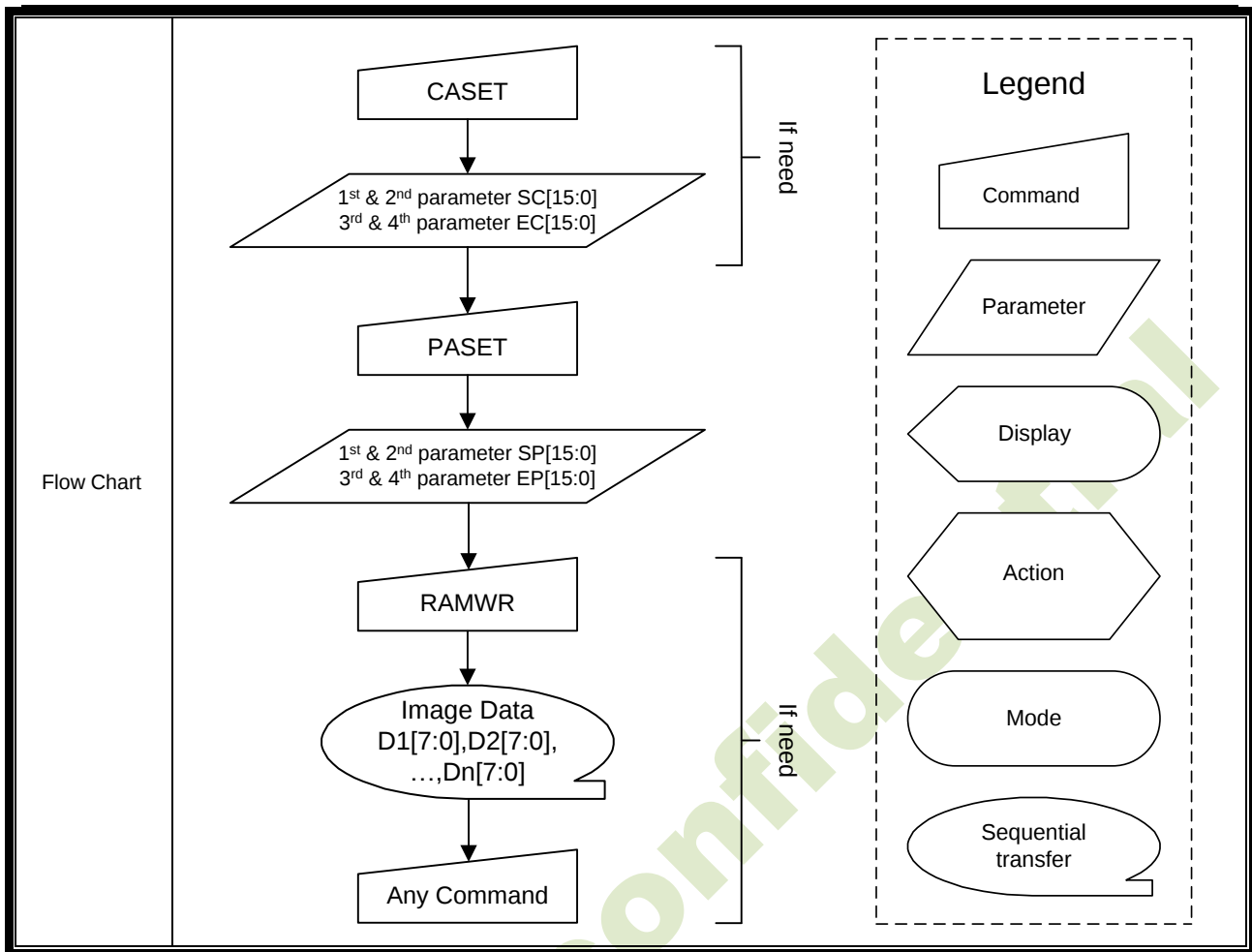
9.2.19. CASET: Column Address Set (2Ah)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	0	1	0	2A												
1 st Parameter	1	↑	1	-	SC[15:8]																				
2 nd Parameter	1	↑	1	-	SC[7:0]																				
3 rd Parameter	1	↑	1	-	EC[15:0]																				
4 th Parameter	1	↑	1	-	EC[7:0]																				
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.																								
	SC[15:0] EC[15:0] 																								
Restriction	SC[15:0] always must be equal to or less than EC[15:0] Note 1: When SC[15:0] or EC[15:0] is greater than 7Fh (when MADCTL's B5=0) or 9Fh (when MADCTL's B5=1), data of out of range will be ignored																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th colspan="2">Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>SC[15:0] = 0000h</td><td>EC[15:0] = 00EFh</td></tr><tr><td>SW Reset</td><td>SC[15:0] = 0000h</td><td>When MV=0: EC[15:0] = 00EFh When MV=1: EC[15:0] = 013Fh</td></tr><tr><td>HW Reset</td><td>SC[15:0] = 0000h</td><td>EC[15:0] = 00EFh</td></tr></tbody></table>													Status	Default Value		Power On Sequence	SC[15:0] = 0000h	EC[15:0] = 00EFh	SW Reset	SC[15:0] = 0000h	When MV=0: EC[15:0] = 00EFh When MV=1: EC[15:0] = 013Fh	HW Reset	SC[15:0] = 0000h	EC[15:0] = 00EFh
Status	Default Value																								
Power On Sequence	SC[15:0] = 0000h	EC[15:0] = 00EFh																							
SW Reset	SC[15:0] = 0000h	When MV=0: EC[15:0] = 00EFh When MV=1: EC[15:0] = 013Fh																							
HW Reset	SC[15:0] = 0000h	EC[15:0] = 00EFh																							



9.2.20. PASET: Page Address Set (2Bh)

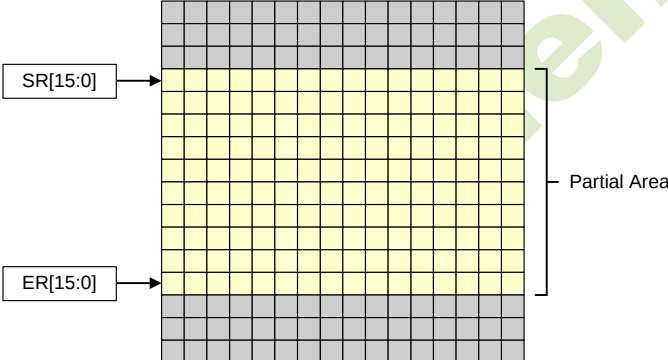
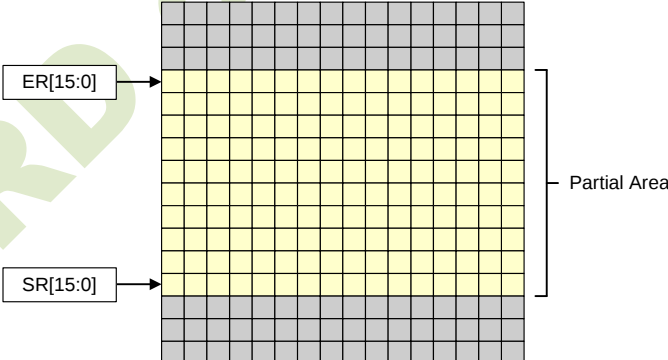
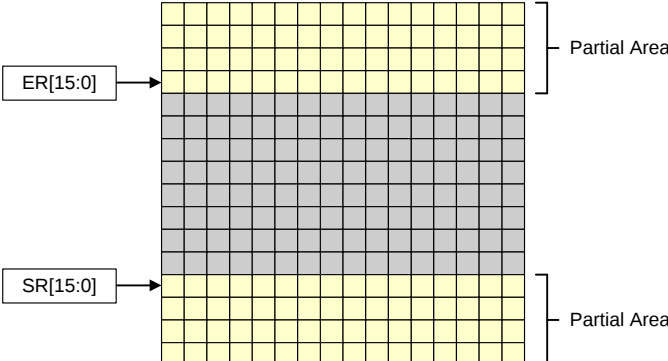
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	0	1	1	2B												
1 st Parameter	1	↑	1	-	SP[15:8]																				
2 nd Parameter	1	↑	1	-	SP[7:0]																				
3 rd Parameter	1	↑	1	-	EP[15:0]																				
4 th Parameter	1	↑	1	-	EP[7:0]																				
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory. SP[15:0] EP[15:0]																								
Restriction	SP[15:0] always must be equal to or less than EP[15:0] Note 1: When SP[15:0] or EP[15:0] is greater than 9Fh (When MADCTL's B5=0) or 7Fh (When MADCTL's B5=1), data of out of range will be ignored.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th colspan="2">Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>SP[15:0] = 0000h</td><td>EC[15:0] = 013Fh</td></tr><tr><td>SW Reset</td><td>SP[15:0] = 0000h</td><td>When MV=0: EC[15:0] = 013Fh When MV=1: EC[15:0] = 00EFh</td></tr><tr><td>HW Reset</td><td>SP[15:0] = 0000h</td><td>EC[15:0] = 013Fh</td></tr></tbody></table>													Status	Default Value		Power On Sequence	SP[15:0] = 0000h	EC[15:0] = 013Fh	SW Reset	SP[15:0] = 0000h	When MV=0: EC[15:0] = 013Fh When MV=1: EC[15:0] = 00EFh	HW Reset	SP[15:0] = 0000h	EC[15:0] = 013Fh
Status	Default Value																								
Power On Sequence	SP[15:0] = 0000h	EC[15:0] = 013Fh																							
SW Reset	SP[15:0] = 0000h	When MV=0: EC[15:0] = 013Fh When MV=1: EC[15:0] = 00EFh																							
HW Reset	SP[15:0] = 0000h	EC[15:0] = 013Fh																							



9.2.21. RAMWR: Memory Write (2Ch)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	0	1	1	0	0	2C												
1 st Parameter	1	↑	1	D1[8]	D1[7:0]																				
...	1	↑	1	Dx[8]	Dx[7:0]																				
N th Parameter	1	↑	1	Dn[8]	Dn[7:0]																				
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. Then D[8:0] is stored in frame memory and the column register and the page register Incremented. Sending any other command can stop frame Write.																								
Restriction	In all color modes, there is no restriction on length of parameters..																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is not cleared																								
HW Reset	Contents of memory is not cleared																								
Flow Chart	RAMWR ↓ Image Data D1[7:0],D2[7:0], ...,Dn[7:0] ↓ Any Command Legend Command Parameter Display Action Mode Sequential transfer																								

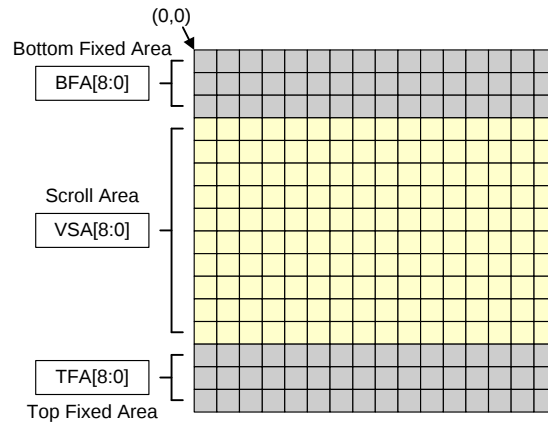
9.2.22. PTLAR: Partial Area (30h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	0	0	30
1 st Parameter	1	↑	1	-	SR[15:8]								
2 nd Parameter	1	↑	1	-	SR[7:0]								
3 rd Parameter	1	↑	1	-	ER[15:0]								
4 th Parameter	1	↑	1	-	ER[7:0]								
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4 (ML) = 0:  If End Row>Start Row when MADCTL B4 (ML) = 1:  If End Row<Start Row when MADCTL B4=0:  If End Row = Start Row then the Partial Area will be one row deep.												

Restriction	SR[15..0] and ER[15..0] cannot be greater than 13Fh.																				
Register Availability	<table><thead><tr><th>Status</th><th colspan="2">Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Sleep In</td><td colspan="2">Yes</td></tr></tbody></table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Partial Mode On, Idle Mode Off, Sleep Out	Yes		Partial Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
Status	Availability																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																				
Partial Mode On, Idle Mode Off, Sleep Out	Yes																				
Partial Mode On, Idle Mode On, Sleep Out	Yes																				
Sleep In	Yes																				
Default	<table><thead><tr><th>Status</th><th colspan="2">Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>SR[15:0] = 0000h</td><td>ER[15:0] = 013Fh</td></tr><tr><td>SW Reset</td><td>SR[15:0] = 0000h</td><td>ER[15:0] = 013Fh</td></tr><tr><td>HW Reset</td><td>SR[15:0] = 0000h</td><td>EC[15:0] = 013Fh</td></tr></tbody></table>			Status	Default Value		Power On Sequence	SR[15:0] = 0000h	ER[15:0] = 013Fh	SW Reset	SR[15:0] = 0000h	ER[15:0] = 013Fh	HW Reset	SR[15:0] = 0000h	EC[15:0] = 013Fh						
Status	Default Value																				
Power On Sequence	SR[15:0] = 0000h	ER[15:0] = 013Fh																			
SW Reset	SR[15:0] = 0000h	ER[15:0] = 013Fh																			
HW Reset	SR[15:0] = 0000h	EC[15:0] = 013Fh																			
Flow Chart	1. To Enter Partial Mode <pre>graph TD; PLTAR[/PLTAR/] --> SR150[/SR[15:0]/]; SR150 --> ER150[/ER[15:0]/]; ER150 --> PTLON[/PTLON/]; PTLON --> PM([Partial Mode]);</pre> 2. To Leave Partial Mode <pre>graph TD; PM([Partial Mode]) --> DISPOFF[/DISPOFF/]; DISPOFF --> NORON[/NORON/]; NORON --> PMOff([Partial Mode Off]); PMOff --> RAMRW[/RAMRW/]; RAMRW --> ID[/Image Data D1[7:0], D1[7:0], ..., Dn[7:0]/];</pre> (option) To prevent Tearing Effect Image displayed Legend - Command - Parameter - Display - Action - Mode - Sequential transfer																				

9.2.23. VSCRDEF: Vertical(Horizontal) Scrolling Definition (33h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	1	1	33
1 st Parameter	1	↑	1	-	SCR_ SEL							TFA[8]	
2 nd Parameter	1	↑	1	-	TFA [7:0]								
3 rd Parameter	1	↑	1	-								VSA[8]	
4 th Parameter	1	↑	1	-	VSA [7:0]								
5 th Parameter	1	↑	1	-								BFA[8]	
6 th Parameter	1	↑	1	-	BFA[7:0]								
Description	This command defines the Vertical/Horizontal Scrolling Area of the display.												
	When SCR_SEL = 0, MADCTL B4 (ML) = 0 The 1st & 2nd parameter TFA[8..0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA[8..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[8..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer. When SCR_SEL = 0, MADCTL B4 (ML) = 1 The 1st & 2nd parameter TFA[8..0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[8..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[8..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).												



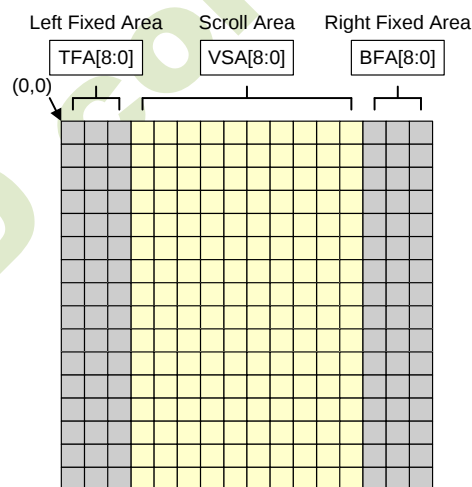
Horizontal Scrolling

When SCR_SEL = 1,

The 1st & 2nd parameter TFA[8..0] describes the Left Fixed Area (in No. of columns from Left of the Frame Memory and Display).

The 3rd & 4th parameter VSA[8..0] describes the width of the Horizontal Scrolling Area (in No. of columns of the Frame Memory [not the display] from the Horizontal Scrolling Start Address) The first columns appears immediately after the right most columns of the Left Fixed Area.

The 5th & 6th parameter BFA[8..0] describes the Right Fixed Area (in No. of columns from Right of the Frame Memory and Display).



Restriction

The condition is $(TFA+VSA+BFA)=320$, otherwise Scrolling mode is undefined.

In Vertical Scroll Mode, MADCTL B5 (MV) should be set to '0' – this only affects the Frame Memory Write.

Register Availability

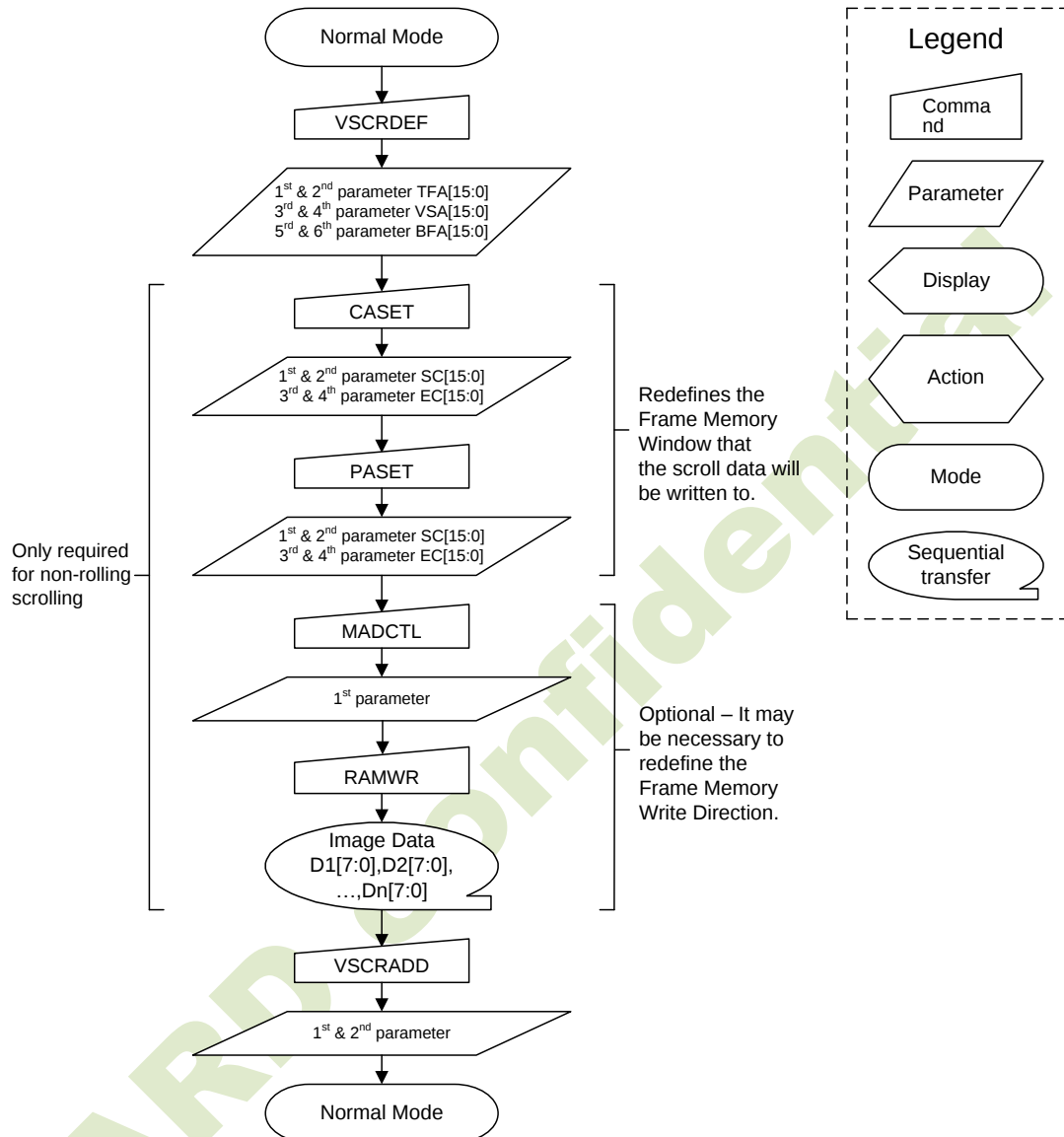
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default			
	Status	Default Value	
	Power On Sequence	TFA[15:0] = 0000h	VSA[15:0] = 0140h BFA[15:0] = 0000h
	SW Reset	TFA[15:0] = 0000h	VSA[15:0] = 0140h BFA[15:0] = 0000h
	HW Reset	TFA[15:0] = 0000h	VSA[15:0] = 0140h BFA[15:0] = 0000h

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1. To enter Vertical Scroll Mode:

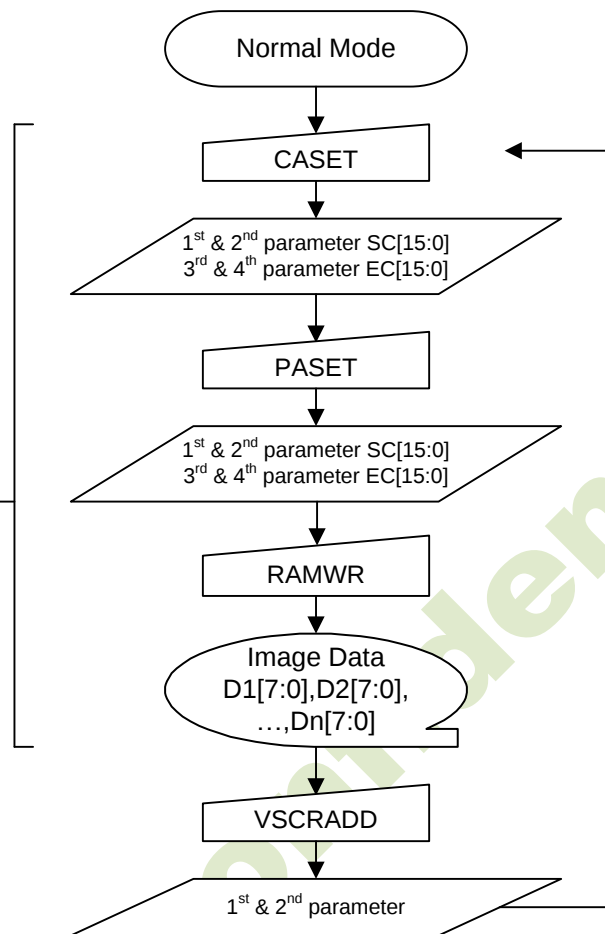
Flow Chart



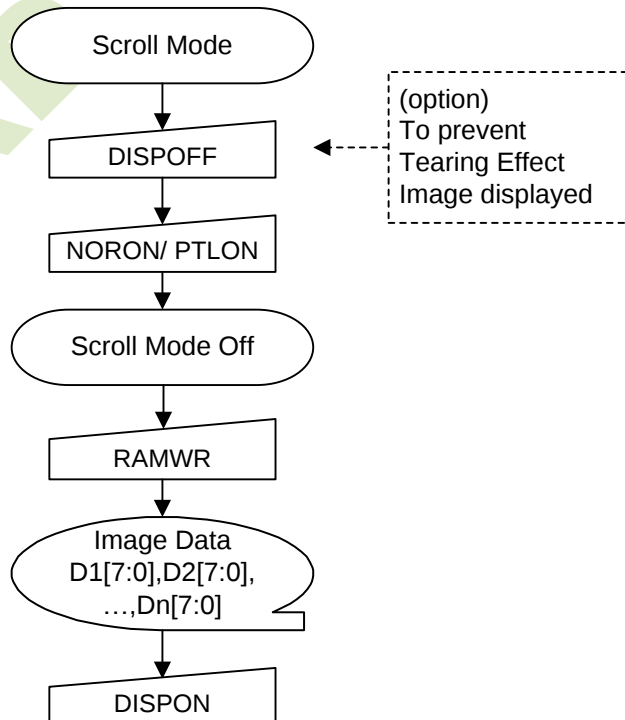
Note The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:

Only required
for non-rolling
scrolling



3. To Leave Vertical Scroll Mode:

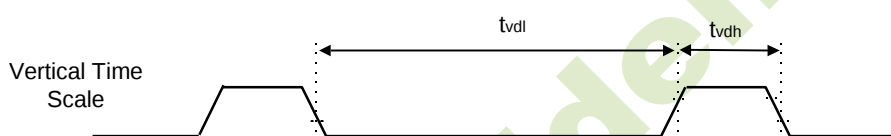
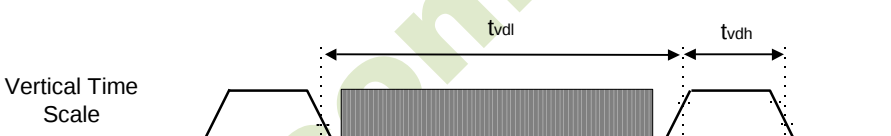


Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

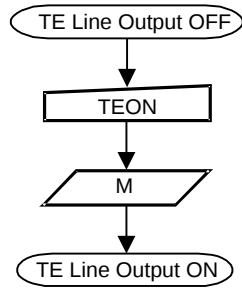
9.2.24. TEOFF: Tearing Effect Line OFF (34h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	1	0	1	0	0	34												
Parameter	No Parameter																								
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.																								
Restriction	This command has no effect when Tearing Effect output is already OFF.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>SW Reset</td><td>Off</td></tr><tr><td>HW Reset</td><td>Off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Off	SW Reset	Off	HW Reset	Off				
Status	Default Value																								
Power On Sequence	Off																								
SW Reset	Off																								
HW Reset	Off																								
Flow Chart	TE Line Output ON ↓ TEOFF ↓ TE Line Output OFF																								

9.2.25. TEON: Tearing Effect Line ON (35h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	1	0	1	0	1	35												
1 st Parameter	1	↑	1	-	X	X	X	X	X	X	X	M													
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care). When M=0: The Tearing Effect Output line consists of V-Blanking information only:  When M=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.																								
	Restriction	This command has no effect when Tearing Effect output is already ON.																							
	Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>SW Reset</td><td>Off</td></tr><tr><td>HW Reset</td><td>Off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Off	SW Reset	Off	HW Reset	Off				
Status	Default Value																								
Power On Sequence	Off																								
SW Reset	Off																								
HW Reset	Off																								

Flow Chart



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9.2.26. MADCTL: Memory Access Control(36h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	0	36
1 st Parameter	1	↑	1	-	B7	B6	B5	B4	B3	B2	B1	B0	

This command defines read/ write scanning direction of frame memory.

This command makes no change on the other driver status.

Bit	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
B2	Horizontal ORDER (MH)	LCD horizontal refresh direction control
B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module

ML - Vertical Updating order

ML= 0

ML= 1

RGB-BGR Order

B3= 0

B3= 1

MH - Horizontal Updating order

MH= 0

MH= 1

Note: Top-Left (0,0) means a physical memory location

Restriction	D1 and D0 are set to '00' internally. D2 is implemented if the LCD is updating pixel-by-pixel. D2 is set to '0' internally if the LCD is updating line-by-line.												
Register Availability	<table> <tr> <th>Status</th><th>Availability</th></tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table> <tr> <th>Status</th><th>Default Value</th></tr> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>SW Reset</td><td>No Change</td></tr> <tr> <td>HW Reset</td><td>00h</td></tr> </table>	Status	Default Value	Power On Sequence	00h	SW Reset	No Change	HW Reset	00h				
Status	Default Value												
Power On Sequence	00h												
SW Reset	No Change												
HW Reset	00h												
Flow Chart	<pre> graph TD A[MADCTL] --> B[/1st parameter B[7:0]/] </pre>												

9.2.27. VSCRSADD: Vertical(Horizontal) Scrolling Start Address (37h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	1	37
1 st Parameter	1	↑	1	-								VSP[8]	
2 nd Parameter	1	↑	1	-	VSP[7:0]								

This command is used together with Vertical(Horizontal) Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When SCR_SEL = 0, MADCTL B4 (ML) = 0

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP = '3'.

(0,0)

Memory

VSP[8:0]

→

(0,319)

0

1

2

3

⋮

⋮

318

319

→

Pointer (ML=0)

→

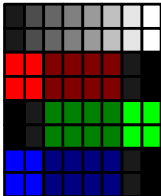
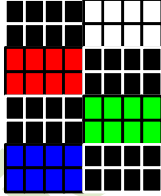
Display

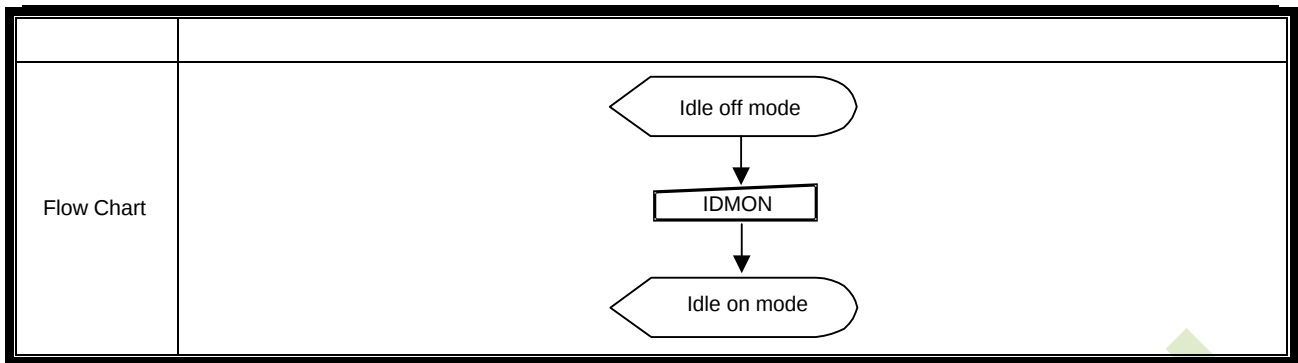
	SCR_SEL = 1 When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP = '3' Memory Display Note1: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. Note3: VSP refers to the Frame Memory line Pointer.												
Restriction	Since the value of the Vertical(Horizontal) Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical(Horizontal) Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	No												
Partial Mode On, Idle Mode On, Sleep Out	No												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000h</td></tr> <tr> <td>SW Reset</td><td>0000h</td></tr> <tr> <td>HW Reset</td><td>0000h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	0000h	SW Reset	0000h	HW Reset	0000h				
Status	Default Value												
Power On Sequence	0000h												
SW Reset	0000h												
HW Reset	0000h												
Flow Chart	See Vertica(Horizontal) Scrolling Definition (33h) description												

9.2.28. IDMOFF: Idle Mode OFF (38h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	1	1	0	0	0	38												
Parameter	No Parameter																								
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262144 colors.																								
Restriction	This command has no effect when module is already in idle off mode.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Idle mode off</td></tr><tr><td>SW Reset</td><td>Idle mode off</td></tr><tr><td>HW Reset</td><td>Idle mode off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Idle mode off	SW Reset	Idle mode off	HW Reset	Idle mode off				
Status	Default Value																								
Power On Sequence	Idle mode off																								
SW Reset	Idle mode off																								
HW Reset	Idle mode off																								
Flow Chart	Idle on mode ↓ IDMOFF ↓ Idle off mode																								

9.2.29. IDMON: Idle Mode ON (39h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	↑	1	-	0	0	1	1	1	0	0	1	39																																			
Parameter	No Parameter																																															
Description	This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.																																															
	(Example) Memory  → Display 																																															
	<table><thead><tr><th>Color</th><th>R₅R₄R₃R₂R₁R₀</th><th>G₅G₄G₃G₂G₁G₀</th><th>B₅B₄B₃B₂B₁B₀</th></tr></thead><tbody><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></tbody></table>													Color	R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₅ B ₄ B ₃ B ₂ B ₁ B ₀	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX
Color	R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₅ B ₄ B ₃ B ₂ B ₁ B ₀																																													
Black	0XXXXX	0XXXXX	0XXXXX																																													
Blue	0XXXXX	0XXXXX	1XXXXX																																													
Red	1XXXXX	0XXXXX	0XXXXX																																													
Magenta	1XXXXX	0XXXXX	1XXXXX																																													
Green	0XXXXX	1XXXXX	0XXXXX																																													
Cyan	0XXXXX	1XXXXX	1XXXXX																																													
Yellow	1XXXXX	1XXXXX	0XXXXX																																													
White	1XXXXX	1XXXXX	1XXXXX																																													
Restriction	This command has no effect when module is already in idle on mode.																																															
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																							
Status	Availability																																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																																															
Sleep In	Yes																																															
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Idle mode off</td></tr><tr><td>SW Reset</td><td>Idle mode off</td></tr><tr><td>HW Reset</td><td>Idle mode off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Idle mode off	SW Reset	Idle mode off	HW Reset	Idle mode off																											
Status	Default Value																																															
Power On Sequence	Idle mode off																																															
SW Reset	Idle mode off																																															
HW Reset	Idle mode off																																															

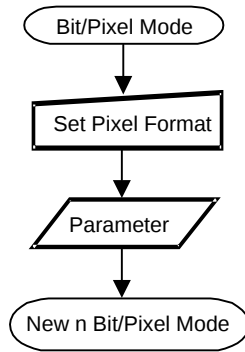


JADARD confidential

9.2.30. COLMOD: Pixel Format Set (3Ah)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	1	0	3A
1 st Parameter	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0	
Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:												
	Bit	Description						Value					
	D7	-						Set to '0'					
	D6	RGB Interface Color Format						'011' = 12 bits/pixel					
	D5							'101' = 16 bits/pixel					
	D4							'110' = 18 bits/pixel					
	D3	-						Set to '0'					
	D2	Control Interface Color Format						'011' = 12 bits/pixel					
	D1							'101' = 16 bits/pixel					
D0	'110' = 18 bits/pixel												
Restriction													
Register Availability													
	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
Sleep In								Yes					
Default													
	Status						Default Value						
	Power On Sequence						18bits/pixel						
	SW Reset						No change						
HW Reset						18bits/pixel							

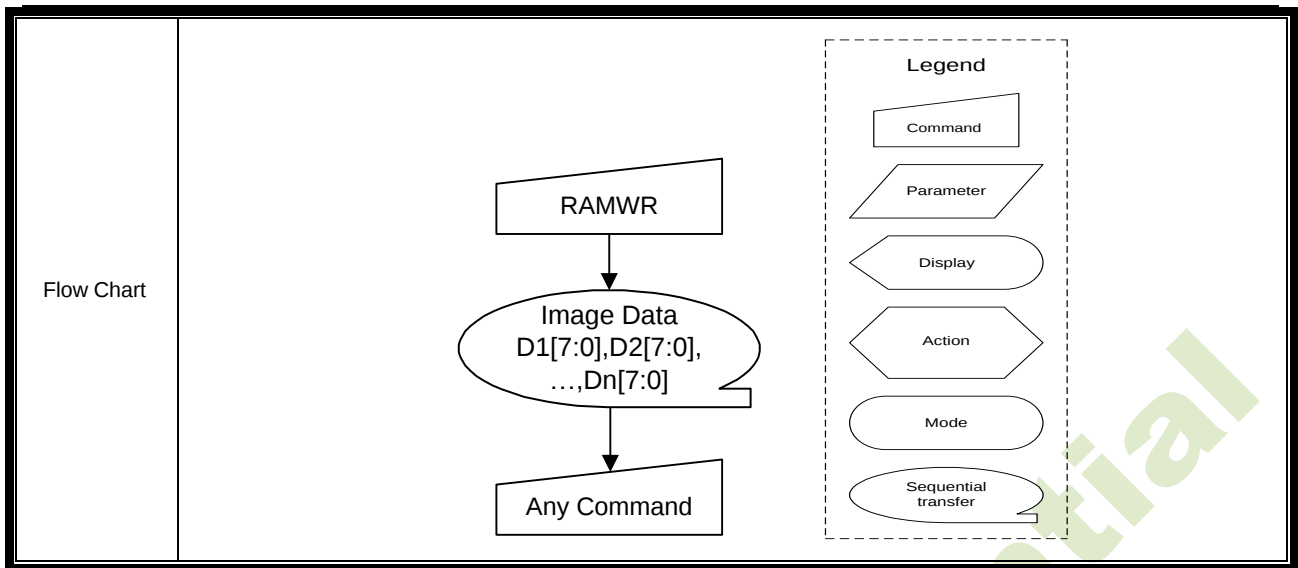
Flow Chart



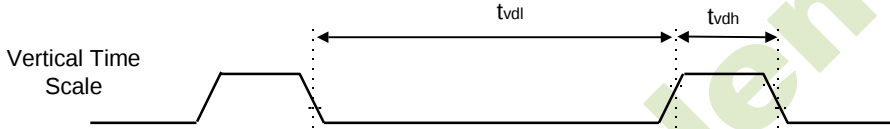
JADARD confidential

9.2.31. WRMEMC: Write Memory Continue (3Ch)

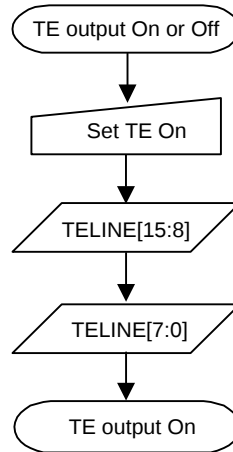
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	0	1	1	1	1	0	0	3C												
1 st Parameter	1	↑	1	D1[8]	D1[7:0]																				
...	1	↑	1	Dx[8]	Dx[7:0]																				
N th Parameter	1	↑	1	Dn[8]	Dn[7:0]																				
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous Write Memory Continue (3Ch) or Memory Write Start (2Ch) command. Sending any other command can stop frame Write. If MATCDL MV = 0: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MATCDL MV = 1: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.																								
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is not cleared																								
HW Reset	Contents of memory is not cleared																								



9.2.32. STE: Set Tear Scanline (44h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	1	0	0	0	1	0	0	44												
1 st Parameter	1	↑	1	-	TELINE[15:8]																				
2 th Parameter	1	↑	1	-	TELINE[7:0]																				
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only: Vertical Time Scale  Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.																								
	Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.																							
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>SW Reset</td><td>0000h</td></tr><tr><td>HW Reset</td><td>0000h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	0000h	SW Reset	0000h	HW Reset	0000h				
Status	Default Value																								
Power On Sequence	0000h																								
SW Reset	0000h																								
HW Reset	0000h																								

Flow Chart



JADARD confidential

9.2.33. GSCAN: Get Scanline (45h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	1	0	0	0	1	0	1	45												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd Parameter	1	1	↑	-	SLN[15:0]																				
3 rd Parameter	1	1	↑	-	SLN [7:0]																				
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scanline is undefined.																								
Restriction	-																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>SW Reset</td><td>0000h</td></tr><tr><td>HW Reset</td><td>0000h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	0000h	SW Reset	0000h	HW Reset	0000h				
Status	Default Value																								
Power On Sequence	0000h																								
SW Reset	0000h																								
HW Reset	0000h																								
Flow Chart	Get scanline Dummy Read SLN[15:8] SLN[7:0]																								

9.2.34. RDABCSD: Read Automatic Brightness Control Self-Diagnostic

Result (68h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	0	1	1	0	1	0	0	0	68												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd Parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0													
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below: D7 – Register Loading Detection D6 – Functionality Detection D5, D4, D3, D2, D1 and D0 are for future use and are set to '0'.																								
Restriction	-																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
SW Reset	00h																								
HW Reset	00h																								
Flow Chart	Serial I/F Mode <pre>graph TD; A[RDCABC] --> B[/Send 2nd parameter/];</pre> Parallel I/F Mode <pre>graph TD; A[RDCABC] --> B[/Dummy Read/]; B --> C[/Send 2nd parameter/];</pre>																								

9.2.35. RDID1: Read ID1 (DAh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	1	1	0	1	1	0	1	0	DA												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd Parameter	1	1	↑	-	module's manufacture[7:0]																				
Description	This read byte identifies the LCD module's manufacturer.																								
Restriction	-																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>98h</td></tr><tr><td>SW Reset</td><td>98h</td></tr><tr><td>HW Reset</td><td>98h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	98h	SW Reset	98h	HW Reset	98h				
Status	Default Value																								
Power On Sequence	98h																								
SW Reset	98h																								
HW Reset	98h																								
Flow Chart	Serial I/F Mode <pre>graph TD; RDID1[RDID1] --> SendParam[Send 2nd parameter];</pre> Parallel I/F Mode <pre>graph TD; RDID1[RDID1] --> DummyRead[/Dummy Read/]; DummyRead --> SendParam2[/Send 2nd parameter/];</pre>																								

9.2.36. RDID2: Read ID2 (DBh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	1	1	0	1	1	0	1	1	DB												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd Parameter	1	1	↑	-	LCD module/driver version[7:0]																				
Description	This read byte is used to track the LCD module/driver version.																								
Restriction	-																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>51h</td></tr><tr><td>SW Reset</td><td>51h</td></tr><tr><td>HW Reset</td><td>51h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	51h	SW Reset	51h	HW Reset	51h				
Status	Default Value																								
Power On Sequence	51h																								
SW Reset	51h																								
HW Reset	51h																								
Flow Chart	Serial I/F Mode <pre>graph TD; RDID2[RDID2] --> SendParam[/Send 2nd parameter/];</pre> Parallel I/F Mode <pre>graph TD; RDID2[RDID2] --> DummyRead[/Dummy Read/]; DummyRead --> SendParam[/Send 2nd parameter/];</pre>																								

9.2.37. RDID3: Read ID3 (DCh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	↑	1	-	1	1	0	1	1	1	0	0	DC												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd Parameter	1	1	↑	-	LCD module/driver ID[7:0]																				
Description	This read byte identifies the LCD module/driver.																								
Restriction	-																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>SW Reset</td><td>00h</td></tr><tr><td>HW Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
SW Reset	00h																								
HW Reset	00h																								
Flow Chart	Serial I/F Mode Parallel I/F Mode																								

9.3. Uesr Command

TBD

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10. Electrical Characteristics

10.1. Absolute maximum ratings

Symbol	Parameter	Unit	Value	Note
IOVCC	Interface Supply Voltage	V	-0.3 to +3.6	Note ^{(3),(4)}
VCI	Logic Supply Voltage	V	-0.3 to +3.6	Note ^{(3),(5)}
AVDD	Positive Voltage input	V	-0.3 to +6.6	Note ⁽⁶⁾
AVEE	Negative Voltage input	V	0 to -6.0	Note ⁽⁷⁾
VGH	Power Supply Voltage	V	-0.3 to +18	Note ⁽⁸⁾
VGL	Power Supply Voltage	V	0 to -16	Note ⁽⁹⁾
Top	Operating Temperature	°C	-40 to +85	Note ⁽¹⁰⁾
Tstg	Storage Temperature	°C	-55 to +110	Note ⁽¹¹⁾

Note: (1) Permanent device damage may occur if absolute maximum conditions are exceeded.

(2) Functional operation should be restricted to the conditions described under DC Characteristics.

(3) IOVCC, VSSD must be maintained.

(4) To make sure $IOVCC \geq VSSD$.

(5) To make sure $VCI \geq AVSS$.

(6) To make sure $AVDD \geq AVSS$.

(7) To make sure $AVSS \geq VSEE$.

(8) To make sure $VGH \geq AVSS$.

(9) To make sure $AVSS \geq VGL$

$VGH + |VGL| < 30V$

(10) For die and wafer products, specified up to +85°C

(11) This temperature specifications apply to the TCP package.

10.2. DC Characteristics

($T_A = -40 \sim 85^\circ\text{C}$, $V_{CI} = 2.6 \sim 3.3\text{V}$, $IOVCC = 1.65 \sim 3.3\text{V}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IOVCC	V_{IN}	Interface Supply Voltage	1.65	-	3.3	V
VCI	V_{IN}	Analog Supply Voltage	2.6	-	3.3	V
VCCH	V_{IN}	High speed interface Supply Voltage	1.65	-	3.3	V
Input high voltage	V_{IH}	IOVCC= 1.65 ~ 3.3V VCI= 2.6 ~ 3.3V	$0.7 \cdot IOVCC$	-	IOVCC	V
Input low voltage	V_{IL}		0	-	$0.3 \cdot IOVCC$	V
VPP	V_{IH}	VPP	8.0V	8.25V	8.5V	V
	V_{IL}					
Output high voltage (SDO, LEDPWM)	V_{OH1}	$I_{OH} = -1.0 \text{ mA}$	$0.8 \cdot IOVCC$	-	IOVCC	V
Output low voltage (SDO, LEDPWM)	V_{OL1}	IOVCC= 1.65 ~ 2.4V $I_{OL} = 1.0 \text{ mA}$	0	-	$0.2 \cdot IOVCC$	V
Logic High level input current	I_{IH}	VSYN, HSYN	-	-	1	μA
		RESX, DCX_SCL, CSX, RDX, WRX_SCL	-	-	1	μA
	I_{IHD}	DB[8...0], SDI, DCX	-	-	1	μA
		DB[8...0]	-	-	1	μA
Logic Low level input current	I_{IL}	VSYN, HSYN	-1	-		μA
		RESX, DCX, CSX, RDX, WRX_SCL	-1	-		μA
	I_{ILD}	DB[8...0], SDI, DCX	-1	-		μA
		DB[8...0]	-1	-		μA
Current consumption Sleep In mode	I_{IOVCC}	VCI=2.8V, IOVCC=1.8V $T_A = 25^\circ\text{C}$	-	TBD	-	μA
	I_{VCI}		-	TBD	-	μA

10.3. AC Characteristics

10.3.1. 8080 Series Parallel 9/8-bit Interface Characteristics

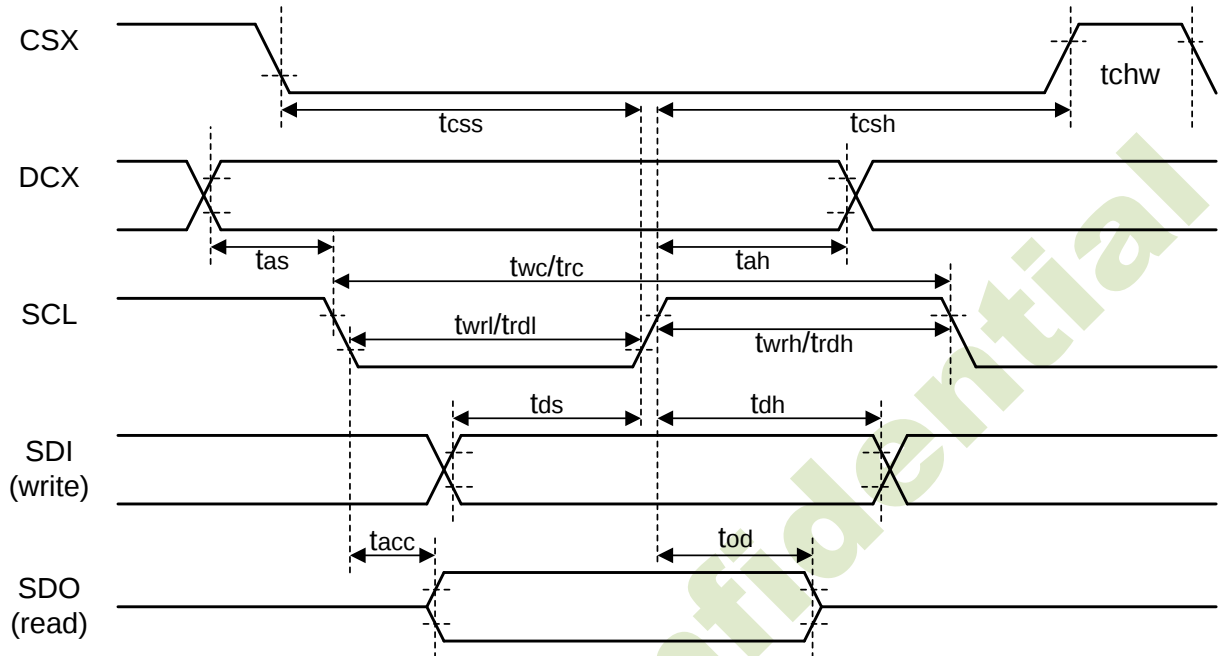


Figure. 10.1 8080 Series Parallel interface Timing Characteristics

($T_A=25^{\circ}\text{C}$, $\text{IOVCC}=1.8\text{V}$, $\text{VCIP}=2.8\text{V}$, $\text{VCI}=2.8\text{V}$)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (write/read)	10	-	ns	
CSX	tchw	CSX "H" Pulse Width	0		ns	
	tcs	Chip select setup time (write)	15		ns	
	trcs	Chip select setup time (read ID)	45		ns	
	trcsfm	Chip Select setup time (read FM)	355		ns	
	tcsf	Chip select wait time (write/read)	10		ns	
	tcsh	Chip select hold time	10		ns	
	tchw	Chip select "H" pulse width	40		ns	
	twc	Write cycle	66		ns	
WRX	twrh	Control pulse "H" duration	15		ns	
	twrl	Control pulse "L" duration	15		ns	
	trc	Read cycle (ID)	160		ns	
RDX(ID)	trdh	Control pulse "H" duration (ID)	90		ns	
	trdl	Control pulse "L" duration (ID)	45		ns	
	trcfm	Read cycle (FM)	450		ns	
RDX(FM)	trdhfm	Control pulse "H" duration (FM)	90		ns	
	trdlfm	Control pulse "L" duration (FM)	355		ns	
D[8:0]	Tdst	Data setup time	10		ns	
	tdht	Data hold time	10		ns	
	trat	Read access time (ID)		40	ns	
	tratfm	Read access time (FM)		340	ns	
	todh	Output disable time	20	80	ns	

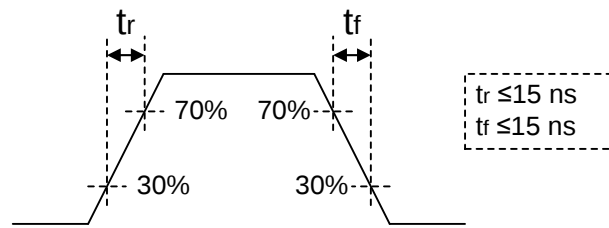


Figure. 10.2 Input rise and fall times

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10.3.2. Serial Interface Timing Characteristics (3-line SPI)

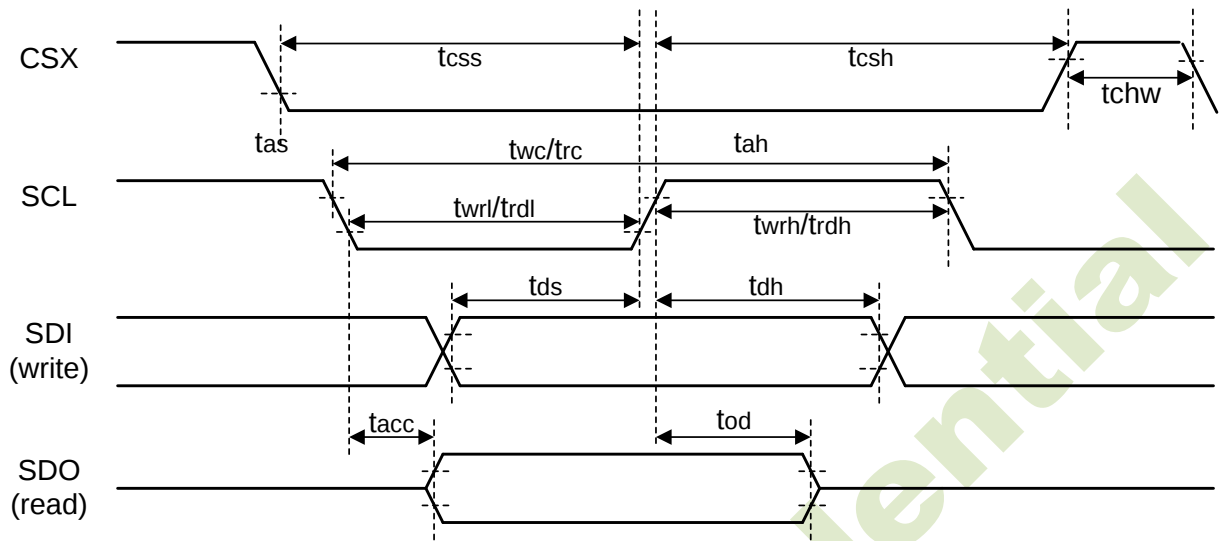


Figure. 10.3 3-line Serial Interface Timing Characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css}	Chip select setup time (Write)	15		ns	
	t_{csh}	Chip select setup time (Write)	15		ns	
	t_{css}	Chip select hold time (Read)	60		ns	
	t_{csh}	Chip select hold time (Read)	65		ns	
	t_{chwh}	Chip select "H" pulse width	40		ns	
SCL (write)	t_{wc}	Write cycle	16		ns	
	t_{wrh}	Control pulse "H" duration	7		ns	
	t_{wrl}	Control pulse "L" duration	7		ns	
SCL (read)	t_{rc}	Read cycle	150		ns	
	t_{rdh}	Control pulse "H" duration	60		ns	
	t_{rdl}	Control pulse "L" duration	60		ns	
SDI/SDO (write)	t_{ds}	Data setup time	7		ns	
	t_{dt}	Data hold time	7		ns	
SDI/SDO (read)	t_{acc}	Read access time	20		ns	
	t_{od}	Output disable time	25		ns	

10.3.3. Serial Interface Timing Characteristics (4-line SPI)

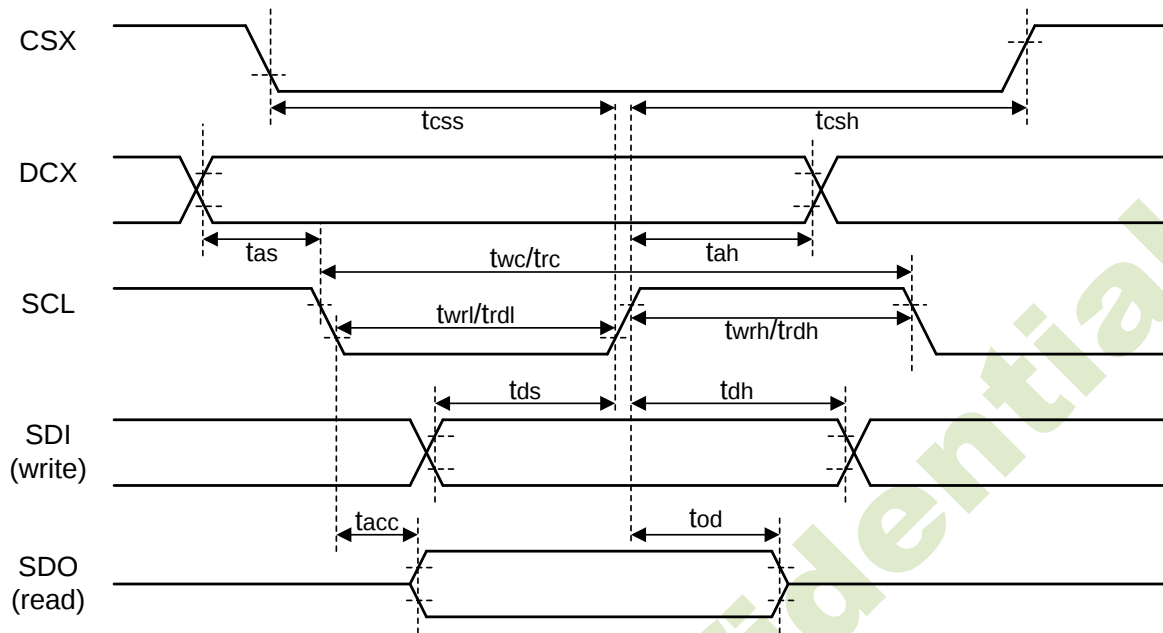


Figure. 10.4 4-line Serial Interface Timing Characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css}	Chip select setup time (Write)	15		ns	
	t_{csh}	Chip select setup time (Write)	15		ns	
	t_{css}	Chip select hold time (Read)	60		ns	
	t_{csh}	Chip select hold time (Read)	65		ns	
DCX	t_{as}	Address setup time	10		ns	
	t_{ah}	Address hold time (Write/Read)	10		ns	
SCL (write)	t_{wc}	Write cycle	16		ns	
	t_{wrh}	Control pulse "H" duration	7		ns	
	t_{wrl}	Control pulse "L" duration	7		ns	
SCL (read)	t_{rc}	Read cycle	150		ns	
	t_{rdh}	Control pulse "H" duration	60		ns	
	t_{rdl}	Control pulse "L" duration	60		ns	
SDI/SDO (write)	t_{ds}	Data setup time	7		ns	
	t_{dt}	Data hold time	7		ns	
SDI/SDO (read)	t_{racc}	Read access time	20		ns	
	t_{od}	Output disable time	25		ns	

10.3.4. QSPI Timing Characteristics

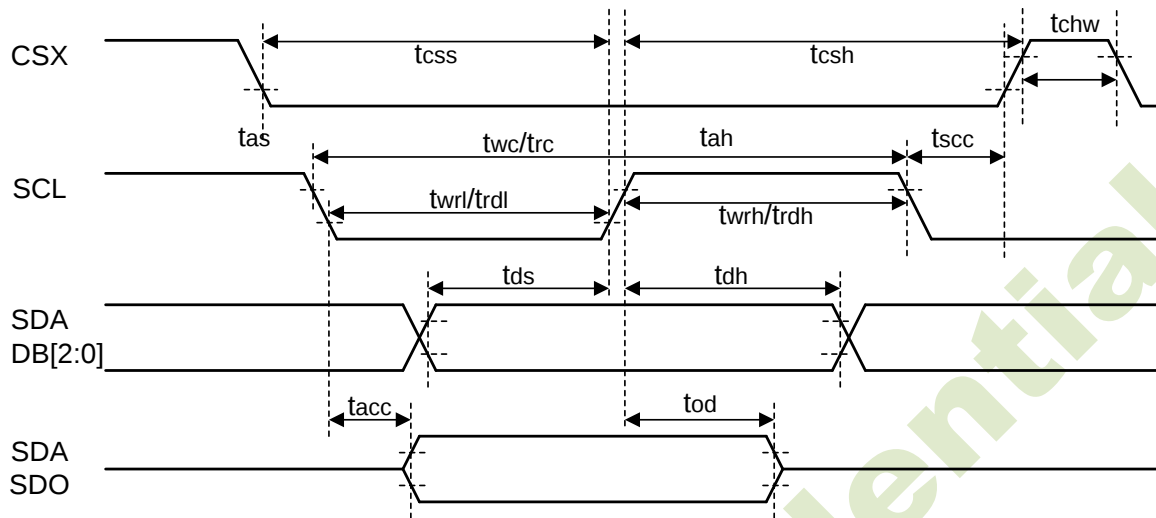


Figure 10.5 QSPI Timing Characteristics

($T_A=25^{\circ}\text{C}$, $\text{IOVCC}=\text{VCC}=1.8\text{V}$, $\text{VCIA}=\text{VCIB}=\text{VCIR}=2.8\text{V}$)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	tcsw	Chip select setup time (write)	10		ns	
	tchsh	Chip select hold time (write)	15		ns	
	tcsw	Chip select setup time (read)	130		ns	
	tsccl	Chip select hold time (read)	65		ns	
	tchwl	Chip select "H" pulse width	40		ns	
SCL (write)	twc	Write cycle	20		ns	
	twrh	Control pulse "H" duration	10		ns	
	twrl	Control pulse "L" duration	10		ns	
SCL (read)	trc	Read cycle	150		ns	
	trdh	Control pulse "H" duration	75		ns	
	trdl	Control pulse "L" duration	75		ns	
SDI/DCX/D[1:0] (write)	tds	Data setup time	5.7		ns	
	tdt	Data hold time	5		ns	
SDO (read)	tracc	Read access time	20		ns	
	tod	Output disable time	25		ns	

Table 10.1 QUAD SPI AC characteristics

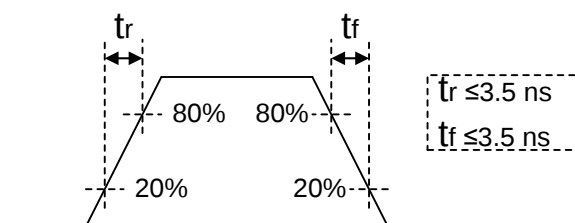
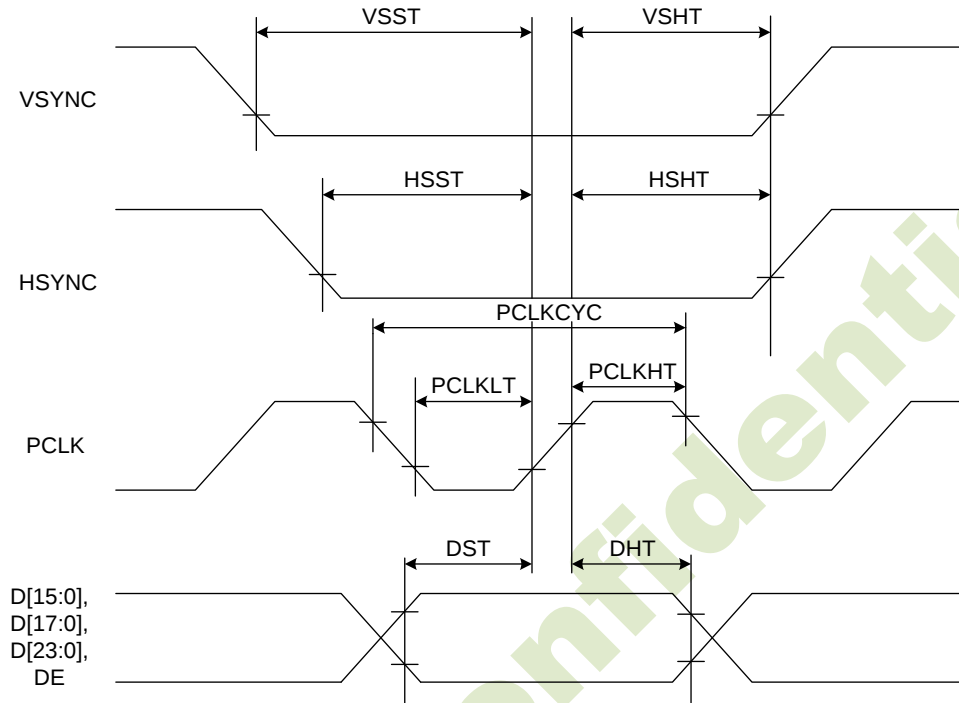


Figure 10.6 SCL rise and fall time

10.3.5. RGB Interface Timing Characteristics

General Timings for RGB I/F



$T_A=25^{\circ}\text{C}$, $\text{IOVCC}=1.8\text{V}$, $\text{VCI}=2.8\text{V}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	30	-	-	ns
Vertical sync. hold time	VSHT	-	30	-	-	ns
Horizontal sync. setup time	HSST	-	30	-	-	ns
Horizontal sync. hold time	HSHT	-	30	-	-	ns
Pixel clock cycle when RGB I/F is running	PCLKCYC	-	120	-	-	ns
Pixel clock low time	PCLKLT	-	60	-	-	ns
Pixel clock high time	PCLKHT	-	60	-	-	ns
Data setup time D[23:0]	DST	-	50	-	-	ns
Data hold time D[23:0]	DHT	-	50	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Measuring of input signals are using $0.30 \times \text{IOVCC}$ for low state and $0.70 \times \text{IOVCC}$ for high state.

10.3.6. Reset Input Timing

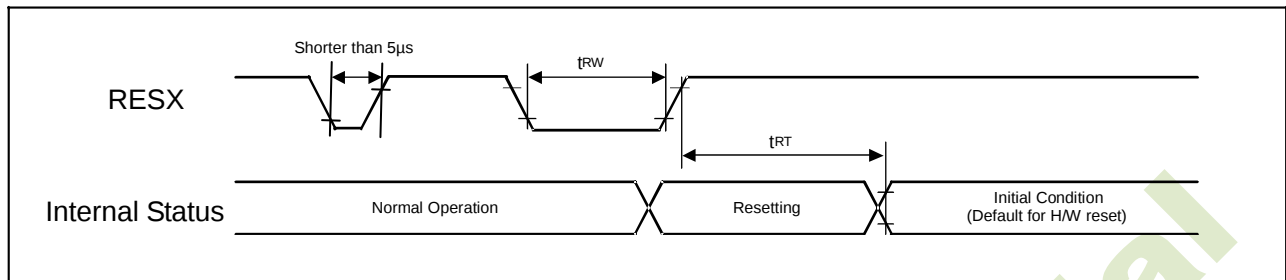


Figure. 10.7 Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width ⁽²⁾	RESX	10	-	μs
t_{RT}	Reset complete time ⁽³⁾	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

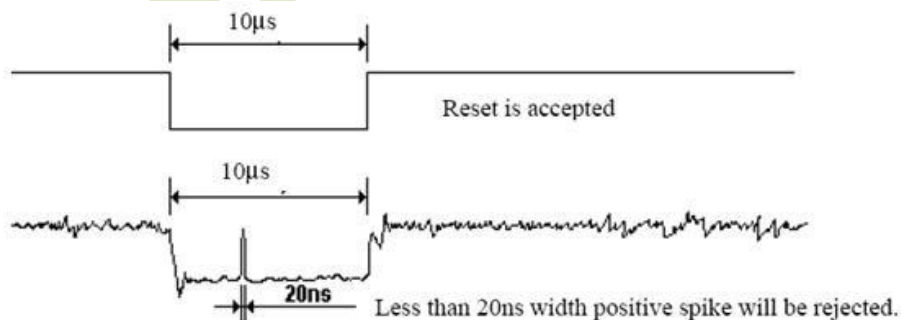
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.