PREPARED BY: DATE		SPEC No. LD-K24Z07
		FILE No.
APPROVED BY: DATE		ISSUE : Dec, 20, 2012
		PAGE :

LIQUID CRYSTAL DISPLAY GROUP
Sakai Display Products Corporation

SPECIFICATION

MODEL No.

DEVICE SPECIFICATION FOR

TFT-LCD Open Cell

JE400D3HC2N

Tentative

CUSTOMER'S APPROVAL

DATE

PRESENTED

BY

BY

K.Kobayashi
Center General Manager
Technology Center
Liquid Crystal Display Business Group
Sakai Display Products Corporation

RECORDS OF REVISION

MODEL No. : JE400D3HC2N

SPEC No. : LD-K24Z07

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-K24Z07	2012/12/20	-	-	-	1st ISSUE

1 Application

This specification applies to the color 40.0” TFT-LCD Open Cell JE400D3HC2N.
（With parts (S-Dr, G-Dr, S-PWB) to drive it.）

* This specification sheets are proprietary products of Sakai Display Products Corporation (“SDP”) and include materials protected under copyright of SDP. Do not reproduce or cause any third party to reproduce them in any form or by any means, electronic or mechanical, for any purpose, in whole or in part, without the express written permission of SDP.

* In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

* Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

* SDP assumes no responsibility for any damage resulting from the use of the device that does not comply with the instructions and the precautions specified in these specification.

* Contact and consult with the SDP sales representative for any questions about this device.

2 Overview

This Open Cell (JE400D3HC2N) is a color active matrix LCD PANEL incorporating amorphous silicon TFT (Thin Film Transistor), Polarizers, Source-PWBs, Source-Drivers, Gate-Drivers and Control-PWB(C-PWB). The following content can be achieved in using C-PWB (JE0DZ1C0010) that SDP specifies.

Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with one billion colors by using 10bit LVDS (Low Voltage Differential Signaling) to interface, +12V of DC supply voltages.

In order to improve the response time of LCD, This C-PWB applies the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With combination of this technologies, motion blur can be reduced and clearer display performance can be realized.

[Caution] You should design thermal conductive interface pad and C-PWB cover enough to radiate heat from T-CON IC in C-PWB.

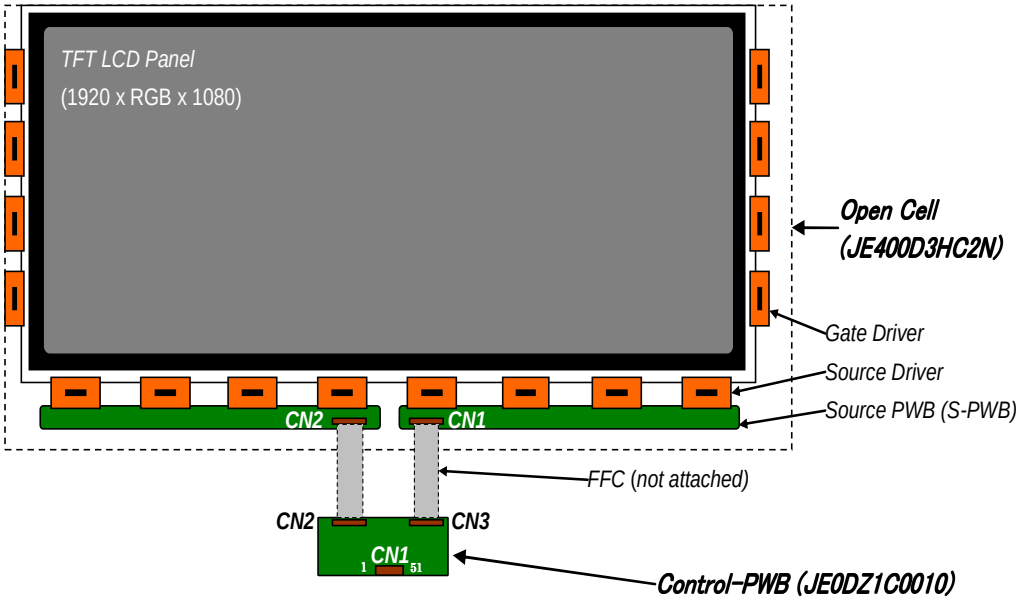


Fig.1 Overview of Open-Cell: JE400D3HC2N and C-PWB

3 Mechanical Specifications

Parameter	Specifications	Unit
Display size	101.61 （Diagonal）	cm
	40.00 （Diagonal）	inch
Active area	885.60(H) x 498.15 (V)	mm
Pixel Format	1920(H) x 1080(V) （1pixel = R + G + B dot）	pixel
Pixel pitch	0.46125 (H) x 0.46125 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Cell Outline Dimensions[Note1]	921.18 (H) x 541.25(V) x 1.66(D)	mm
Mass	1.72±0.3	kg
Surface treatment [Note2]	Anti Glare Hard coating : 2H and more	
Underside Surface treatment [Note2]	Hard coat less	

[Note1] Outline dimensions are shown in P20. Dimension "D" does not include the parts on S-PWB.
[Note2] With the protection film removed.

4 Cell Driving Specifications

4.1 Driving interface of Control PWB SDP specifies

Parts code: JE0DZ1C0010

CN1 (Interface signals and +12V DC power supply) shown in Fig.1

Using connector : 91213-0510 (Aces Electronics Co., Ltd.)

Matching connector : FI-RE51HL, FI-RE51CL (Japan Aviation Electronics Ind., Ltd.) or equivalent device

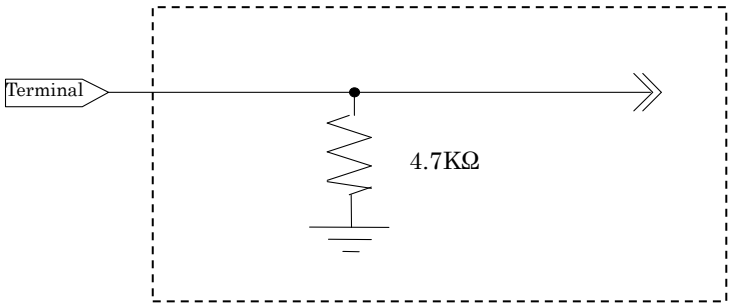
Matching LVDS transmitter : THC63LVD1023 or equivalent device

Pin No.	Symbol	Function	Remark
1	GND		
2	Reserved	It is required to set non-connection(OPEN)	
3	Reserved	It is required to set non-connection(OPEN)	
4	Reserved	It is required to set non-connection(OPEN)	
5	Reserved	It is required to set non-connection(OPEN)	
6	Reserved	It is required to set non-connection(OPEN)	
7	SELLVDS	Select LVDS data order [Note 1,2]	Pull down
8	Reserved	It is required to set non-connection(OPEN)	
9	Reserved	It is required to set non-connection(OPEN)	
10	Reserved	It is required to set non-connection(OPEN)	
11	GND		
12	AIN0-	Aport (-)LVDS CH0 differential data input	
13	AIN0+	Aport (+)LVDS CH0 differential data input	
14	AIN1-	Aport (-)LVDS CH1 differential data input	
15	AIN1+	Aport (+)LVDS CH1 differential data input	
16	AIN2-	Aport (-)LVDS CH2 differential data input	
17	AIN2+	Aport (+)LVDS CH2 differential data input	
18	GND		
19	ACK-	Aport LVDS Clock signal(-)	
20	ACK+	Aport LVDS Clock signal(+)	
21	GND		
22	AIN3-	Aport (-)LVDS CH3 differential data input	
23	AIN3+	Aport (+)LVDS CH3 differential data input	
24	AIN4-	Aport (-)LVDS CH4 differential data input	
25	AIN4+	Aport (+)LVDS CH4 differential data input	
26	GND		
27	GND		
28	BIN0-	Bport (-)LVDS CH0 differential data input	
29	BIN0+	Bport (+)LVDS CH0 differential data input	
30	BIN1-	Bport (-)LVDS CH1 differential data input	

31	BIN1+	Bport (+)LVDS CH1 differential data input	
32	BIN2-	Bport (-)LVDS CH2 differential data input	
33	BIN2+	Bport (+)LVDS CH2 differential data input	
34	GND		
35	BCK-	Bport LVDS Clock signal(-)	
36	BCK+	Bport LVDS Clock signal(+)	
37	GND		
38	BIN3-	Bport (-)LVDS CH3 differential data input	
39	BIN3+	Bport (+)LVDS CH3 differential data input	
40	BIN4-	Bport (-)LVDS CH4 differential data input	
41	BIN4+	Bport (+)LVDS CH4 differential data input	
42	GND		
43	GND		
44	GND		
45	GND		
46	GND		
47	VCC	+12V Power Supply	
48	VCC	+12V Power Supply	
49	VCC	+12V Power Supply	
50	VCC	+12V Power Supply	
51	VCC	+12V Power Supply	

[Note] You should connect GND plane in Control PWB to module chassis.

[Note 1] The equivalent circuit figure of the terminal:



Control PWB

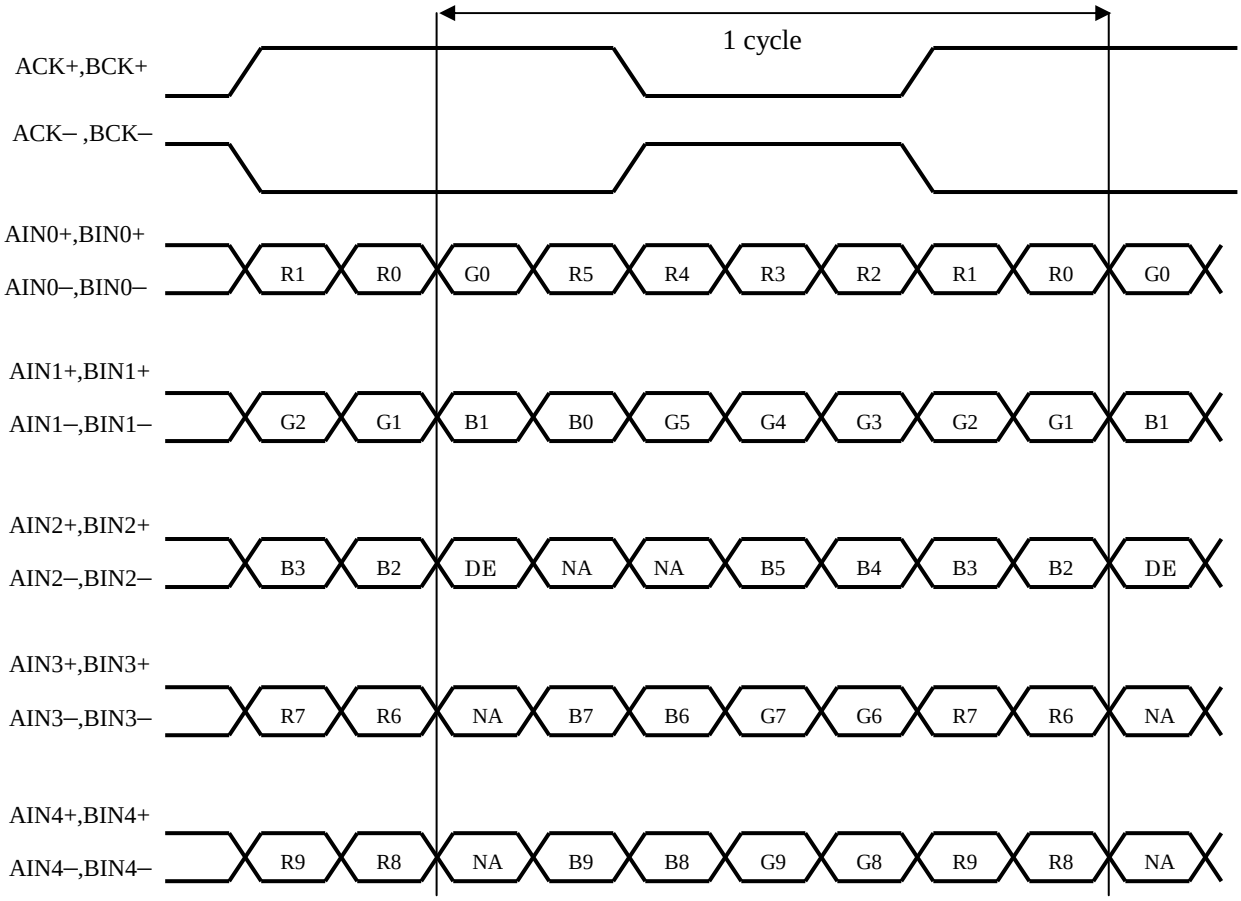
[Note 2] LVDS Data order

SELLVDS		
Data	L(GND) or Open [VESA]	H(3.3V) [JEIDA]
TA0	R0(LSB)	R4
TA1	R1	R5
TA2	R2	R6
TA3	R3	R7
TA4	R4	R8
TA5	R5	R9(MSB)
TA6	G0(LSB)	G4
TB0	G1	G5
TB1	G2	G6
TB2	G3	G7
TB3	G4	G8
TB4	G5	G9(MSB)
TB5	B0(LSB)	B4
TB6	B1	B5
TC0	B2	B6
TC1	B3	B7
TC2	B4	B8
TC3	B5	B9(MSB)
TC4	NA	NA
TC5	NA	NA
TC6	DE(*)	DE(*)
TD0	R6	R2
TD1	R7	R3
TD2	G6	G2
TD3	G7	G3
TD4	B6	B2
TD5	B7	B3
TD6	N/A	N/A
TE0	R8	R0(LSB)
TE1	R9(MSB)	R1
TE2	G8	G0(LSB)
TE3	G9(MSB)	G1
TE4	B8	B0(LSB)
TE5	B9(MSB)	B1
TE6	N/A	N/A

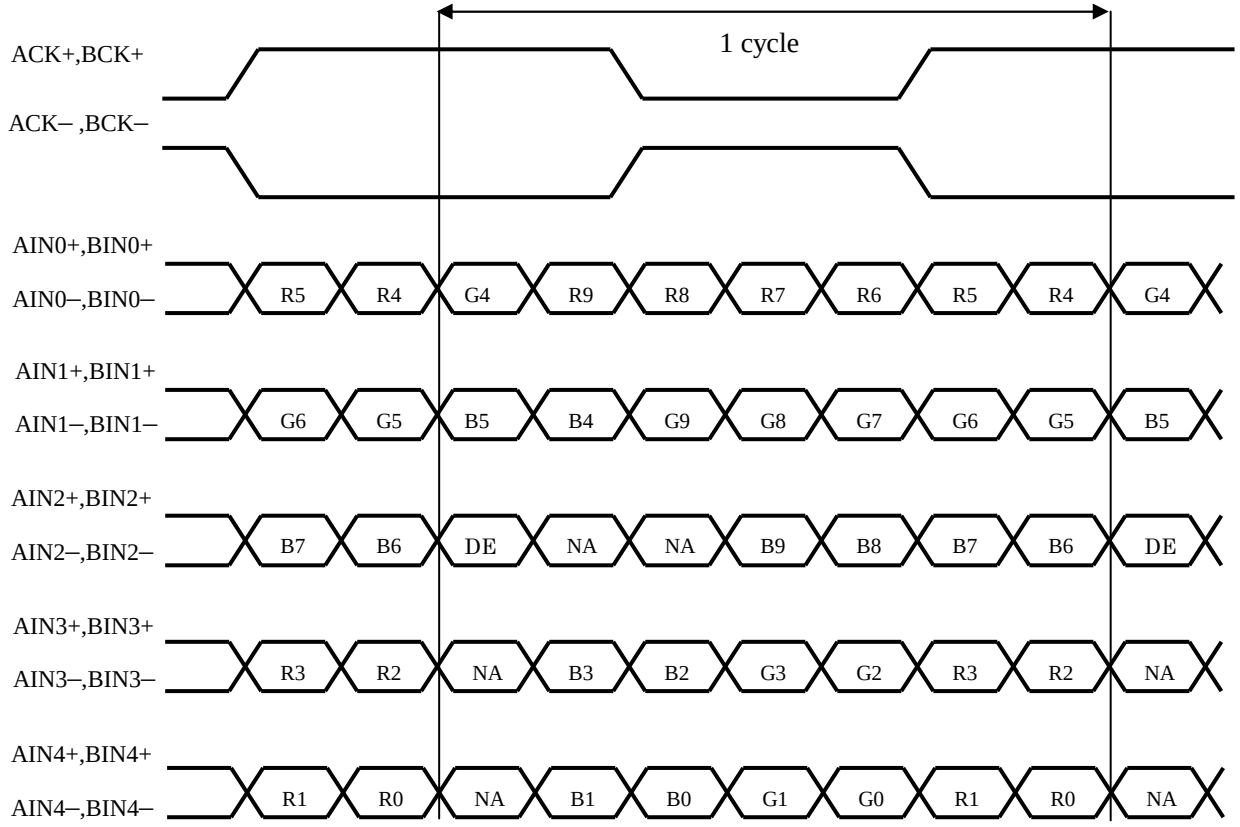
NA: Not Available

(*)Since the display position is prescribed by the rise of DE(Display Enable)signal, please do not fix DE signal at ”High” during operation. And you should input DE signal in all LVDS port.

SELLVDS= Low (GND) or OPEN：VESA



SELLVDS= High (3.3V)：JEIDA



DE: Display Enable, NA: Not Available (Fixed Low)

4.2 Interface block diagram

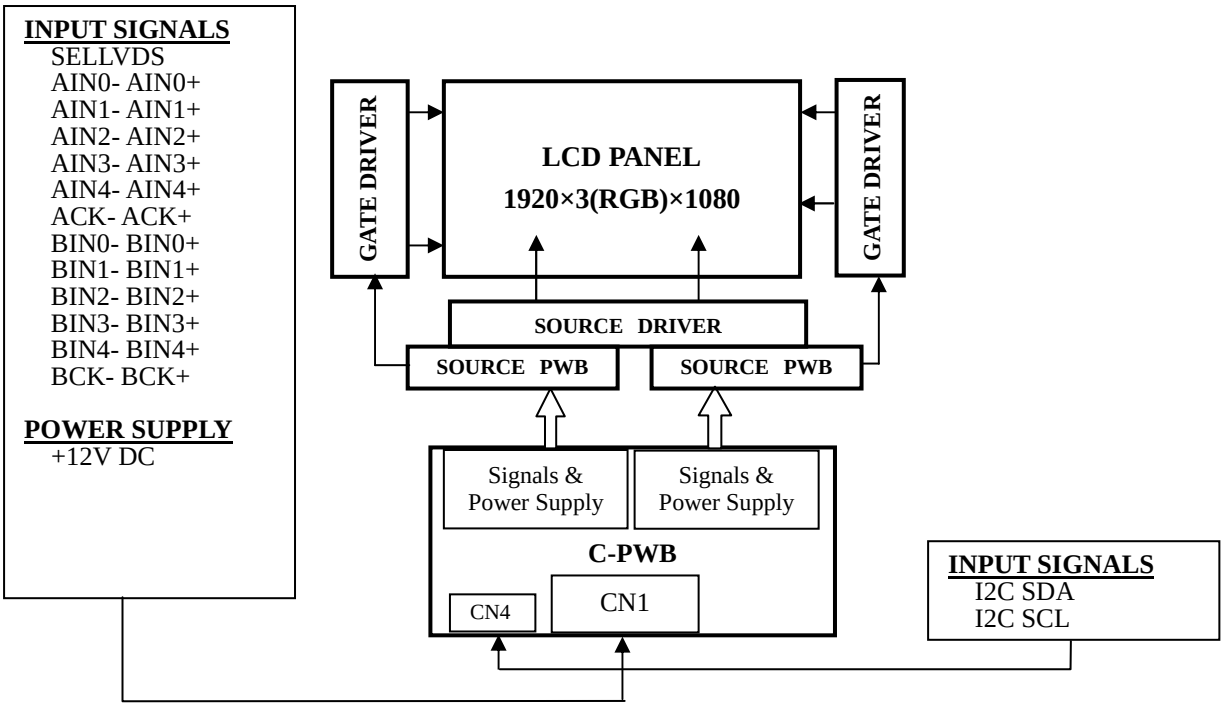
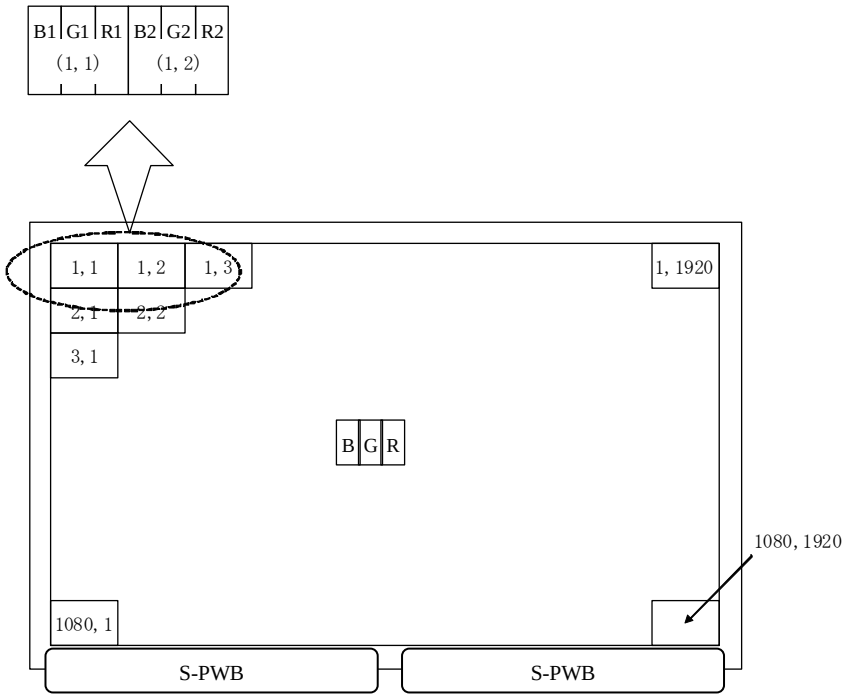


Fig.2 Interface block diagram

4.3 Display position of data



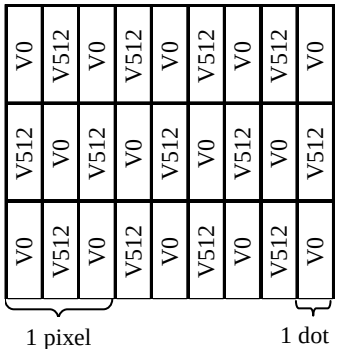
[Note] You should assemble Open-Cell for S-PWBs to be located at the downside of your TV set.

4.4 Vcom Adjusting interface of Control PWB SDP specifies [JE0DZ1C0010]

For the prevention of long-time image sticking of TFT-LCD panel, be sure to adjust Vcom flicker to be minimized on the center of display by visual or flicker meter.

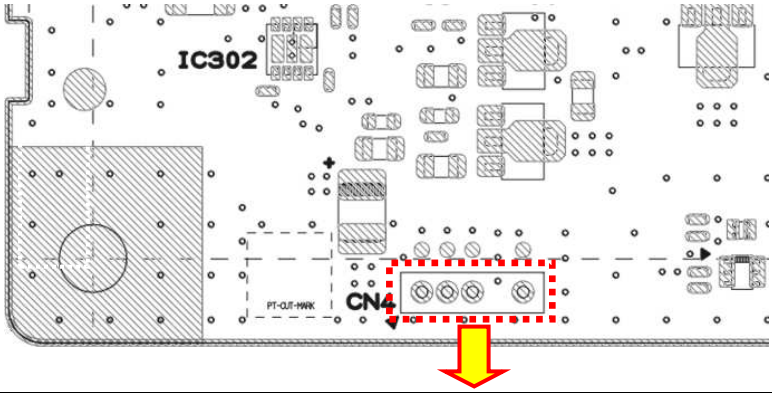
.

[Note 1] Please adjust VCOM voltage at below pattern:



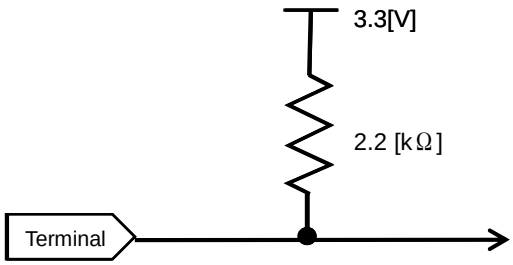
[Note 2] VCOM voltage can be adjusted through via hole (CN4). Potentiometer IC and via hole are as follows:

IC for adjusting VCOM : ISL24837A (Intersil)
Using Via Hole : 1.5mm Pitch (φ0.7mm)
Mating connector : (housing)5P-SZN,
(contact)SZN-002T-P0.7K (JST Co.,Ltd.)
Communication method : I2C



CN4 Pin No.	symbol	Function	Remark
1	SCL	I2C CLK	Pull up:3.3V[Note3]
2	SDA	I2C DATA	Pull up:3.3V[Note3]
3	BUS_EN	—	Required to set NC
4	—	—	
5	GND	GND	-

[Note3] The equivalent circuit figure of the terminal



4.5 Driving interface of S-PWB

CN1 and CN2 on the S-PWB: Input signal from C-PWB

- Using connector: 25P80B120 (ZXEC) or equivalent connector

Pin No.	CN1 on the S-PWB	CN2 on the S-PWB
1	GND	GND
2	Gate Power (L)	Gate Power (L)
3	Gate Power (H)	Gate Power (H)
4	Gate Start Pulse2	Gate Start Pulse 2
5	Gate Start Pulse1	Gate Start Pulse 1
6	Gate Clock	Gate Clock
7	Gate Output Enable	Gate Output Enable
8	Gate Scan Control	Gate Scan Control
9	MPD Control 1	MPD Control 1
10	MPD Control 2	MPD Control 2
11	MPD Control 3	MPD Control 3
12	MPD Control 4	MPD Control 4
13	MPD Control 5	MPD Control 5
14	MPD Control 6	MPD Control 6
15	MPD Control 7	MPD Control 7
16	MPD Control 8	MPD Control 8
17	MPD Control 9	MPD Control 9
18	MPD Control 10	MPD Control 10
19	MPD Control 11	MPD Control 11
20	MPD Control 12	MPD Control 12
21	Vcom	Vcom
22	Gray Level 9 (H)	Gray Level 9 (H)
23	Gray Level 8 (H)	Gray Level 8 (H)
24	Gray Level 7 (H)	Gray Level 7 (H)
25	Gray Level 6 (H)	Gray Level 6 (H)
26	Gray Level 5 (H)	Gray Level 5 (H)
27	Gray Level 4 (H)	Gray Level 4 (H)
28	Gray Level 3 (H)	Gray Level 3 (H)
29	Gray Level 2 (H)	Gray Level 2 (H)
30	Gray Level 1 (H)	Gray Level 1 (H)
31	miniLVDS data(+)	GND
32	miniLVDS data(-)	GND
33	miniLVDS data(+)	GND
34	miniLVDS data(-)	GND
35	miniLVDS data(+)	GND
36	miniLVDS data(-)	GND
37	GND	GND
38	miniLVDS clock(+)	GND
39	miniLVDS clock(-)	GND
40	GND	GND
41	miniLVDS data(+)	GND
42	miniLVDS data(-)	GND
43	miniLVDS data(+)	GND
44	miniLVDS data(-)	miniLVDS Cascade Control 2
45	miniLVDS data(+)	miniLVDS Scan Control
46	miniLVDS data(-)	miniLVDS Cascade Control 1
47	Logic Circuit Power	Logic Circuit Power
48	Logic Circuit Power	Logic Circuit Power

49	Reserved	Reserved
50	Polarity Control	Polarity Control
51	Latch Strobe	Latch Strobe
52	GND	GND
53	miniLVDS Cascade Control 2	miniLVDS data(+)
54	miniLVDS Scan Control	miniLVDS data(-)
55	miniLVDS Cascade Control 1	miniLVDS data(+)
56	GND	miniLVDS data(-)
57	GND	miniLVDS data(+)
58	GND	miniLVDS data(-)
59	GND	GND
60	GND	miniLVDS clock(+)
61	GND	miniLVDS clock(-)
62	GND	GND
63	GND	miniLVDS data(+)
64	GND	miniLVDS data(-)
65	GND	miniLVDS data(+)
66	GND	miniLVDS data(-)
67	GND	miniLVDS data(+)
68	GND	miniLVDS data(-)
69	Analog circuit power	Analog circuit power
70	Analog circuit power	Analog circuit power
71	Gray Level 1 (L)	Gray Level 1 (L)
72	Gray Level 2 (L)	Gray Level 2 (L)
73	Gray Level 3 (L)	Gray Level 3 (L)
74	Gray Level 4 (L)	Gray Level 4 (L)
75	Gray Level 5 (L)	Gray Level 5 (L)
76	Gray Level 6 (L)	Gray Level 6 (L)
77	Gray Level 7 (L)	Gray Level 7 (L)
78	Gray Level 8 (L)	Gray Level 8 (L)
79	Gray Level 9 (L)	Gray Level 9 (L)
80	GND	GND

5 Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage (for Control)	V_I	Ta=25 °C	-0.3 ~ +3.60	V	[Note 1]
12V supply voltage (for Control)	VCC	Ta=25 °C	0 ~ + 14	V	[Note 2]
Storage temperature	Tstg	—	-25 ~ +60	°C	[Note 3]
Operation temperature (Ambient)	Topa	—	0 ~ +50	°C	
Source driver chip surface temperature	Tc	—	+115	℃	[Note 4]

[Note 1] Applies to the input signals to C-PWB SELLVDS, SCL, SDA.

[Note 2] Applies to the supply voltage of C-PWB.

[Note 3] Applies to the JE400D3HC2N(Open-Cell) and C-PWB

- Humidity: 95%RH Max.(Ta ≦ 40°C)
- Maximum wet-bulb temperature at 39°C or less. (Ta > 40°C)
- No condensation.

[Note 4] Recommended operating condition：chip surface temperature ≦ 115℃.

※Please take measures of the heat radiation .

6 Electrical Characteristics of input signals

Ta=25 °C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+12V supply voltage	Supply voltage	Vcc	11.4	12	12.6	V	[Note 1]
	Current dissipation	Icc	-	0.56	1.4	A	[Note 2]
	Inrush current	$I_{RUSH}1$	-	4.0	-	A	t1=500us [Note 4]
Permissible input ripple voltage		V_{RP}	-	-	100	mV_{P-P}	Vcc = +12.0V
Differential input threshold voltage	High	V_{TH}	-	-	100	mV	V_{CM} = +1.2V [Note 3]
	Low	V_{TL}	-100	-	-	mV	
Input Low voltage		V_{IL}	0	-	0.7	V	SELLVDS
Input High voltage		V_{IH}	2.3	3.3	3.6	V	
Input leak current (Low)		I_{IL}	-	-	1500	μA	V_I = 0V SCL,SDA
Input leak current (High)		I_{IH}	-	-	700	μA	V_I = 3.3V SELLVDS
Terminal resistor		R_T	-	100	-	Ω	Differential input

[Note]V_{CM}: Common mode voltage of LVDS driver.

[Note1]

Input voltage sequences

50us < t1 < 20ms

20ms < t2 < 50ms

20ms < t3 < 50ms

0 < t_4 < 1s

1s < t_{5-1} 1s < t_{5-2}

0 < t_{6-1} 0 < t_{6-2}

1s < t_7

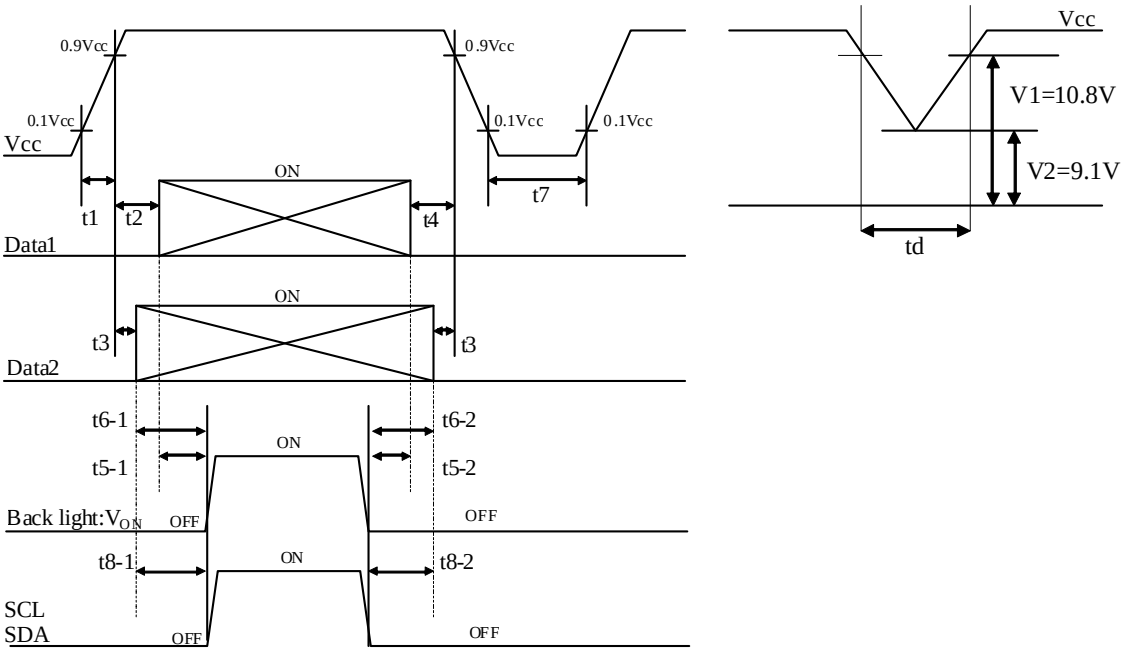
1s < t_{8-1} 1s < t_{8-2}

Dip conditions for supply voltage

9.1V ≦ Vcc < 10.8V

td < 10ms

This case is based on input voltage sequences.



※ Data1: ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±,BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±

※ Data2: SELLVDS

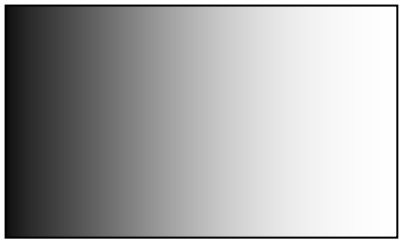
※About the relation between data input and back light lighting, we recommend the above-mentioned input

sequence. If the back light is switched on before a panel operation begins or after a panel operation stops, the screen may not be displayed properly. But this phenomenon is not caused by change of an incoming signal, and does not give damage to a liquid crystal display.

[Note 2] Typical current situation: 1024 gray-bar patterns. (Vcc = +12.0V)

The explanation of RGB gray scale is seen in section 8.

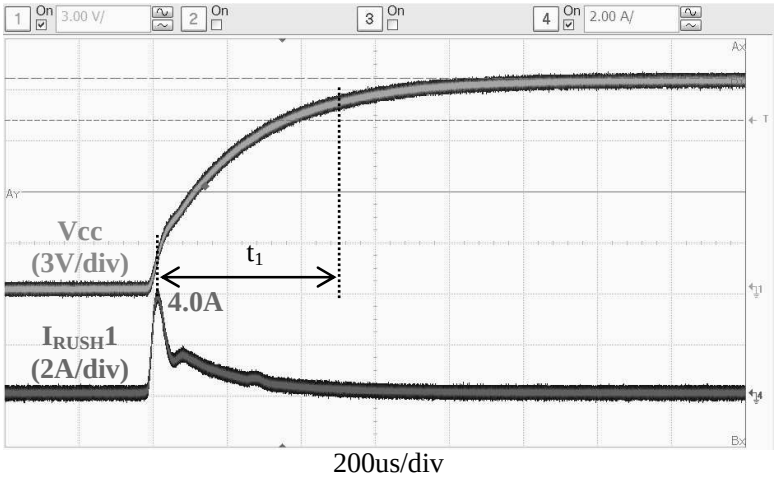
RGB
GS0→GS1→GS2→ ・・・・・・ →GS1023



Vcc＝+12.0V
CK＝74.25MHz
TH＝14.8μs

[Note 3] ACK±, AIN0±, AIN1±, AIN2±, AIN3±, AIN4±, BCK±, BIN0±, BIN1±, BIN2±, BIN3±, BIN4±

[Note 4] Vcc12V inrush current waveform is as follows. (I_{RUSH} : t_1=500us)



200us/div

7 Timing characteristics of input signals for C-PWB

7.1 Timing characteristics

Timing diagrams of input signal are shown in Fig.3.

Parameter		Symbol	Min.	Typ.		Max.	Unit	Remark
				NTSC	PAL			
Clock	Frequency	1/Tc	69	74.25		76	MHz	
Data enable signal	Horizontal period	TH	1050	1100		1300	clock	
			14.2	14.8		16.1	µs	
	Horizontal period (High)	THd	960	960		960	clock	
	Vertical period	TV	1109	1125	1350	1400	line	
			47	60	50	63	Hz	
	Vertical period (High)	TVd	1080	1080		1080	line	

[Note]-When vertical period is very long, flicker and etc. may occur.

-Please turn off the module after it shows the black screen.

-Please make sure that length of vertical period should become of an integral multiple of horizontal length of period. Otherwise, the screen may not display properly.

-As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

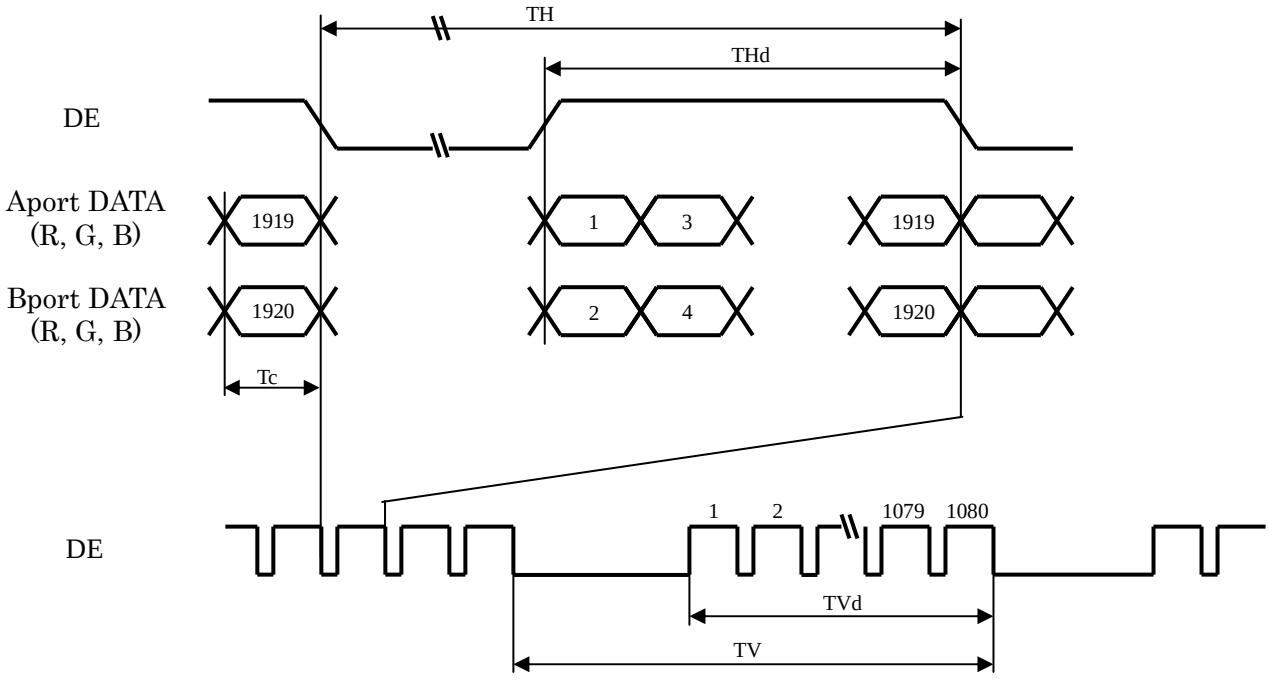
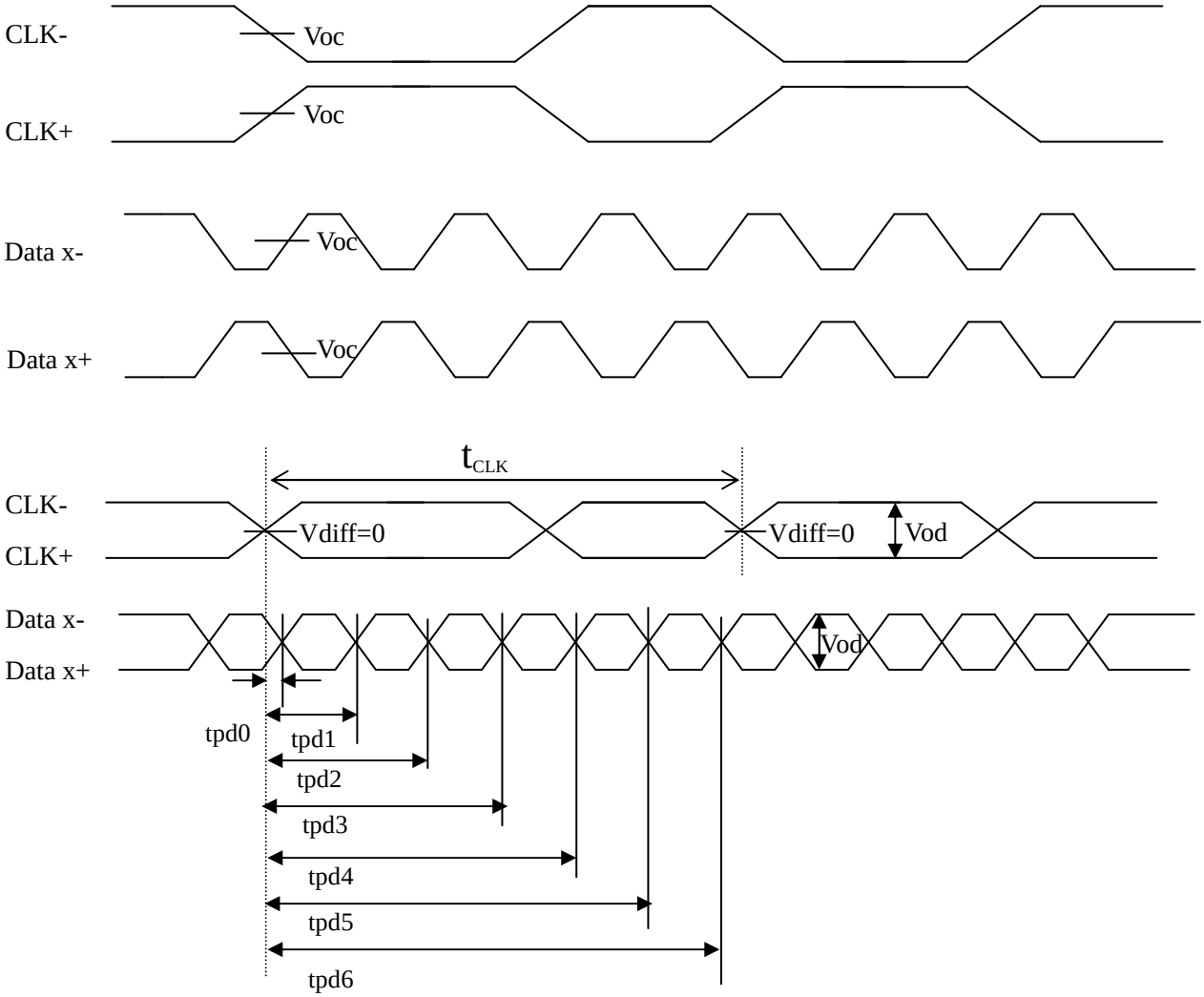


Fig3. Timing characteristics of input signal.

7.2 LVDS signal characteristics



The item		Symbol	min.	typ.	max.	unit
Differential voltage		Vod	200	400	600	mV
Common mode voltage		Voc	600	1200	1800	
LVDS clock period		t_{CLK}	12.35	13.50	13.69	ns
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.25	0	0.25	
	Delay time, CLK rising edge to serial bit position 1	tpd1	1*t_{CLK}/7-0.25	1* t_{CLK} /7	1* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 2	tpd2	2* t_{CLK} /7-0.25	2* t_{CLK} /7	2* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 3	tpd3	3* t_{CLK} /7-0.25	3* t_{CLK} /7	3* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 4	tpd4	4* t_{CLK} /7-0.25	4* t_{CLK} /7	4* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 5	tpd5	5* t_{CLK} /7-0.25	5* t_{CLK} /7	5* t_{CLK} /7+0.25	
	Delay time, CLK rising edge to serial bit position 6	tpd6	6* t_{CLK} 7-0.25	6* t_{CLK} /7	6* t_{CLK} /7+0.25	

8 Input Signal, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Gray Scale	Data signal																													
			R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	⇩	↓					↓										↓										↓					
	⇩	↓					↓										↓										↓					
	Brighter	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	⇩	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage.

Each basic color can be displayed in 1024 gray scales from 10 bits data signals. According to the combination of total 30 bits data signals, one billion-color display can be achieved on the screen.

9 Optical Specifications

Ta=25°C, Vcc=12.0V, Frame rate:60Hz (typical)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21 θ22	CR≧10	80	88	-	Deg.	[Note1,4]
	Vertical	θ11 θ12		80	88	-	Deg.	
Contrast ratio		CRn	θ=0 deg.	4000	5000	-	-	[Note2,4]
Response time		τ_{DRV}		-	6	-	ms	[Note3,4,5]
Chromaticity	White	x		Typ.-0.03	0.281	Typ.+0.03	-	[Note4]
		y		Typ.-0.03	0.285	Typ.+0.03	-	
	Red	x		Typ.-0.03	0.640	Typ.+0.03	-	
		y		Typ.-0.03	0.354	Typ.+0.03	-	
	Green	x		Typ.-0.03	0.324	Typ.+0.03	-	
		y		Typ.-0.03	0.624	Typ.+0.03	-	
	Blue	x		Typ.-0.03	0.152	Typ.+0.03	-	
		y		Typ.-0.03	0.056	Typ.+0.03	-	
Transmittance	White				6.01		%	

-Optical characteristics are based on SDP standard module.

-The measurement shall be executed 60 minutes after lighting at rating.

[Note]The optical characteristics are measured using the following equipment.

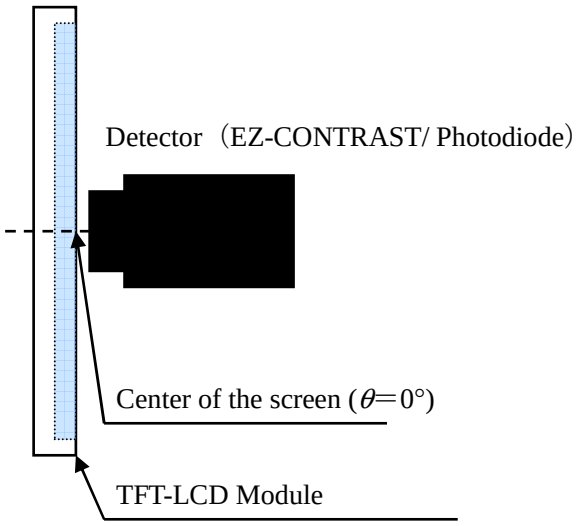


Fig.4-1 Measurement of viewing angle range and Response time.
Viewing angle range: EZ-CONTRAST
Response time: Photodiode

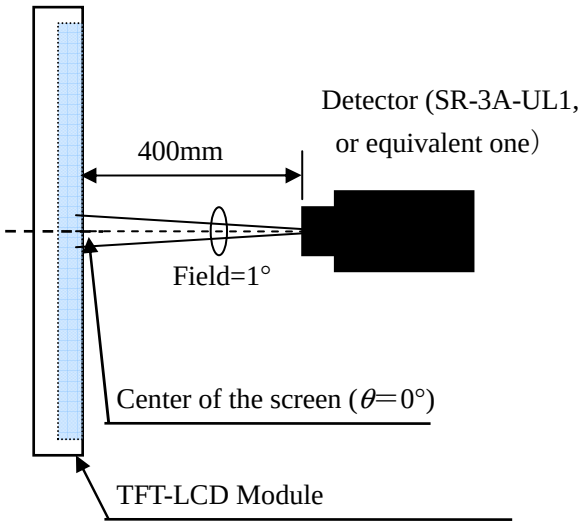
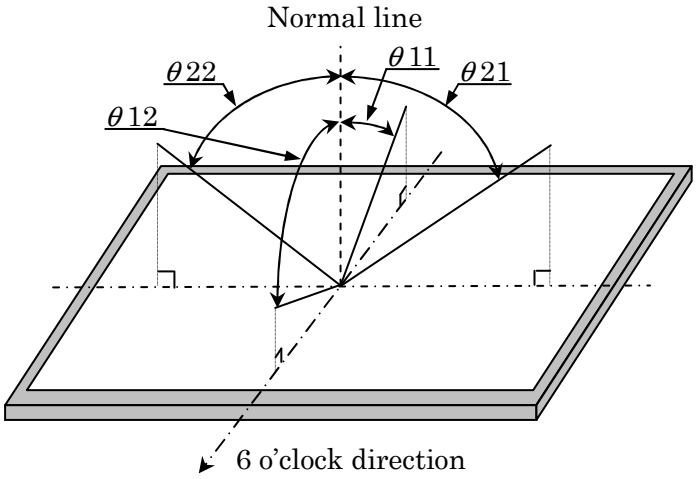


Fig.4-2 Measurement of Contrast, Luminance, Chromaticity.

[Note 1] Definitions of viewing angle range:



[Note 2] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

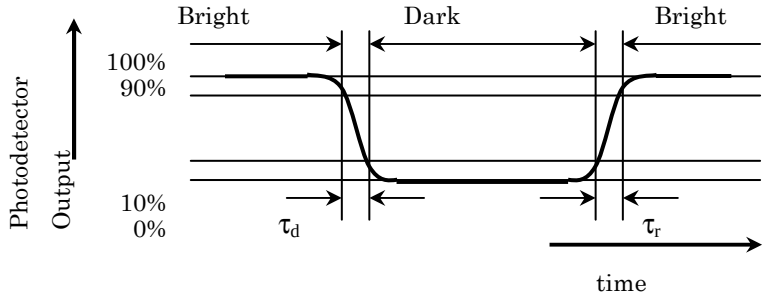
[Note 3] Definition of response time

The response time (τ_d and τ_r) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%)" and "any level of gray (0%, 25%, 50%, 75% and 100%)".

	0%	25%	50%	75%	100%
0%		tr:0%-25%	tr:0%-50%	tr:0%-75%	tr:0%-100%
25%	td: 25%-0%		tr: 25%-50%	tr25%-75%	tr: 25%-100%
50%	td: 50%-0%	td: 50%-25%		tr: 50%-75%	tr: 50%-100%
75%	td: 75%-0%	td: 75%-25%	td: 75%-50%		tr: 75%-100%
100%	td: 100%-0%	td: 100%-25%	td: 100%-50%	td:100%-75%	

t*:x-y...response time from level of gray(x) to level of gray(y)

$\tau_r = \Sigma(tr:x\text{-}y)/10$, $\tau_d = \Sigma(td:x\text{-}y)/10$



[Note 4] This shall be measured at center of the screen.

[Note 5] This value is valid when O/S driving is used at typical input time value.

10 Shipping and Packing

10.1 Packing form

a) Open Cell quantity in 1 cell box : 20 pcs

b) Piling number of cell box : 12 pcs (Max.)

c) 1 palette size : 1390(W)×1150 (D)×1038(H) [mm]

d) Total mass of 1 palette filled with full open cells : 480 kg (Max.)

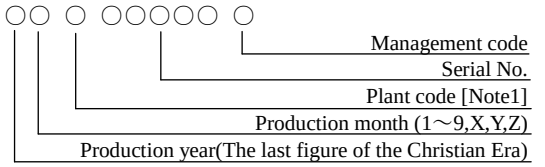
10.2 Label

a) Cell Label

This label is stuck on the protection film of front polarizer. (Please trace the Cell lot number after the film is peeled off.)

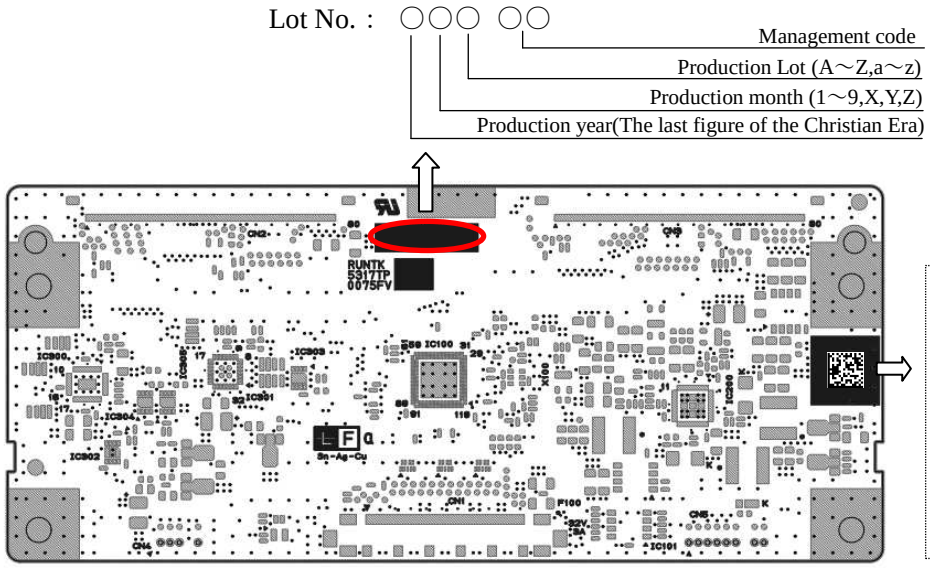
ex) JE400D3HC2NM

How to express Lot No.



[Note1] L:Kameyama, Z:Sakai, N:NSEC, G:SMM, P:SMPL, X:SEMEX

b) C-PWB Label & Lot No.

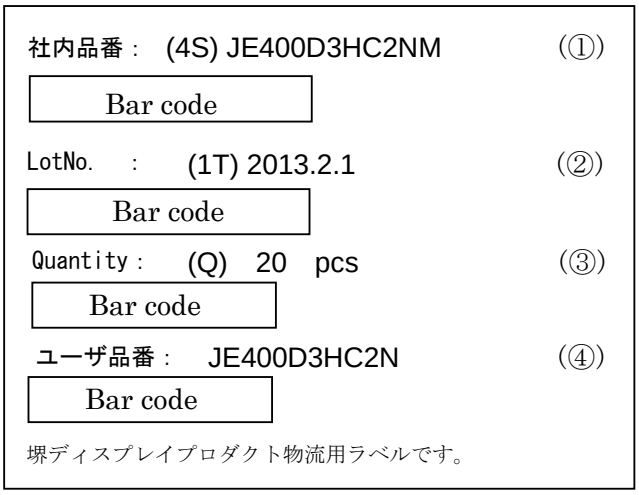


K0075Z 1 - 12Z - HD 000001
① ② ③ ④ ⑤

①Parts code
②Management code
③Production year and months :
The last two figures of the Christian Era + Month (1～9,X,Y,Z)
④Plant code
⑤Serial No.

c) Packing Label

This label is stuck on the packing case (cell box) and carton.



① Model No. & Suffix Code
② Lot No. (Date)
③ Quantity
④ Model No. for USER

11 Carton storage condition.

Temperature	0°C to 40°C
Humidity	95%RH or less
Reference condition	: 20°C to 35°C, 85%RH or less (summer) : 5°C to 15°C, 85%RH or less (winter) ・the total storage time (40°C, 95%RH) : 240H or less
Sunlight	Be sure to shelter a product from the direct sunlight.
Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes	Be sure to put cartons on palette or base, don't put it on the floor, and store them keeping off the wall. Please take care of ventilation in storehouse and around cartons, and control temperature not to exceed the limit one of natural environment.
Storage life	1 year

12 Reliability

Reliability test item:

No.	Test item	Condition
1	High temperature storage test	Ta = 60°C 500h
2	Low temperature storage test	Ta = -25°C 500h
3	High temperature and high humidity operation test	Ta = 40°C ; 95%RH 500h (No condensation)
4	High temperature operation test	Ta = 50°C 500h
5	Low temperature operation test	Ta = 0°C 500h
6	Vibration test (Cell Box with full Open Cells)	X and Y direction: 15min, Z direction: 60min. 5Hz to 50Hz acceleration velocity: 1.0G Sweeping ratio: 3min
7	Drop test (Cell Box with full Open Cells)	Height: 15cm (1 face and 2 sides) Number: 3 times (1 time in each of drop direction)

13 Precautions

1) Be sure to turn off the power supply when inserting or disconnecting the cable.
2) Be sure to design the cabinet so that the Open Cell can be installed without any extra stress such as warp or twist.
3) Since the polarizer is easily damaged, pay attention not to scratch it.
4) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
5) When the polarizer is soiled, wipe it with absorbent cotton or other soft cloth.
6) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
7) Precautions of peeling off the protection film.
   - Be sure to peel off slowly (recommended more than 7sec) and constant speed.
   - Peeling direction shows below Fig.5.
   - Be sure to ground person with adequate methods such as the anti-static wrist band.
   - Be sure to ground S-PWB while peeling of the protection film.
   - Ionized air should be blown over during peeling action.
   - The protection film must not touch drivers and S-PWBs.
   - If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

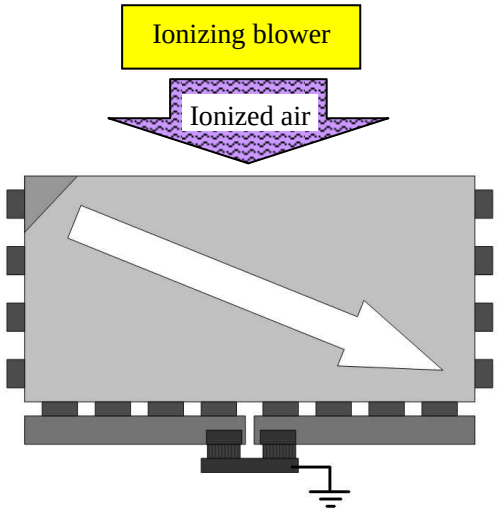
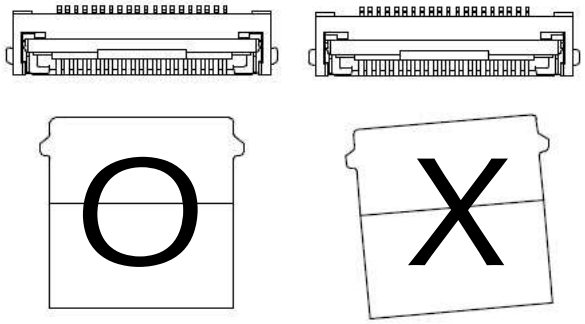


Fig.5 Direction of peeling off a protection film.

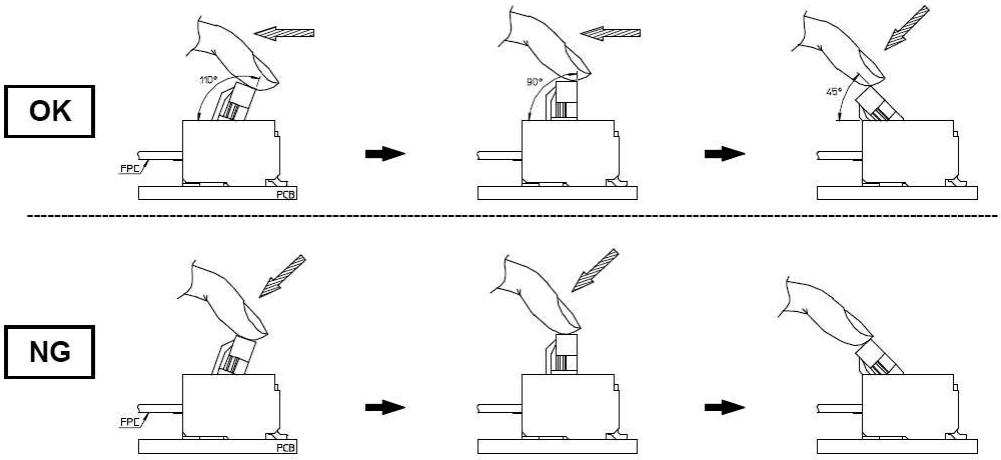
8) Since the Open Cell consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.
   - Reference : Process control standard of SDP

	Item	Management standard value and performance standard
1	Anti-static mat (floor)	1 to 50 [M ohm]
2	Anti-static mat (shelf, desk)	1 to 100 [M ohm]
3	Ionizer	Attenuate from ±1000V to ±100V within 2 sec
4	Anti-static wrist band	0.8 to 10 [M ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000 [ohm]
6	Temperature	22 to 26 [℃]
7	Humidity	60 to 70 [%RH]

9) The Open Cell has some PWBs, take care to prevent them from any stress or pressure when handling or installing the Open Cell, otherwise some of electronic parts on the PWBs may be damaged.
10) Be sure to turn off the power supply when inserting or disconnecting the cable.
11) Be sure to design the module and cabinet so that the Open Cell can be installed without any extra stress such as warp or twist.
12) When handling the Open Cell and assembling them into module and cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open Cell.
13) Applying too much force and stress to PWB and driver may cause a malfunction electrically and mechanically.
14) The Open Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.
15) The chemical compound, which causes the destruction of ozone layer, is not used.
16) Instruction of connector upon usage.
   a) Do with the actuator opened completely , and insert it in the interior of the insertion entrance surely Horizontally When you insert FFC. (Please put the FFC tab in the ditch of the housing surely with the FFC tab.) Might it become short defective, and it cause the corner to transform the caught terminal into the terminal by the pitch gap when inserting it right and left and diagonally.

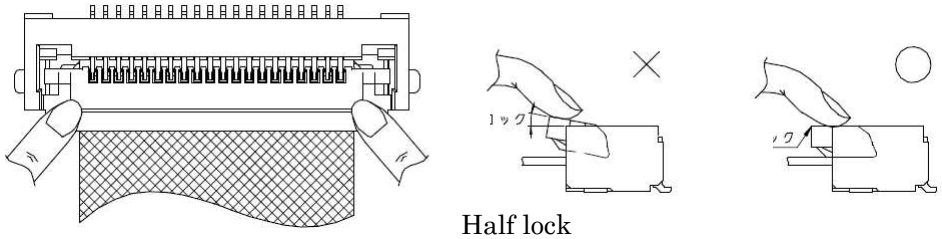


   b) Please add force in the direction where the actuator is held and do by rotating it pushing in parallel to the C-PWB direction when becoming 90°or less as shown in the figure below until the angle of the actuator becomes 90°or less when you shut the actuator. Please do not add the force to rotary axis of actuator in the direction that the actuator is off.



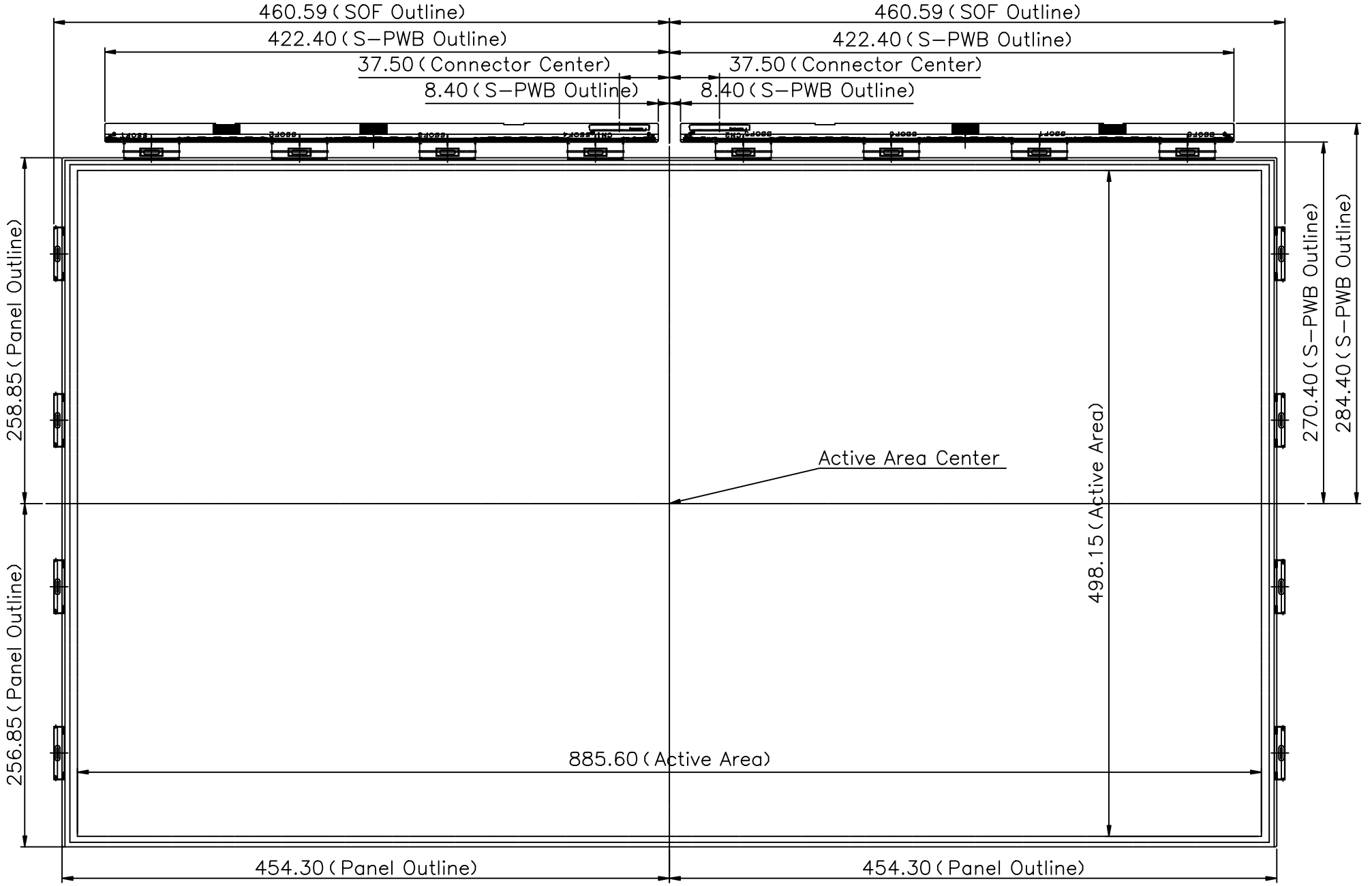
c) About the lock operation

When you lock, it should be push on both sides of the actuator. And it is necessary to confirm that the actuator is surely shut.



Half lock

17) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
18) This Open Cell is corresponded to RoHS. ‘‘R.C.’’ label on the side of palette shows it.
19) When any question or issue occurs, it shall be solved by mutual discussion.


460.59 (SOF Outline)
460.59 (SOF Outline)
422.40 (S−PWB Outline)
422.40 (S−PWB Outline)
37.50 (Connector Center)
37.50 (Connector Center)
8.40 (S−PWB Outline)
8.40 (S−PWB Outline)
258.85 (Panel Outline)
256.85 (Panel Outline)
Active Area Center
498.15 (Active Area)
270.40 (S−PWB Outline)
284.40 (S−PWB Outline)
885.60 (Active Area)
454.30 (Panel Outline)
454.30 (Panel Outline)