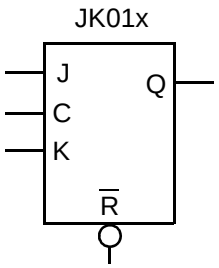
### Description

JK01x is a family of static, master-slave JK flip-flops. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

**Logic Symbol**




**Truth Table**

| RN | J | K | C | Q(n+1) |
|---|---|---|---|---|
| L | X | X | X | L |
| H | L | L | ↑ | NC |
| H | L | H | ↑ | L |
| H | H | L | ↑ | H |
| H | H | H | ↑ | $\overline{Q(n)}$ |

NC = No Change



### HDL Syntax

Verilog ..... JK01x *inst_name* (Q, C, J, K, RN);

VHDL..... *inst_name*: JK01x port map (Q, C, J, K, RN);

### Pin Loading

| Pin Name | Equivalent Loads | |
|---|---|---|
| | JK011 | JK012 |
| J | 1.0 | 1.0 |
| K | 1.0 | 1.0 |
| C | 1.0 | 1.0 |
| RN | 1.0 | 1.0 |

### Size And Power Characteristics

| Cell | Equivalent Gates | Power Characteristics[a] | |
|---|---|---|---|
| | | Static $I_{DD}$ ($T_J$ = 85°C) (nA) | $EQL_{pd}$ (Eq-load) |
| JK011 | 11.0 | TBD | 25.0 |
| JK012 | 12.0 | TBD | 28.3 |

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

## AMI5HG 0.5 micron CMOS Gate Array



### Propagation Delays (ns)

Conditions: $T_J$ = 25°C, $V_{DD}$ = 5.0V, Typical Process

| | Number of Equivalent Loads | | 1 | 2 | 5 | 8 | 10 (max) |
|---|---|---|---|---|---|---|---|
| JK011 | From: C<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.83<br>0.70 | 0.87<br>0.76 | 1.02<br>0.88 | 1.20<br>0.98 | 1.33<br>1.04 |
| | From: RN<br>To: Q | $t_{PHL}$ | 0.31 | 0.35 | 0.45 | 0.53 | 0.59 |
| | **Number of Equivalent Loads** | | **1** | **4** | **8** | **13** | **17 (max)** |
| JK012 | From: C<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.84<br>0.71 | 0.93<br>0.80 | 1.03<br>0.88 | 1.15<br>0.97 | 1.24<br>1.03 |
| | From: RN<br>To: Q | $t_{PHL}$ | 0.31 | 0.37 | 0.44 | 0.52 | 0.58 |

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

### Timing Constraints

Conditions: $T_J$ = 25°C, $V_{DD}$ = 5.0V, Typical Process

| Delay (ns) From | To | Parameter | Cell | |
|---|---|---|---|---|
| | | | JK011 | JK012 |
| Min C Width | High | $t_w$ | 0.84 | 0.84 |
| Min C Width | Low | $t_w$ | 0.75 | 0.75 |
| Min RN Width | Low | $t_w$ | 0.53 | 0.58 |
| Min J Setup | | $t_{su}$ | 0.75 | 0.75 |
| Min J Hold | | $t_h$ | 0.17 | 0.17 |
| Min K Setup | | $t_{su}$ | 0.64 | 0.64 |
| Min K Hold | | $t_h$ | 0.17 | 0.17 |
| Min RN Setup | | $t_{su}$ | 0.36 | 0.40 |
| Min RN Hold | | $t_h$ | 0.33 | 0.33 |

## Logic Schematic