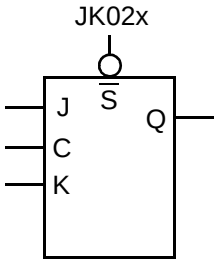
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

JK02x is a family of static, master-slave JK flip-flops. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)
L	X	X	X	H
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK02x *inst_name* (Q, C, J, K, SN);

VHDL..... *inst_name*: JK02x port map (Q, C, J, K, SN);

Pin Loading

Pin Name	Equivalent Loads	
	JK021	JK022
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
SN	2.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK021	11.0	TBD	22.3
JK022	11.0	TBD	24.3

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	5	8	10 (max)
JK021	From: C To: Q	t_{PLH} t_{PHL}	0.75 0.78	0.79 0.85	0.88 1.01	0.98 1.16	1.05 1.25
	From: SN To: Q	t_{PLH}	0.14	0.18	0.28	0.37	0.42
	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
JK022	From: C To: Q	t_{PLH} t_{PHL}	0.76 0.80	0.81 0.91	0.87 1.02	0.96 1.15	1.02 1.24
	From: SN To: Q	t_{PLH}	0.10	0.15	0.22	0.28	0.33

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Core Logic

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK021	JK022
Min C Width	High	t_w	0.77	0.80
Min C Width	Low	t_w	0.79	0.80
Min SN Width	Low	t_w	0.69	0.65
Min J Setup		t_{su}	0.79	0.80
Min J Hold		t_h	0.17	0.17
Min K Setup		t_{su}	0.70	0.71
Min K Hold		t_h	0.17	0.17
Min SN Setup		t_{su}	0.21	0.21
Min SN Hold		t_h	0.49	0.48

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Logic Schematic