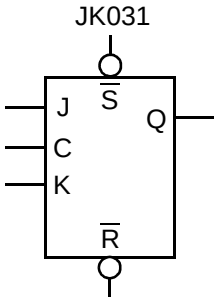
Description

JK031 is a static, master-slave JK flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)
L	L	X	X	X	IL
L	H	X	X	X	L
H	L	X	X	X	H
H	H	L	L	↑	NC
H	H	L	H	↑	L
H	H	H	L	↑	H
H	H	H	H	↑	$\overline{Q(n)}$

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	1.0
SN	2.1
RN	2.2

Core Logic

Equivalent Gates 12.0

HDL Syntax

Verilog ..... JK031 *inst_name* (Q, C, J, K, RN, SN);

VHDL..... *inst_name*: JK031 port map (Q, C, J, K, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	26.2	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.76 0.80	0.80 0.87	0.90 1.04	0.99 1.18	1.05 1.26
RN	Q	t_{PHL}	0.94	0.99	1.15	1.33	1.45
SN	Q	t_{PLH}	0.14	0.17	0.27	0.36	0.42

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.79
Min C Width	Low	t_w	0.80
Min RN Width	Low	t_w	0.96
Min SN Width	Low	t_w	0.84
Min J Setup		t_{su}	0.80
Min J Hold		t_h	0.17
Min K Setup		t_{su}	0.72
Min K Hold		t_h	0.17
Min RN Setup		t_{su}	0.36
Min RN Hold		t_h	0.33
Min SN Setup		t_{su}	0.22
Min SN Hold		t_h	0.49

Logic Schematic