



PROMATE ELECTRONIC CO., LTD.

Product Specification

Model No.: JLPA070VW01-2
 7.0" TFT-LCD Module

Description: with Touch Panel

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R&D	Robert	8/30/04	Gilbert 8/30	Ray Aug. /30th/ 2004
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Production	Ray	7/1/04	<input checked="" type="checkbox"/> Production	<input type="checkbox"/> Production



Promate Electronic Co., Ltd

4F, 32, Sec. 1, Huan Shan RD., Nei Hu, 104, Taipei, R.O.C
 Tel: 886-2-2659-0303 FAX: 886-2-2658-0988

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1. Physical specifications

No.	Item	Specification	Remark
1	Display resolution (pixel)	800(w) x 480(H)	
2	Active area (mm)	152.4(W) x 91.44(H)	
3	Screen size (inch)	7.0(Diagonal)	
4	Pixel pitch (mm)	0.1905(W) x 0.1905(H)	
5	Color configuration	R.G.B. stripe	
6	Overall dimension (mm)	165(W)x104(H)x7.4(D)	Note 1
7	Weight (g)	185±10	
8	Surface treatment	AG(5.5%) with WV film	
9	Backlight unit	CCFL	

Note 1: Refer to Fig. 1



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2. Electrical specifications

2.1 Absolute maximum ratings

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	Vcc	-0.5		5	V
	AVDD	-0.5		12	V
	VGH	-0.3		18	V
	VGL	-15		0.3	V
	VGH-VGL			33	V
Input Signal Voltage	Vi	-0.3		Vcc+0.3	V
	Vref(V1~V5)	0.4AVDD		AVDD+0.3	V
	Vref(V6~V10)	-0.3		0.6AVDD	V
	Vcom		2.6		V
Operation Temperature	Topa	-5		60	□
Storage Temperature	Tstg	-30		70	□

2.2 Typical operating conditions (GND=AVss=0V)

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	Vcc	3.0	3.3	3.6	V
	AVDD	7.8	8.4	9.2	V
	VGH	14.0	15.0	16.0	V
	VCOM		2.6		V
	VGL	-11.0	-10	-9.0	V
Input Reference Voltage	V1~V5	0.4AVDD	-	AVDD-0.2	V
	V6~V10	0.2	-	0.6AVDD	V
Input H/L Level Voltage	VIH	0.8VCC	-	VCC	V
	VIL	0	-	0.2VCC	V

2.3 Current consumption conditions (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current For Driver	IGH	VGH=15V	-	100	150	uA
	IGL	VGL=-10V	-	-100	-150	uA
	ICC	VCC=5V	-	3.5	5	mA
	IDD	AVDD=5V	-	20	30	mA



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2.4 Backlight driving conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage	VL			(580)	(640)	Vrms
Current	IL			6	7	mA
Frequency	FL			60	80	KHz
Lamp Start Voltage	Vs	T=25□			850	Vrms
		T=0□			1150	Vrms
		T=-30□			1300	Vrms

2.5 Timing conditions

AC Electrical Characteristics (VCC=3.3V, AVDD=8.4V, AVSS=GND=0V, TA=25□)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK frequency	Fclk		40	42	MHz
CLK pulse width	TCW	6			ns
Data set-up time	Tsu	4			ns
Data hold time	Thd	2			ns
Propagation delay of DIO2/1	Tphl	6			ns
Time that the last data to LD	Tld	1			Tcw
Pulse width of LD	Twld	2			Tcw
Time that LD to DIO1/2	Tlds	5			Tcw
POL set-up time	Tpsu	6			ns
POL hold time	Tphd	6			ns
OEV pulse width	TOEV		12		Tcw
CKV pulse width	TCKV	16	28	40	Tcw
Horizontal display start	TSH		0		Tcw/3
Horizontal display timing range	TDH		800		Tcw/3
STV setup time	TSUV	400			ns
STV hold time	THDV	400			ns
STV pulse width	TSTV			1	TDH
Horizontal lines per field	TV	512	525	610	TDH
Vertical display start	TSV		3		TDH
Vertical display timing range	TDV		480		TDH

DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	2.7	3.3	3.6	V
Low Level Input Voltage	Vil	0	-	0.3*Vcc	V
High Level Input Voltage	Vih	0.7*Vcc	-	Vcc	V
High Level Output Voltage	Voh	Vcc-0.4	-	-	V
Low Level Output Voltage	Vol	GND	-	GND+0.4	V
Supply Voltage	AVDD	6.5	8.4	10	V
Sinking Current of Outputs	IOL	-80	-	-	uA
Driving Current of Outputs	IOH	80	-	-	uA



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2.6 Pin assignment

FPC I/O pin assignment, FH12-50S-0.5SH(Hirose)

Pin no.	Symbol	I/O	Description	Remark
1	GND	P	Ground for gate drive	
2	VCC	P	Digital voltage for gate driver	
3	VGL	P	TFT low voltage	
4	VGH	P	TFT high voltage	
5	STVL	I/O	Start pulse signal input/output (vertical)	
6	STVR	I/O	Start pulse signal input/output (vertical)	
7	CKV	I	CLK (vertical)	
8	U/D	I	Up or Down display	
9	OEV	I	Output enable	
10	VCOM	I	VCOM voltage	
11	DIO1	I/O	Start pulse signal input/output (horizontal)	
12	AVDD	P	Analog voltage for source driver	
13	AVSS	P	Analog ground for source driver	
14	GND	P	Digital ground for source driver	
15	VCC(DVDD)	P	Digital voltage for source driver	
16	EDGSL	I	Select raising edge or raising/falling edge	
17	CLK	I	Sample CLK	
18	SHL(R/L)	I	Right or Left display control	
19	R0	I	Red data	
20	R1	I	Red data	
21	R2	I	Red data	
22	R3	I	Red data	
23	R4	I	Red data	
24	R5	I	Red data	
25	G0	I	Green data	
26	G1	I	Green data	
27	G2	I	Green data	
28	G3	I	Green data	
29	G4	I	Green data	
30	G5	I	Green data	
31	V1	I	Reference voltage	
32	V2	I	Reference voltage	
33	V3	I	Reference voltage	
34	V4	I	Reference voltage	
35	V5	I	Reference voltage	
36	V6	I	Reference voltage	
37	V7	I	Reference voltage	
38	V8	I	Reference voltage	
39	V9	I	Reference voltage	
40	V10	I	Reference voltage	
41	B0	I	Blue data	
42	B1	I	Blue data	
43	B2	I	Blue data	
44	B3	I	Blue data	
45	B4	I	Blue data	
46	B5	I	Blue data	
47	LD(OEH)	I	Latch and switch data to output	
48	REV	I	Control data are inverted or not	
49	POL	I	Polarity selection	
50	DIO2	I/O	Start pulse signal input/output (horizontal)	



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3. Optical specification (Note 1, Note 2)

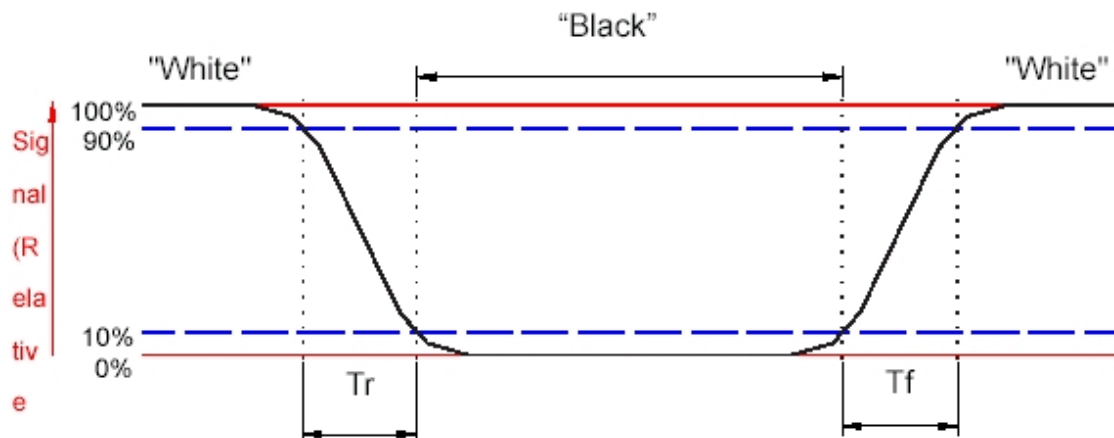
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	$\theta=0^\circ$	-	12	50	ms	Note 3, 5
	Fall		-	18	60	ms	
Contrast ratio	CR	At optimized viewing angle	200	300	-		Note 4, 5
Viewing angle	Top	$CR \geq 10$	30	40	-	deg	Note 5, 6
	Bottom		50	60	-		
	Left		50	60	-		
	Right		50	60	-		
Viewing angle	Top	$CR \geq 5$	40	50	-	deg	Note 5, 6
	Bottom		60	70	-		
	Left		60	70	-		
	Right		60	70	-		
Brightness	Y_L	$I_L=6mA, 25^\circ C$	280	320	-	nit	Note 7
White chromaticity	X	$\theta=0^\circ$	0.26	0.31	0.36		Note 7
	Y	$\theta=0^\circ$	0.28	0.33	0.38		

Note 1: Ambient temperature $T_a=25^\circ C$, and lamp current $I_L=6 mA$. To be measured in the dark room.

Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.





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Note 4: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5:

White $V_i = V_{i50} + 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

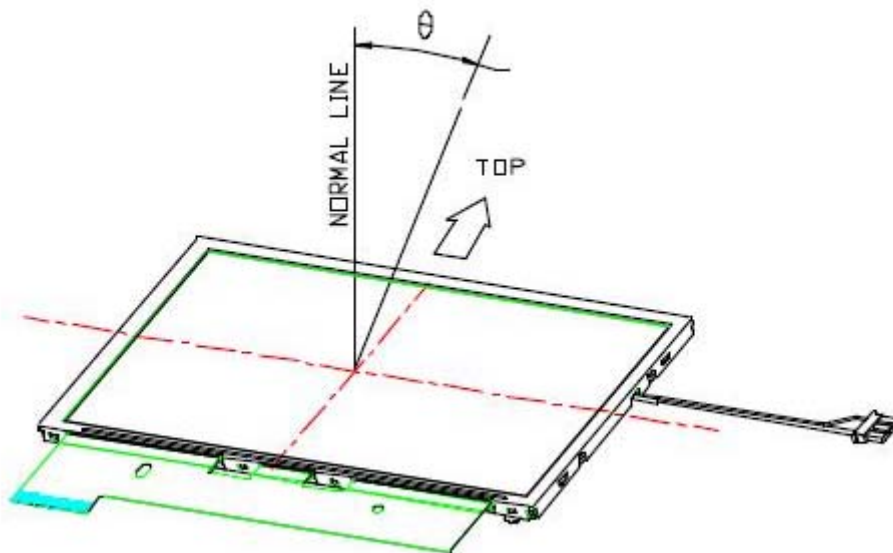
“+/-” means that the analog input signal swings in phase with V_{COM} signal

“-/+” means that the analog input signal swings out phase with V_{COM} signal

V_{i50} The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened

Note 6: Definition of viewing angle, refer to figure as below.



Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



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4. Touch panel specification

- Operating condition

Item	Min.	Typ.	Max.	Unit	Remark
Operating voltage	-	-	7	V _{DC}	

- Electrical characteristic

Item		Min.	Typ.	Max.	Unit	Remark
Resistance between terminal	XH-XL	120	-	600		
	YH-YL	400	-	1100		
Insulation resistance	X-Y	10	-	-	M	
Linearity	X	-	-	1.5	%	
	Y	-	-	1.5	%	

- Mechanical characteristic

Item	Min.	Typ.	Max.	Unit	Remark
Pen/Finger input pressure	-	-	80	g	
Surface hardness	-	3		H	

- Optical characteristic

Item	Min.	Typ.	Max.	Unit	Remark
Transparency	-	82.5	-	%	
HAZE	-	5.0		%	



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5. Reliability test items (Note 2)

No.	Test Items	Conditions	Remark
1	High temperature storage	Ta=70°C, 8 hrs	
2	Low temperature storage	Ta=-30°C, 8 hrs	
3	High temperature operation	Tp=60°C, 8 hrs	
4	Low temperature operation	Ta=-5°C, 8 hrs	
5	High temperature and high humidity	Tp=40°C, 90%, 8 hrs	Operation

Note 1: Ta: Ambient temperature

Note 2: Tp: Panel surface temperature

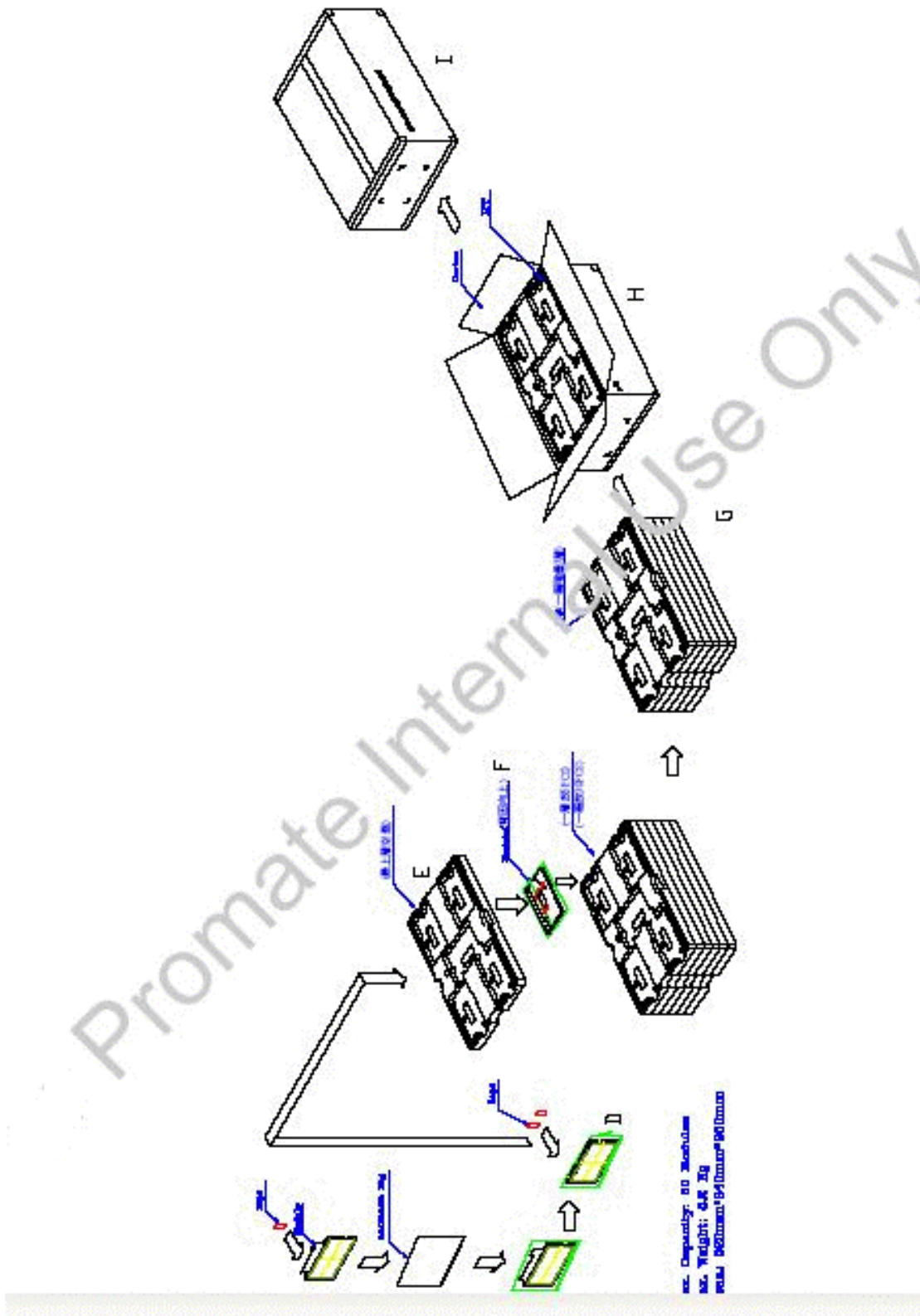
Note 3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.



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6. Packing form





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7. Appendix

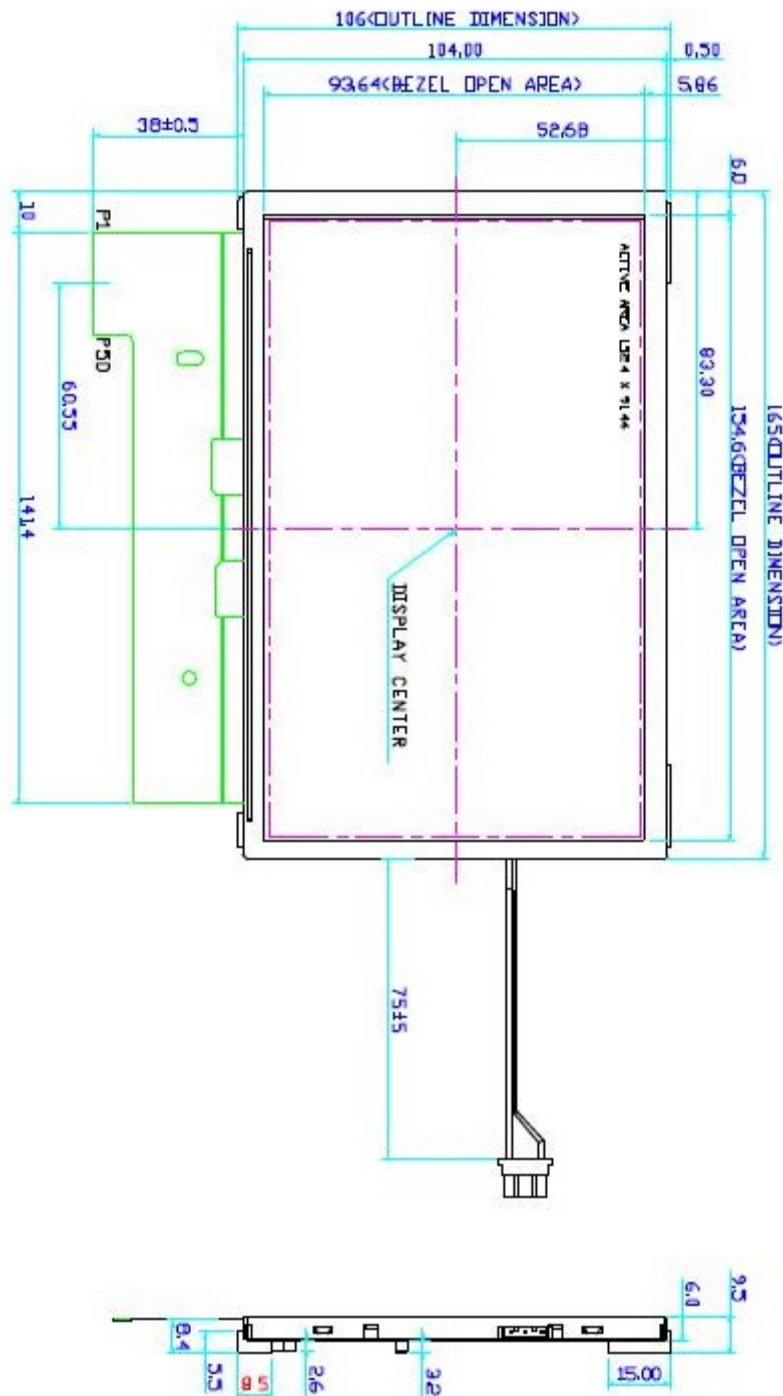


Fig.1 Outline dimension of TFT-LCD panel (Front side)



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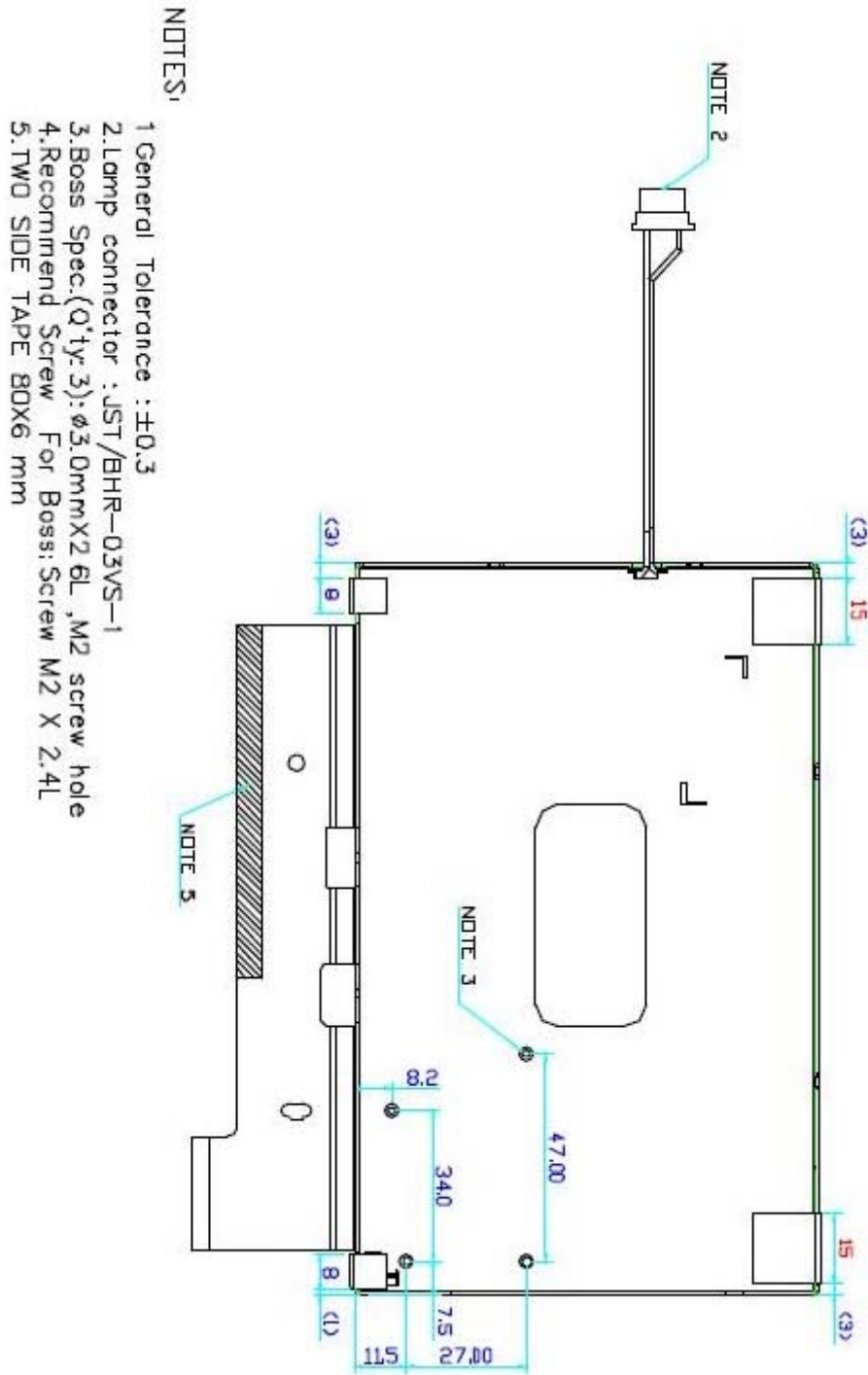


Fig.2 Outline dimension of TFT-LCD panel (Rear side)



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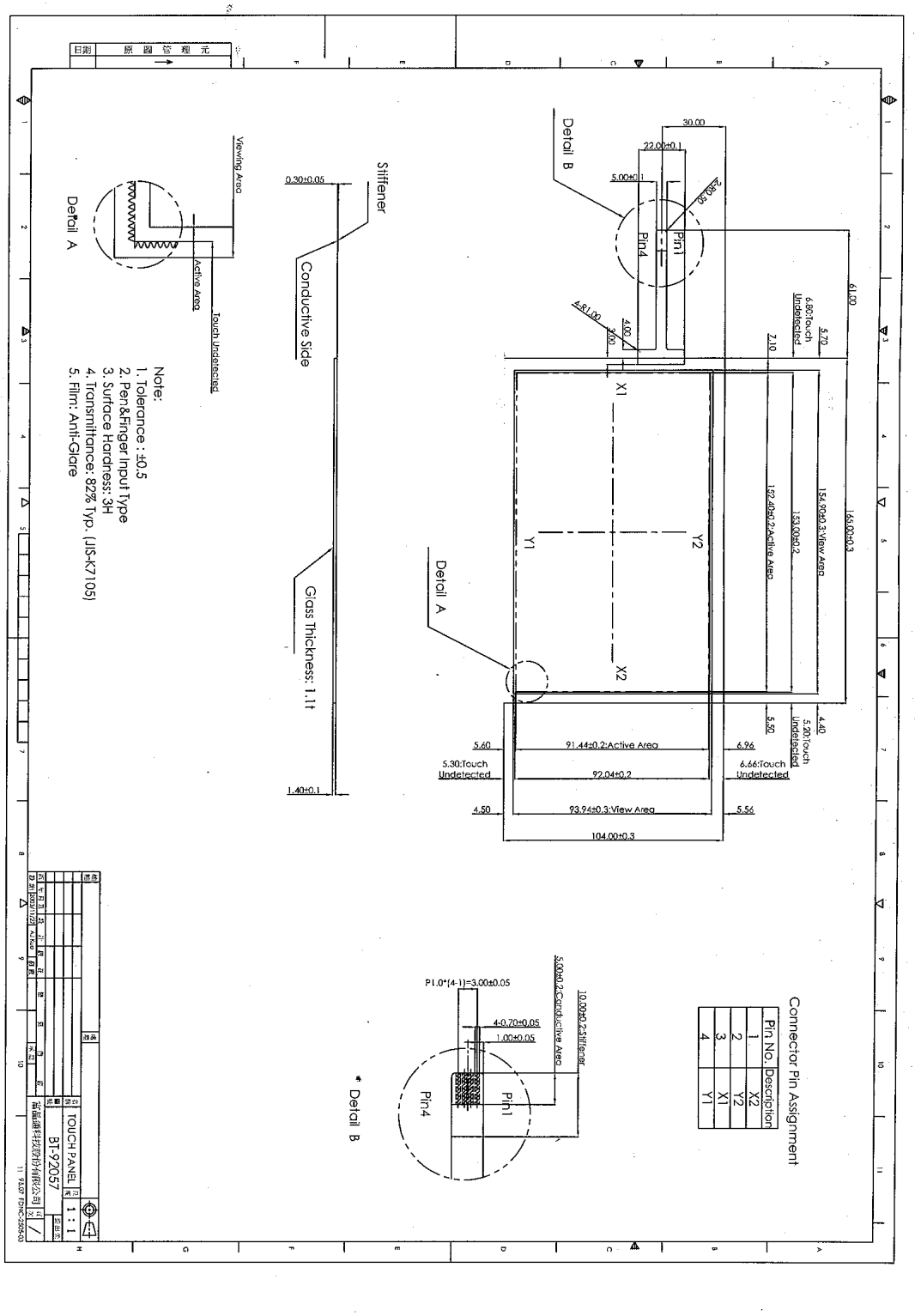


Fig.3 Outline dimension of touch panel



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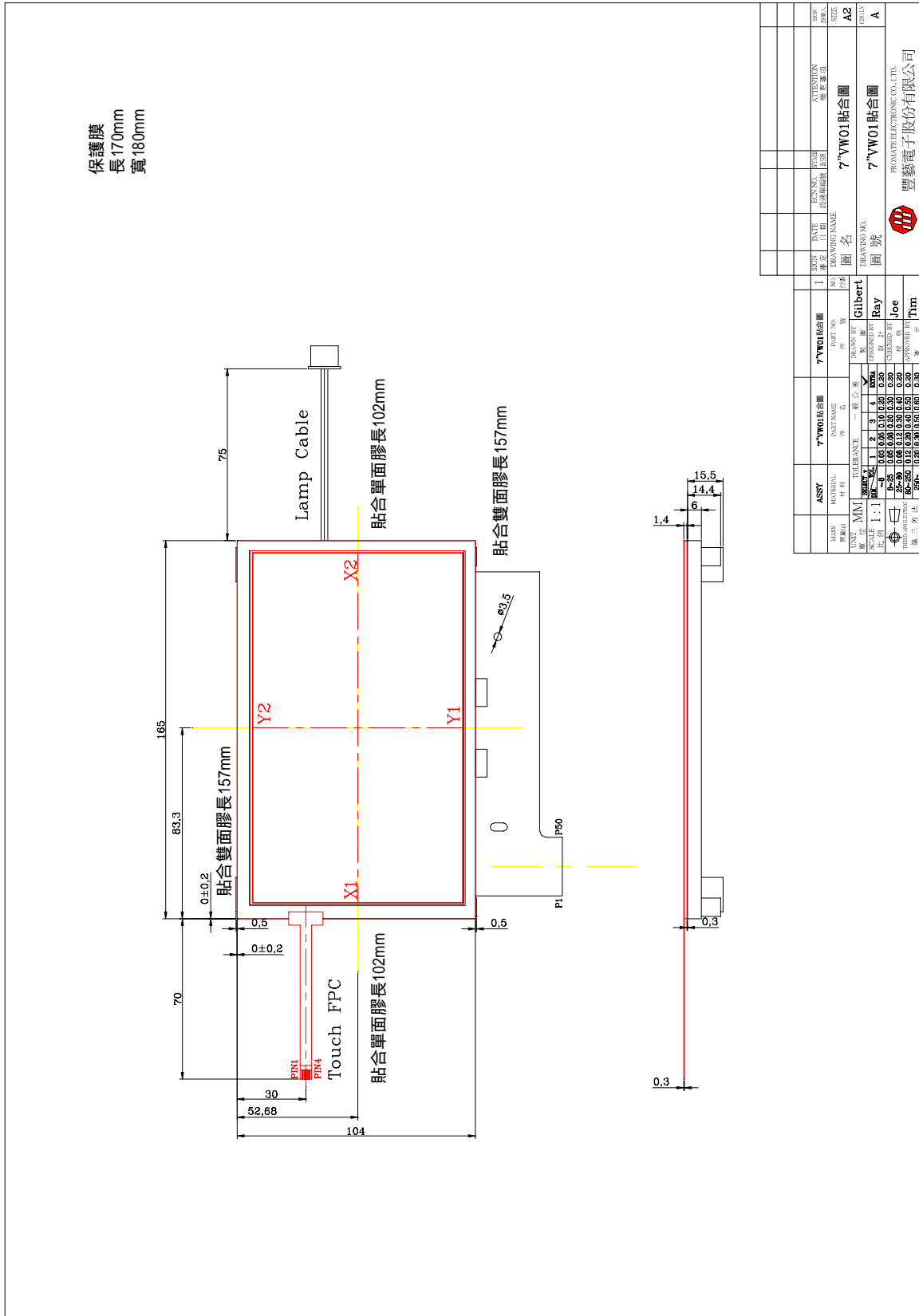


Fig. 4 Touch panel assembly drawing



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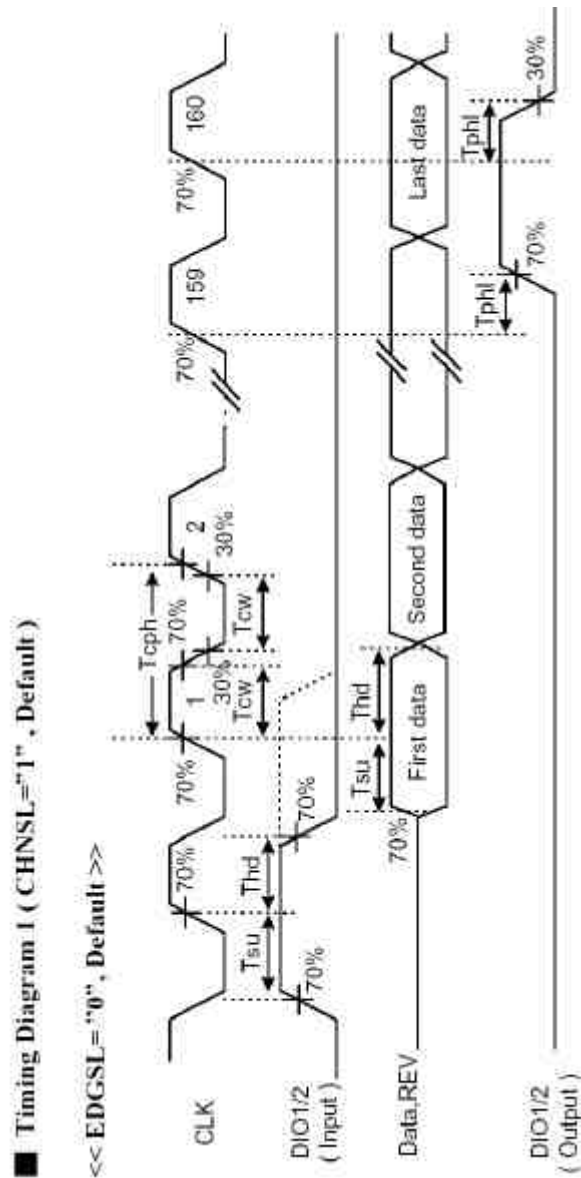


Fig.5 Operation mode 1



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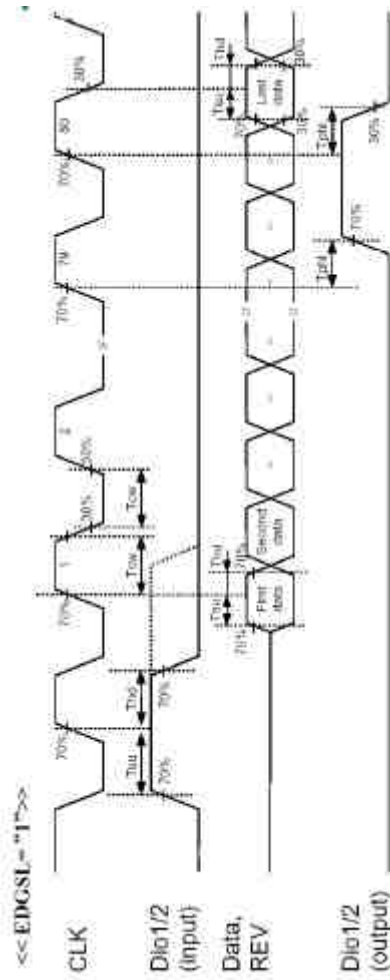


Fig.6 Operation mode 2



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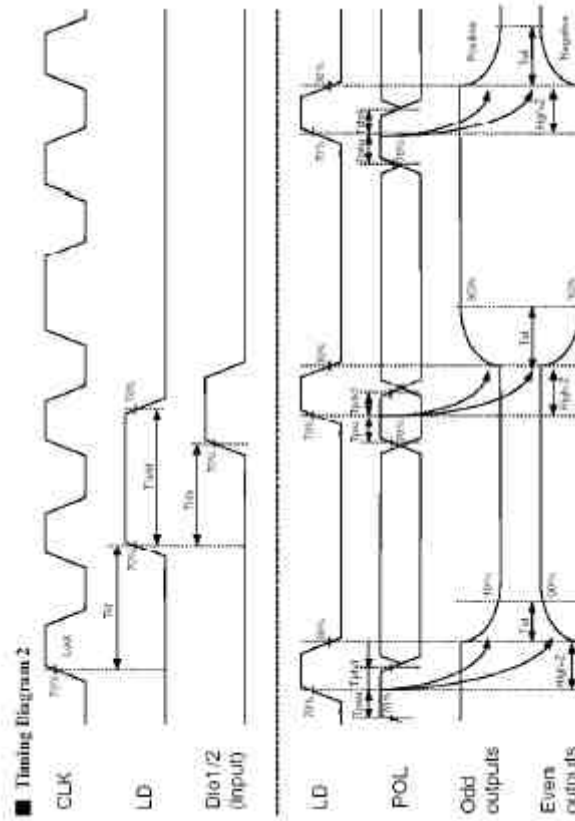


Fig.7 Horizontal timing



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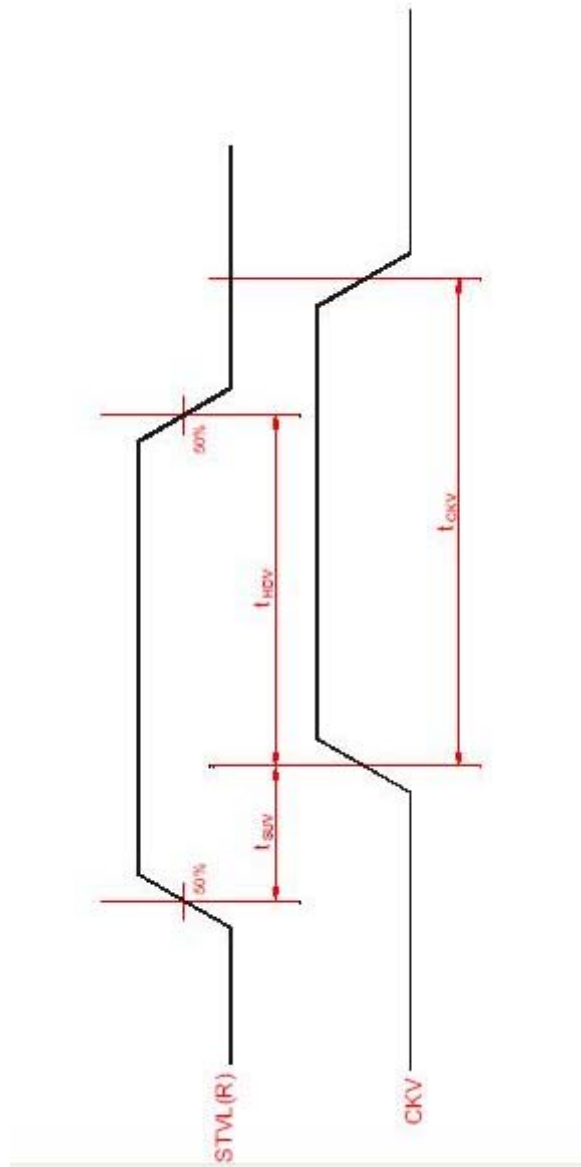


Fig.8 Vertical shift clock timing



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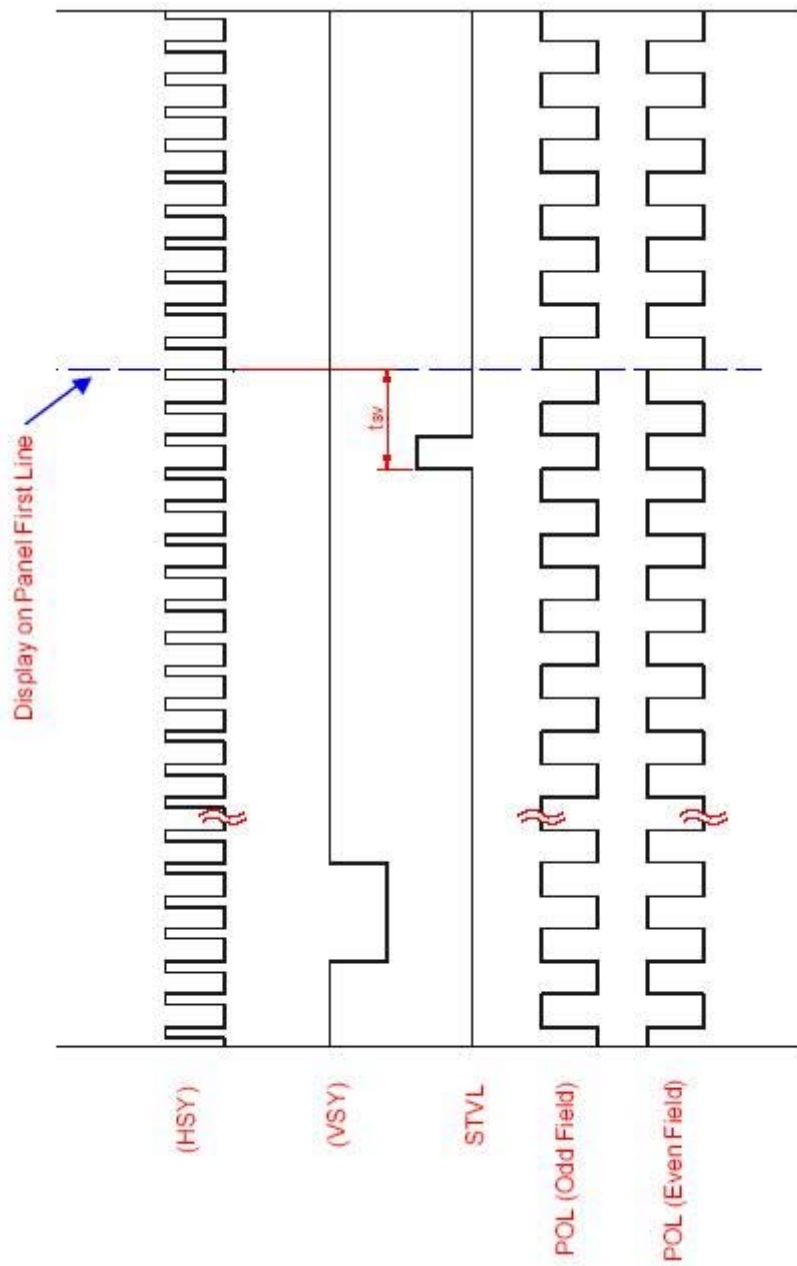


Fig.9 Vertical timing (from up to down)