JM20330
Serial ATA Bridge Chip

Datasheet

Rev. 3.0

Revision History

Version	Date	Author	Revision Description
Preliminary	2004-08-05		Initial B version
Preliminary 1	2004-08-27		Provide internal weak pull-low (Typical 31 KΩ) & internal weak pull-high (Typical 31 KΩ).
2.0	2005-01-20		1.Support Multiple-Word DMA. 2.Modify the description of signals HSTROBE and DSTROBE. 3.Modify the 6-10 Ultra DMA Transfer Rate to only support 150Mhz operation. 4.Extend the ACTL from 20 bits to 40 bits.
2.1	2005-03-10		Modify Absolute Maximum Ratings voltage and current.
2.2	2006-01-11		1.Add description of crystal Oscillator in page 14 2.Add industry spec. description in section 8.3
2.3	2006-07-20		1.Add power on sequence. 2.Modify Absolute Maximum Ratings voltage and current. 3.Change the minimum commercial ambient operation temperature from –10 to 0. 4.Revised REXT 12KΩ 1% 5.Add 6.11 section for device mode master-only operation.
2.4	2006-10-30		1.Add the leakage current information. 2.Rise/Fall time meets Gen2 Spec. 3.Add description about MODE[2:0] pin 4.Modify the storage temperature. 5.Remove the min absolute Junction temperature. 6.Remove the Junction temperature information. 7.Modify 8.1 Power Requirements parameter 8.Add 8.7 Partial Power Consumption parameter. 9.Add 8.8 Slumber Power Consumption parameter.
2.5	2007-06-01		Modify REXT resistor for both 12KΩ 1% and 12.1 KΩ 1%
3.0	2008/03/31		1.Support SSC. 2.Remove the Vender Specific Command. 3.Remove the UART Interface Operation. 4.Remove the Partial Power Consumption. 5.Remove the Power-on Reset Sequence. 6.Add 2.2 Host Bridge figure. 7.Add 2.3 Device Bridge figure. 8.Modify 4.1 Package-Dimensions. 9.Modify 5.3 Parallel ATA Interface DASPn and SP. 10.Modify 5.5 Configuration Interface descriptions. 11.Add 6.9 Ultra DMA Transfer Rate descriptions. 12.Add 7.0 Power Management descriptions. 13.Modify 8.2 Absolute Maximum Ratings parameter.

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1. General Description

The Serial ATA Bridge is a single chip solution for serial and parallel ATA translation. It includes the Serial ATA PHY, Link, Transport, and parallel ATA (application layer) controller. The main applications are for legacy IDE storage devices connecting to newer chipset supporting serial ATA, such as the iCH5 south bridge of Intel chipset, and serial ATA IDE storage devices connecting to traditional IDE south bridge.

The Serial ATA physical, link, and transport layer are compliance to Serial ATA Generation 1, which supports a 1.5Gbps data rate. The application layer supports both the ATA register command set and PACKET command set, which could drive both the Hard Disk Drive and ATAPI Optical Storage such as CR-ROM, CD-RW, DVD-ROM, DVD-RW, etc. The serial ATA and application layer support both device and host operation and could be configured by a simple HOST/DEVICE pin.

This chip is designed by 0.18um CMOS technology and 64-pin TQFP or QFN package.

2. Features

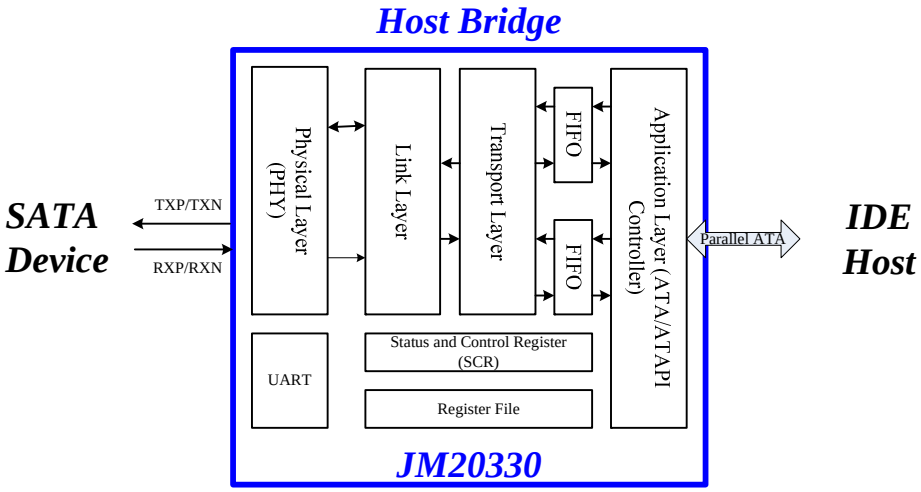
2.1 General

- **0.18um CMOS technology.**
- **Compliance with Gen1i/Gen1m of Serial ATA II Electrical Specification 2.5**
- **Spread-Spectrum Clock (SSC) technology.**
- **1.8V and 3.3V power system.**
- **25MHz external reference clock.**
- **64-pin TQFP and QFN packages.**
- **Support ATA/ATAPI-7 specification**

2.2 Host Bridge

- **ATA/ATAPI PIO Mode 0, 1, 2, 3, 4.**
- **ATA/ATAPI Multi-Word DMA Mode 0, 1, 2.**
- **ATA/ATAPI Ultra DMA Mode 0, 1, 2, 3, 4, 5, 6, 7.**
- **ATA/ATAPI master/slave emulation.**
- **ATA/ATAPI PACKET command feature set.**
- **ATA/ATAPI LBA48 addressing mode associated with 2-byte sector count.**
- **Serial ATA power saving modes.**
- **Serial ATA hot-plug.**
- **SATA II Asynchronous Signal Recovery support.**

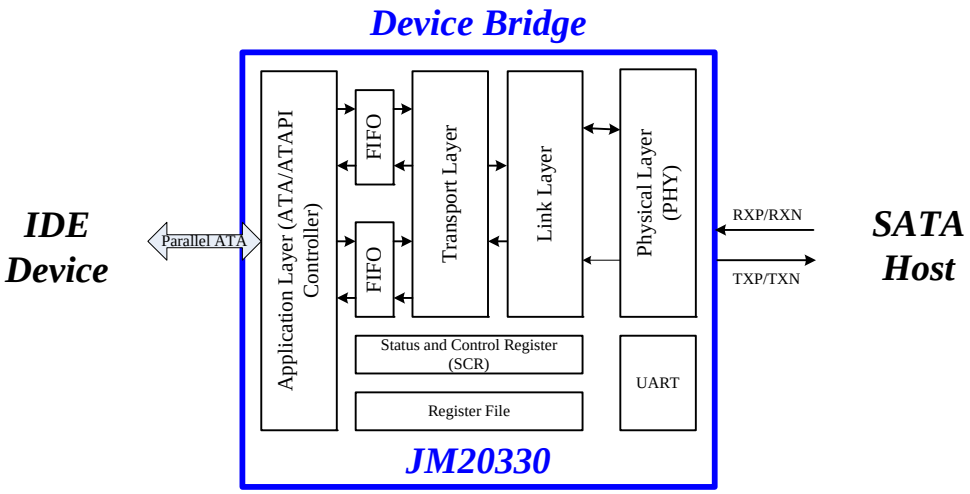
Host bridge mode, the bridge becomes the SATA Host Bus Adaptor. On one side the bridge is connected to the IDE host and to the other side with a SATA device.



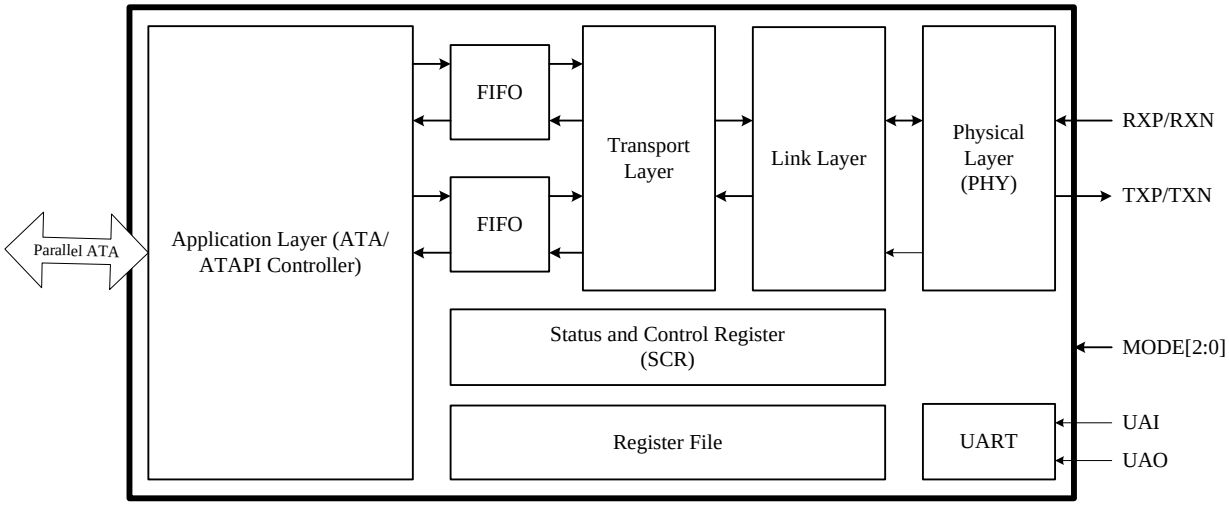
2.3 Device Bridge

- **ATA/ATAPI PIO Mode 0, 1, 2, 3, 4.**
- **ATA/ATAPI Multi-Word DMA Mode 0, 1, 2.**
- **ATA/ATAPI Ultra DMA Mode 0, 1, 2, 3, 4, 5, 6, 7.**
- **ATA/ATAPI PACKET command feature set.**
- **ATA/ATAPI LBA48 addressing mode associated with 2-byte sector count.**
- **Serial ATA power saving modes.**
- **Serial ATA hot-plug.**
- **SATA II Asynchronous Signal Recovery support.**

Device bridge mode, the bridge becomes the SATA device. On one side the bridge is connected to the IDE device and to the other side with a SATA host.



3. Block Diagram



3.1 Physical Layer

The physical layer provides serialization/de-serialization transformation between serial data bus and link layer. It also includes an OOB block to detect COMRESET/COMINIT and COMWAKE for serial bus power on initialization and hot-plug.

3.2 Link Layer

The link layer performs frame envelope encoding and decoding. It receives the frame instruction from transport layer, and generates the necessary primitive for serial link flow control. While receiving data, it detects the primitive and performs the front-end operation to extract the useful frame data for transport layer. It also generates CRC for serial link error handling, and provides 8b/10b data scramble for data transfer.

3.3 Transport Layer

The transfer layer performs frame information structure assembly and decomposition. It also includes FIFO to adjust the speed mismatch between application layer and serial link.

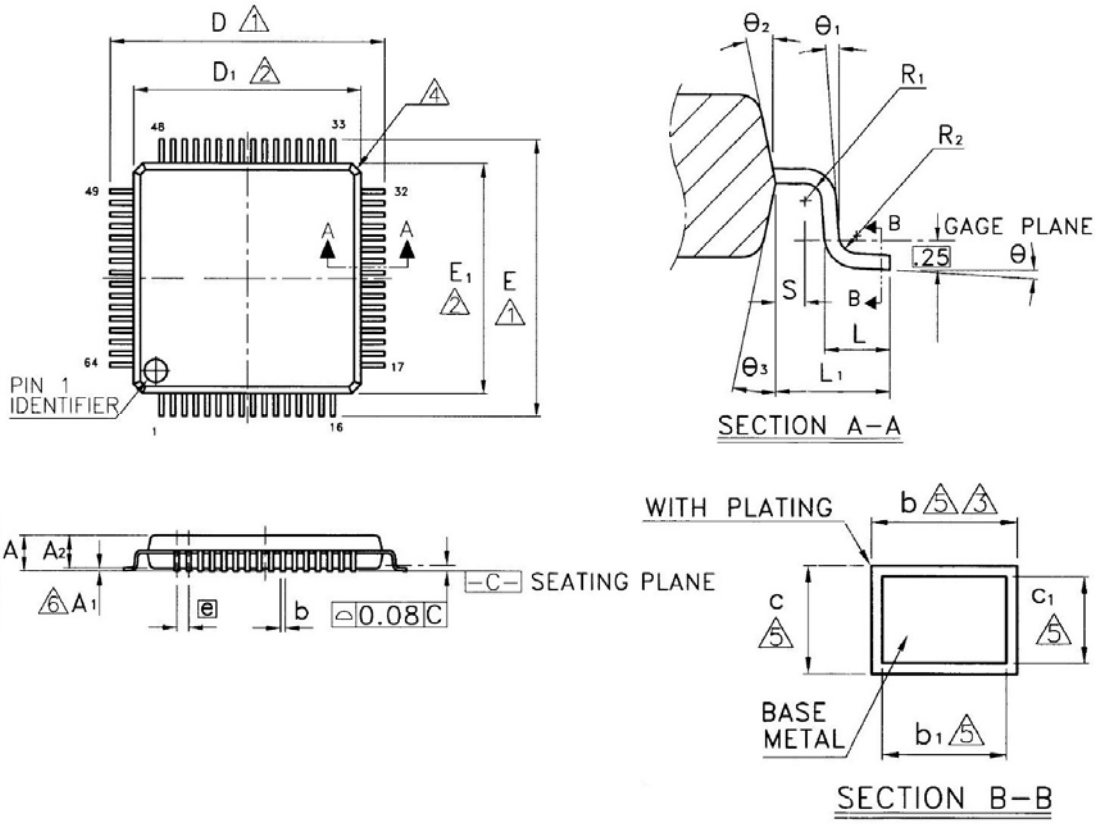
3.4 Application Layer

The application layer is essentially an ATA/ATAPI protocol engine, which complies with ATA/ATAPI-7. It performs the protocol and timing control for parallel ATA and ATAPI command set.

4. Package

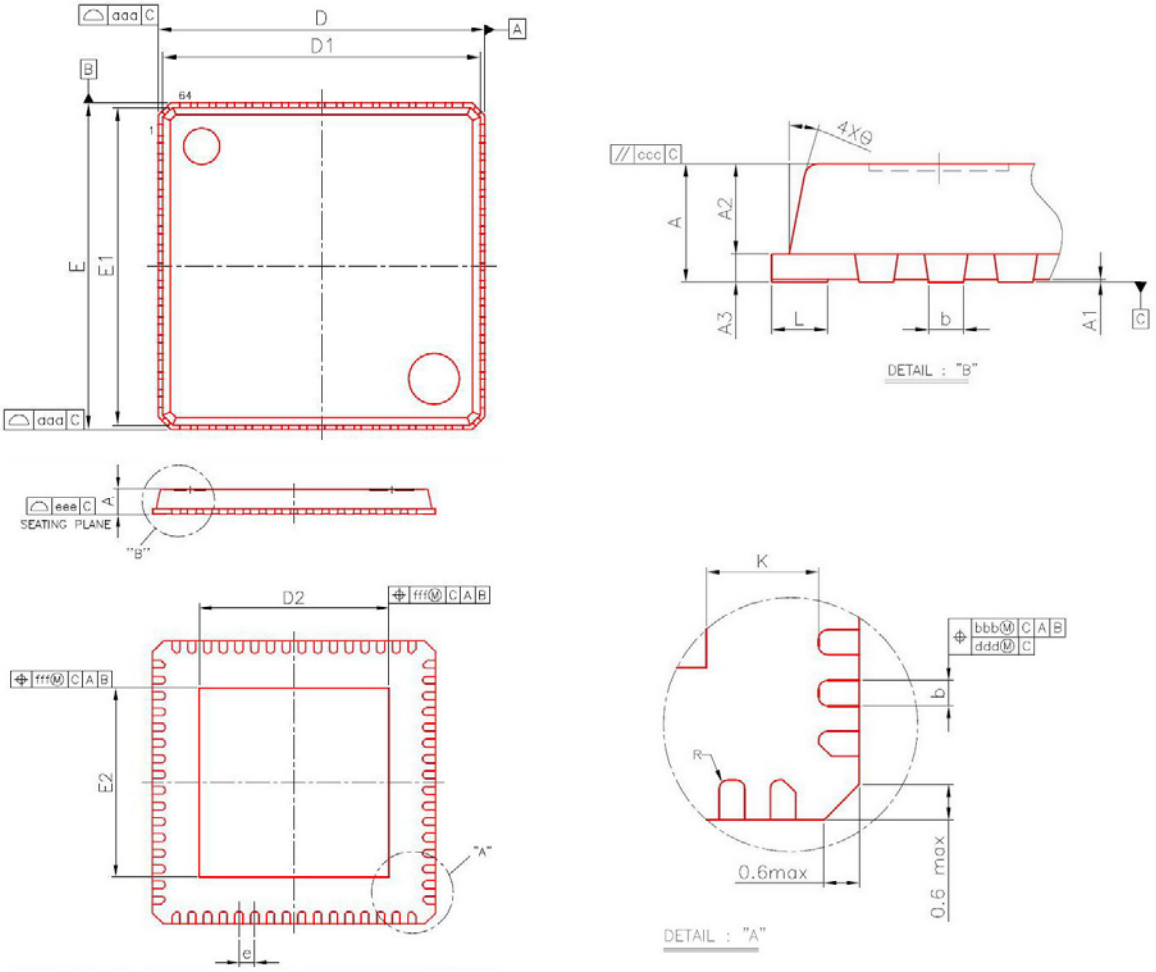
4.1 Package Dimensions

4.1.1 TQFP 64



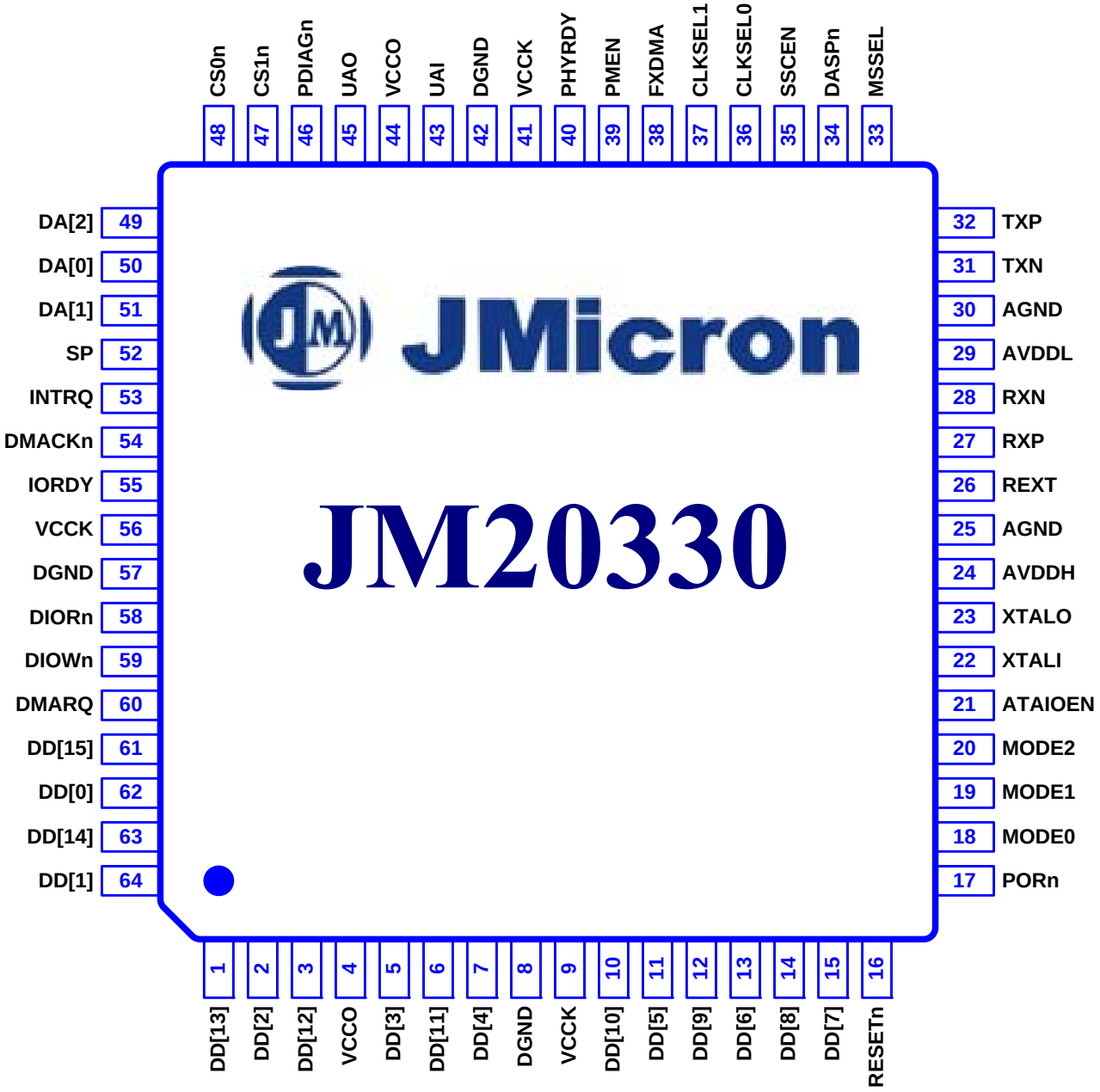
Symbol	Dimension in			Dimension in			Symbol	Dimension in			Dimension in		
	Min	Nom	Max	Min	Nom	Max		Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047	E	12.00 BSC			0.472 BSC		
A1	0.05	---	0.15	0.002	---	0.006	E1	10.00 BSC			0.394 BSC		
A2	0.95	1.00	1.05	0.037	0.039	0.041	e	0.50 BSC			0.020 BSC		
b	0.17	0.22	0.27	0.007	0.009	0.011	L	0.45	0.60	0.75	0.018	0.024	0.030
b1	0.17	0.20	0.23	0.007	0.008	0.009	L1	1.00 REF			0.039 REF		
c	0.09	---	0.20	0.004	---	0.008	θ	0o	3.5o	7o	0o	3.5o	7o
c1	0.09	---	0.16	0.004	---	0.006	θ1	0o	---	---	0o	---	---
D	12.00 BSC			0.472 BSC			θ2	12o TYP			12o TYP		
D1	10.00 BSC			0.394 BSC			θ3	12o TYP			12o TYP		
R1	0.08	----	----	0.003	----	----	S	0.20	----	----	0.008	----	----
R2	0.08	----	0.2	0.003	----	0.008							

4.1.2 QFN 64



Symbol	Dimension in			Dimension in			Symbol	Dimension in			Dimension in		
	Min	Nom	Max	Min	Nom	Max		Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035	Θ	0o	----	14o	0o	----	14o
A1	0.00	0.02	0.05	0.000	0.001	0.002	R	0.09	----	----	0.004	----	----
A2	0.60	0.65	0.70	0.024	0.026	0.028	K	0.20	----	----	0.008	----	----
A3	0.20 REF			0.008 REF			aaa	----	----	0.15	----	----	0.006
b	0.18	0.25	bbb	0.007	0.010	0.012	bbb	----	----	0.10	----	----	0.004
D/E	9.00 BSC			0.354 BSC			ccc	----	----	0.10	----	----	0.004
D1/E1	8.75 BSC			0.344 BSC			ddd	----	----	0.05	----	----	0.002
e	0.50 BSC			0.020 BSC			eee	----	----	0.08	----	----	0.003
L	0.30	0.40	0.50	0.012	----	0.020	fff	----	----	0.10	----	----	0.004

4.2 Package Pin-Out



4.3 Pin List Table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	DD13	17	PORn	33	MSSEL	49	DA2
2	DD2	18	MODE0	34	DASPn	50	DA0
3	DD12	19	MODE1	35	SSCEN	51	DA1
4	VCCO	20	MODE2	36	CLKSEL0	52	SP
5	DD3	21	ATAIOEN	37	CLKSEL1	53	INTRQ
6	DD11	22	XTALI	38	FXDMA	54	DMACKn
7	DD4	23	XTALO	39	PMEN	55	IORDY
8	DGND	24	AVDDH	40	PHYRDY	56	VCCK
9	VCCK	25	AGND	41	VCCK	57	DGND
10	DD10	26	REXT	42	DGND	58	DIORn
11	DD5	27	RXP	43	UAI	59	DIOWn
12	DD9	28	RXN	44	VCCO	60	DMARQ
13	DD6	29	AVDDL	45	UAO	61	DD15
14	DD8	30	AGND	46	PDIAGn	62	DD0
15	DD7	31	TXN	47	CS1n	63	DD14
16	RESETn	32	TXP	48	CS0n	64	DD1

5. Pin Description

5.1 Pin Type Definition

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
L	Internal weak pull-low (Typical 31 KΩ)
H	Internal weak pull-high (Typical 31 KΩ)

5.2 Crystal Interface

Signal Name	Pin Number	Type	Description
XTALI	22	AI	Crystal Input/Oscillator Input. It is connected to a 25MHz crystal or crystal oscillator, frequency tolerance ±50ppm.
XTALO	23	AO	Crystal Output. It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved as No Connection (NC).

5.3 Serial ATA Interface

Signal Name	Pin Number	Type	Description
REXT	26	AI	External Reference Resistance. An external 12KΩ1% (12.1 KΩ 1%) resistor should be connected and bypass to the analog ground. (Note 1)
RXP	27	AI	Serial Data Receiver. It receives positive input of differential signal.
RXN	28	AI	Serial Data Receiver. It receives negative input of differential signal.
TXP	32	AO	Serial Data Transmitter. It transmits positive output of differential signal.
TXN	31	AO	Serial Data Transmitter. It transmits negative output of differential signal.

Note 1: In some area customer may find 12KΩ 1% resistor is hard to buy, in this case 12.1 KΩ 1% resistor can be an alternative option.

5.4 Parallel ATA Interface

Signal Name	Pin Number	Type	Description
DD[15:0]	61,63,1,3,6,10,12,14,15,13,11,7,5,2,64,62	DIO 8mA	Data Bus. This is a bi-directional data bus for a host and a device to transfer data, command, and status.
CSn[1:0]	47,48	DIO 8mA	Chip Select. Active-low signals from a host to select a Command Block or Control Block register of a device.
DA[2:0]	49, 51,50	DIO 4mA	Device Address. Address signals from a host to access a register or data port of the device.
DIORn/ HDMARDYn/ HSTROBE	58	DIO 8mA	IO Read/Ultra DMA Ready/Ultra DMA Data Strobe. DIORn: Active-low signal from a host to read a register or data port of a device. HDMARDYn: Active-low signal from a host to indicate its ready to receive Ultra DMA data-in burst from a device. HSTROBE: Signal from a host to latch data into a device at Ultra DMA data-out operation.
DIOWn/ STOP	59	DIO 8mA	IO Write/Stop Ultra DMA Burst. DIOWn: Active-low signal from a host to write a register or data port of a device. STOP: Active-high signal from a host to terminate an Ultra DMA transfer.
DMACKn	54	DIO 8mA	DMA Acknowledge. Active-low signal from a host to acknowledge the DMA request from a device.
DMARQ	60	DIO 8mA	DMA Request. Active-high signal from a device to request a DMA transfer.
INTRQ	53	DIO 8mA	Device Interrupt. Active-high signal from a device to interrupt a host.
IORDY/ DDMARDYn/ DSTROBE	55	DIO 8mA	IO Ready/Ultra DMA Ready/Ultra DMA Data Strobe. IORDY: Active-high signal from a device to extend the host cycle time for operation at PIO mode 3 and above. DDMARDYn: Active-low signal from a device used to indicate its ready to receive Ultra DMA data-out burst from a host. DSTROBE: Signal from a device used to latch data into a host at Ultra DMA data-in operation.
PDIAGn/ PATAOR	46	DIOH 8mA	Diagnostic Signal. In Host Bridge mode: PDIAGn provides the diagnostic signals from device 1 to device 0 to indicate the device 1 diagnosis is complete. In Device mode: PATAOR defines the pin order of parallel ATA interface. (see 5.6) 0: ATA interface signals in Normal Order mode. 1: ATA interface signals in Reverse Order mode.
RESETn	16	DIO 8mA	Hardware Reset. Active-low signal from a host to reset a device.
DASPn	34	DIOH 8mA	Slave Device Present. Active-low signal from Device 1 to Device 0 in Host Bridge mode to indicate the presence of slave device. In Device 0: configuration, this pin is an input. In Device 1: configuration, it is an output. This pin is used as slave present indicator at ATA power on device diagnostics phase, and used as device activity at command or data transfer. In Device Bridge mode, the pin is output (reserved).

Signal Name	Pin Number	Type	Description
SP	52	DIOL 4mA	Slave Device Present. Active-high signal from Device 1 to Device 0 in Host Bridge mode to indicate the presence of slave device. In Device 0 configuration, this pin is an input. In Device 1 configuration, it is an output. In Device Bridge mode, SP is cable detection pin, default setting is used 80-conductor cable. 0: 80-conductor cable is detected. 1: 40-conductor cable is detected.

5.5 Power Supply

Signal	Pin Number	Type	Description
AVDDH	24	AI	**Analog Power.** Analog 3.3V power supply. It should be bypassed to ground by a 0.1uF capacitance.
AVDDL	29	AI	**Analog Power.** Analog 1.8V power supply. It should be bypassed to ground by a 0.1uF capacitance.
AGND	25,30	AI	**Analog Ground**.
VCCO	4,44	DI	**Digital IO Power.** Digital 3.3V power supply. It should be bypassed to ground by a 0.1uF capacitance.
VCCK	9,41,56	DI	**Digital Core Power.** Digital 1.8V power supply. It should be bypassed to ground by a 0.1uF capacitance.
DGND	8,42,57	DI	**Digital ground.**

5.6 Configuration Interface

Signal Name	Pin Number	Type	Description
PORn	17	DIH	Power On Reset. Low-active global reset. It should be connected to an external RC to build the power on initialization.
SSCEN	35	DIL	Spread Spectrum Clock Enable. 0: Disable SATA spread spectrum clocking. (default) 1: Enable SATA spread spectrum clocking.
CLKSEL[1:0]	37, 36	DIL DIH	Reference Clock Selection. 01: 25MHz external reference clock. others: reserved.
PHYRDY	40	DO 4mA	Physical Layer Ready. 0: Serial ATA physical layer communication is not established. 1: Serial ATA physical layer communication is established.
MODE[2:0]	20,19,18	DIL DIH DIL	Operation Mode and Ultra DMA operation rate. Mode [2]: select Host/Device bridge mode. 0: Device bridge mode. 1: Host bridge mode. Mode [1:0]: select UDMA speed when FXDMA is set. 00: 100MB/s. 01: 133MB/s. 10: 150MB/s. (default) 11: Reserved. MODE[1:0] must never be set to “11” and shall never be left floating!! External Pull resistor must be added!!
MSSEL	33	DIOL 4mA	Master/Slave Selection. In Host Bridge mode: 0: Device 0 configuration. (default) 1: Device 1 configuration. In Device Bridge mode, the pin is output (reserved).
FXDMA	38	DIL	Fixed UDMA Data Rate. 0: Adjustable Ultra DMA data rate according to SET FEATURE command (EFh). 1: Negate SET FEATURE command, and fix Ultra DMA data rate specified by MODE[1:0] setting.
ATAIOEN	21	DIH	ATA IO Interface Enable. 0: Disable the ATA output pins, present ATA I/O output pins are Hi-Z. 1: Enable the ATA output pins.
PMEN	39	DIH	Power Management Command Enable.(reference 7.0) 0: Disable translating ATA Power Management feature command to Serial ATA Slumber mode. 1: Enable translating ATA Power Management feature command to Serial ATA Slumber mode.
UAI	43	DIH	On-chip UART input used for internal debugging.
UAO	45	DOH 4mA	On-chip UART output used for internal debugging.

5.7 Parallel ATA Reverse Order

The parallel ATA pin order is determined by PDIAGn/PATAOR in device bridge mode. The pin-out in reverse order is shown below.

Pin No.	Normal Order	Reverse Order
1	DD13	DD0
2	DD2	DD15
3	DD12	DMARQ
5	DD3	DIOWn
6	DD11	DIORn
7	DD4	DMACKn
10	DD10	INTRQ
11	DD5	SP
12	DD9	DA1
13	DD6	DA0
14	DD8	DA2
15	DD7	CS0n
16	RESETn	CS1n
34	DASPn	DASPn
47	CS1n	RESETn

Pin No.	Normal Order	Reverse Order
48	CS0n	DD7
49	DA2	DD8
50	DA0	DD6
51	DA1	DD9
52	SP	DD5
53	INTRQ	DD10
54	DMACKn	DD4
55	IORDY	IORDY
58	DIORn	DD11
59	DIOWn	DD3
60	DMARQ	DD12
61	DD15	DD2
62	DD0	DD13
63	DD14	DD1
64	DD1	DD14

6. Supported ATA/ATAPI Command List

6.1 PIO Data-in Commands

Command	Code	Support
CFA TRANSLATE SECTOR	87h	NO
DEVICE CONFIGURATION IDENTIFY	B1h(C2h)	YES
IDENTIFY DEVICE	ECh	YES
IDENTIFY COMPONENT	D0h	YES
IDENTIFY PACKET DEVICE	A1h	YES
READ BUFFER	E4h	YES
READ LOG EXT	2Fh	YES
READ MULTIPLE	C4h	YES
READ MULTIPLE EXT	29h	YES
READ SECTOR(S)	20h/21h	YES
READ SECTOR(S) EXT	24h	YES
READ LONG	22h/23h	YES
SMART READ DATA	B0h(D0h)	YES
SMART READ ATTRIBUTE THRESHOLDS	B0h(D1h)	YES
SMART READ LOG	B0h(D5h)	YES

6.2 PIO Data-Out Commands

Command	Code	Support
CFA WRITE MULTIPLE WITHOUT ERASE	CDh	NO
CFA WRITE SECTORS WITHOUT ERASE	38h	NO
DEVICE CONFIGURATION SET	B1h(C3h)	YES
DOWNLOAD MICROCODE	92h	YES
SECURITY DISABLE PASSWORD	F6h	YES
SECURITY ERASE UNIT	F4h	YES
SECURITY SET PASSWORD	F1h	YES
SECURITY UNLOCK	F2h	YES
SET MAX PASSWORD	F9h(01h)	YES
SET MAX UNLOCK	F9h(03h)	YES
SET MAX PASSWORD EXT	37h(01h)	YES
SET MAX UNLOCK EXT	37h(03h)	YES
SMART WRITE LOG	B0h(D6h)	YES
SMART WRITE ATTRIBUTE THRESHOLDS	B0h(D7h)	YES
WRITE BUFFER	E8h	YES
WRITE LOG EXT	3Fh	YES
WRITE MULTIPLE	C5h	YES
WRITE MULTIPLE EXT	39h	YES
WRITE SECTOR(S)	30h/31h	YES
WRITE SECTOR(S) EXT	34h	YES
WRITE LONG	32h/33h	YES
WRITE VERIFY SECTOR(S)	3Ch	YES

6.3 DMA Data-In Commands

Command	Code	Support
READ DMA	C8h/C9h	YES
IDENTIFY DEVICE DMA	EEh	YES
READ DMA EXT	25h	YES

6.4 DMA Data-Out Commands

Command	Code	Support
WRITE DMA	Cah/CBh	YES
WRITE DMA EXT	35h	YES

6.5 Queued DMA Commands

Command	Code	Support
READ DMA QUEUED	C7h	NO
READ DMA QUEUED EXT	26h	NO
WRITE DMA QUEUED	CCh	NO
WRITE DMA QUEUED EXT	36h	NO
SERVICE	A2h	NO

6.6 PACKET/DIAG Commands

Command	Code	Support
PACKET	A0h	YES
DEVICE RESET	08h	YES
EXECUTE DEVICE DIAGNOSTIC	90h	YES
IDENTIFY PACKET DEVICE	A1h	YES

6.7 Non-Data Commands

Command	Code	Support
CFA ERASE SECTORS	C0h	NO
CFA REQUEST EXTENDED ERROR	03h	NO
CHECK MEDIA CARD TYPE	D1h	YES
CHECK POWER MODE	E5h/98h	YES
DEVICE CONFIGURATION FREEZE LOCK	B1h(C1h)	YES
DEVICE CONFIGURATION RESTORE	B1h(C0h)	YES
FLUSH CACHE	E7h	YES
FLUSH CACHE EXT	EAh	YES
FORMAT TRACK	50h	YES

Command	Code	Support
GET MEDIA STATUS	DAh	YES
IDLE	E3h/97h	YES
IDLE IMMEDIATE	E1h/95h	YES
INITIALIZE DEVICE PARAMETERS	91h	YES
MEDIA EJECT	EDh	YES
MEDIA LOCK	DEh	YES
MEDIA UNLOCK	DFh	YES
NOP	00h	YES
RECALIBRATE	1xh	YES
READ NATIVE MAX ADDRESS	F8h	YES
READ NATIVE MAX ADDRESS EXT	27h	YES
READ VERIFY SECTOR(S)	40h/41h	YES
READ VERIFY SECTOR(S) EXT	42h	YES
SECURITY ERASE PREPARE	F3h	YES
SECURITY FREEZE LOCK	F5h	YES
SEEK	70h	YES
SET FEATURES	EFh	YES
SET MAX ADDRESS	F9h	YES
SET MAX LOCK	F9h(02h)	YES
SET MAX FREEZELOCK	F9h(04h)	YES
SET MAX ADDRESS EXT	37h	YES
SET MAX LOCK EXT	37h(02h)	YES
SET MAX FREEZE LOCK EXT	37h(04h)	YES
SET MULTIPLE MODE	C6h	YES
SLEEP	E6h/99h	YES
SMART DISABLE OPERATIONS	B0h(D9h)	YES
SMART ENABLE OPERATIONS	B0h(D8h)	YES
SMART ENABLE/DISABLE AUTOSAVE	B0h(D2h)	YES
SMART SAVE ATTRIBUTE VALUES	B0h(D3h)	YES
SMART EXECUTE OFF_LINE IMMEDIATE	B0h(D4h)	YES
SMART RETURN STATUS	B0h(DAh)	YES
SMART ENABLE/DISABLE AUTO OFFLINE	B0h(DBh)	YES
STANDBY	E2h/96h	YES
STANDBY IMMEDIATE	E0h/94h	YES

6.8 ATAPI PACKET Commands

Command	Code	Support
FORMAT UNIT	04h	YES
MODE SELECT(6)	15h	YES
MODE SELECT(10)	55h	YES
MEDIUM SCAN	38h	YES
SEND CUE SHEET	5Dh	YES
SEND DVD STRUCTURE	BFh	YES
SEND DIAGNOSTIC	1Dh	YES
SEND EVENT	A2h	YES
SEND KEY	A3h	YES

Command	Code	Support
SEND OPC INFORMATION	54h	YES
WRITE	0Ah	YES
WRITE(10)	2Ah	YES
WRITE(12)	AAh	YES
WRITE AND VERIFY(10)	2Eh	YES
WRITE AND VERIFY(12)	AEh	YES
WRITE BUFFER COMMAND	3Bh	YES
BLANK	A1h	YES
CLOSE TRACK/RZONE/SESSION/BORDER	5Bh	YES
ERASE	19h	YES
GET CONFIGURATION	46h	YES
GET EVENT/STATUS NOTIFICATION	4Ah	YES
GET PERFORMANCE	ACh	YES
INQUIRY	12h	YES
LOAD/UNLOAD MEDIUM	A6h	YES
MECHANISM STATUS	BDh	YES
MODE SENSE(6)	1Ah	YES
MODE SENSE(10)	5Ah	YES
PAUSE/RESUME	4Bh	YES
PLAY AUDIO(10)	45h	YES
PLAY AUDIO(12)	A5h	YES
PLAY AUDIO MSF	47h	YES
PLAY CD	BCh	YES
PREVENT/ALLOW MEDIUM REMOVAL	1Eh	YES
READ(6)	08h	YES
READ(10)	28h	YES
READ(12)	A8h	YES
READ BLOCK LIMITS	05h	YES
READ CAPACITY COMMAND	25h	YES
READ CD	BEh	YES
READ CD MSF	B9h	YES
READ DISC INFORMATION	51h	YES
READ DVD STRUCTURE	ADh	YES
READ FORMAT CAPACITIES	23h	YES
READ HEADER	44h	YES
READ MASTER CUE	59h	YES
READ POSITION	34h	YES
READ REVERSE	0Fh	YES
READ SUBCHANNEL	42h	YES
READ TOC/PMA/ATIP	43h	YES
READ TRACK/RZONE INFORMATION	52h	YES
RECEIVE DIAGNOSTICS	1Ch	YES
RECOVER BUFFERED DATA	14h	YES
RELEASE	17h	YES
REPAIR RZONE	58h	YES
REPORT DENSITY SUPPORT	44h	YES
REPORT KEY	A4h	YES
RESERVE	16h	YES
REQUEST SENSE	03h	YES

Command	Code	Support
RESERVE TRACK/RZONE	53h	YES
REWIND	01h	YES
SCAN	BAh	YES
SEEK	2Bh	YES
SET CD SPEED	BBh	YES
SET READ AHEAD	A7h	YES
SPACE	11h	YES
START/STOP UNIT	1Bh	YES
STOP PLAY/SCAN	4Eh	YES
SYNCHRONIZE CACHE	35h	YES
TEST UNIT READY	00h	YES
VERIFY	13h	YES
VERIFY(10)	2Fh	YES
VERIFY(12)	AFh	YES
READ BUFFER COMMAND	3Ch	YES
READ BUFFER CAPACITY COMMAND	5Ch	YES
WRITE FILEMARKS	10h	YES

6.9 Ultra DMA Transfer Rate

The JM20330 sets its UDMA mode according to:

1. Setting by the SET FEATURES command (EFh) when FXDMA is zero.
2. Setting MODE[1:0] pin when FXDMA is one.

Ultra DMA Mode (Set Feature command)	Max Data Rate (MB/s)
0	16.7
1	25
2	33
3	44
4	66
5	100
6	120
7	150

6.10 Master-Only Operation in Device Bridge Mode

In legacy IDE framework, we can attach two IDE drives on the IDE cable. The two drives are master and slave correspondingly. But in SATA framework, we can only attach one SATA drive on the SATA port. From the SATA Host's viewpoint, the attached SATA drive is master. In order to meet the SATA framework, if we use JM20330 to bridge the SATA Host and IDE drive the jumper selection of the attached IDE drive must be master.

7. Power Management

There are two kinds of power management stated in this chapter, they are ATA power management and SATA power management.

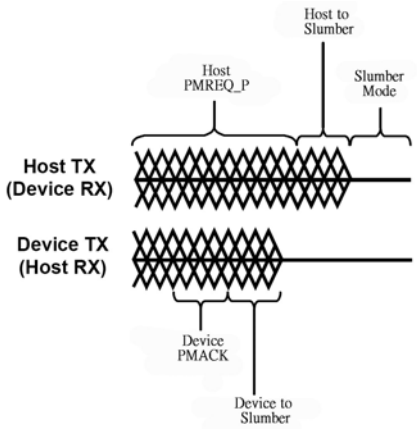
JM20330 DO support ATA power management command set, such as IDLE, IDLE IMMEDIATE, STANDBY, STANDBY IMMEDIATE and SLEEP. When any ATA power management command is from SATA/IDE Host, JM20330 will pass the command to IDE/SATA HDD(ODD) regardless of the PMEN(pin39) setting.

For SATA power management(Partial and Slumber mode), JM20330 can accept or initiate the SATA power management. Customer can use PMEN to enable or disable this feature. If the PMEN is low, JM20330 will not accept or initiate any SATA power management. If the PMEN is high, JM20330 will accept or initiate the SATA power management. There is no standard specification define how a bridge chip initiate the SATA power management. JMicron use ATA power management command to begin the SATA Slumber mode.

In Host bridge mode, when IDE Host perform any IDE power management command, JM20330 will pass the command to SATA HDD(ODD). After the command is finished, JM20330 will start the SATA slumber mode if the PMEN is high. Once the SATA HDD(ODD) accept this slumber mode, the SATA interface is really in slumber mode. Otherwise, the SATA interface is still active.

In Device Bridge mode, when SATA host transmits any ATA power management command, JM20330 will pass the command to PATA HDD(ODD). After the command is finished, JM20330 will start the SATA slumber mode if the PMEN is high and SATA Host accept JM20330 initiating the SATA slumber mode. By SATA Spec, SATA Device has no permission to initiate the SATA power management unless SATA Host enabling this feature by SET FEATURE command.

SATA interface enter slumber state depend on primitive PMREQ_S and PMACK between the host and the device, the following figure shows the power management sequence on SATA interface.



8. Electrical Characteristics

8.1 Power Requirements

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital I/O pad power supply			7.79	11.95	14.25	mA
Digital core power supply			39.46	44.22	48.92	mA
Analog power supply	AVDDH(ABS)		17.79	17.94	18.08	mA
Analog power supply	AVDDL(ABS)		47.83	52.30	56.46	mA
Input High Current	IIH		-10		10	uA
Input with 31 KΩ pull down			40	80	160	uA
Input low Current	IIL		-10		10	uA
Input with 31 KΩ pull up			-160	-80	-40	uA

8.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Absolute digital I/O power supply	VCCO(ABS)		-0.5		4.4	V
Absolute digital core power supply	VCCK(ABS)		-0.5		3.2	V
Absolute analog power supply	AVDDH(ABS)		-0.5		4.4	V
Absolute analog power supply	AVDDL(ABS)		-0.5		3.2	V
Absolute Input Voltage			-0.4		VCCO+0.4	V
Absolute Storage Temperature			-65		+150	oC
Absolute Junction Temperature					+125	oC

8.3 Typical Operation Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Ambient operation temperature		For commercial spec.	0		70	oC
Ambient operation temperature		For industry spec. **	-40		85	oC
Operation digital I/O power supply	VCCO		3.0	3.3	3.6	V
Operation digital core power supply	VCCK		1.62	1.8	1.98	V
Operation analog power supply	AVDDH		3.0	3.3	3.6	V
Operation analog power supply	AVDDL		1.62	1.8	1.98	V

8.4 DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	VIL		0		0.8	V
Input high voltage	VIH		2.0			V
Output low voltage	VOL		0		0.4	V
Output high voltage	VIH		2.6		3.6	V

8.5 ATA I/O DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
DC sink current	IOL		8			mA
Internal pull-up current			40		160	uA
Input low-voltage	VIL				0.8	V
Input high-voltage	VIH		2.0		5.0	V
Output low-voltage	VOL		0		0.4	V
Output high-voltage	VOH		2.6		3.6	V

8.6 ATA I/O AC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Rising slew-rate			0.4	0.7	1.0	V/ns
Falling slew-rate			0.4	0.7	1.0	V/ns
Device Capacitance	C device				27	pF

8.7 Slumber Power Consumption

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital I/O pad power supply			3.79	4.51	6.07	mA
Digital core power supply			5.15	5.67	6.34	mA
Analog power supply	AVDDH(ABS)		17.11	17.18	17.36	mA
Analog power supply	AVDDL(ABS)		26.02	27.10	30.05	mA