JM38510/11401/11402/11403/ 11404/11405/11406

JAN JFET-INPUT
OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low-power, internally-compensated JFET-input operational amplifier as specified in MIL-M-38510/114 for device types 01 to 06. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

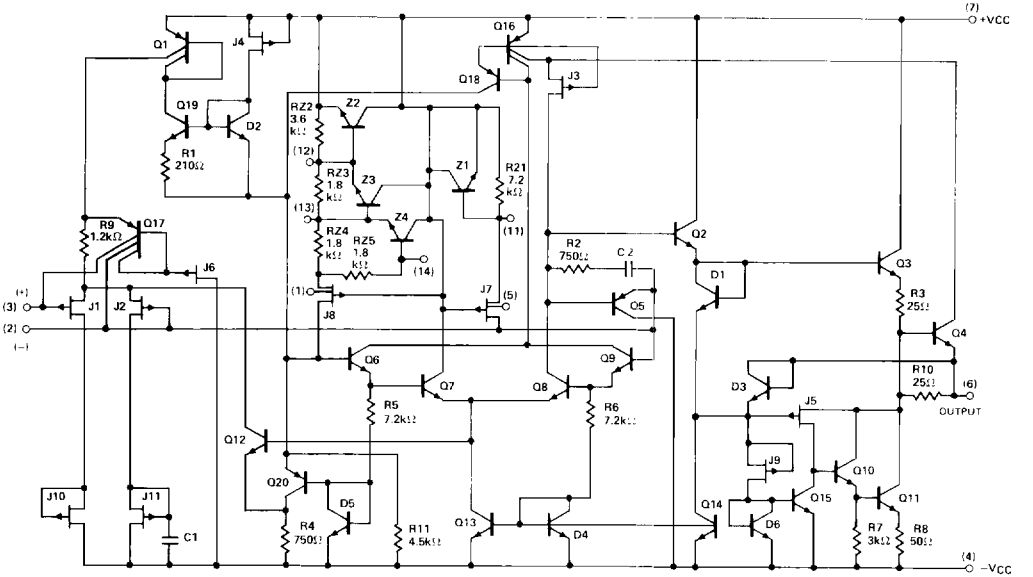
Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/114 for Class B and Class S processed devices.

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
01	LF-155
04	LF-155A
02	LF-156
05	LF-156A
03	LF-157
06	LF-157A

SIMPLIFIED SCHEMATIC



NOTE: For values of C1, C2, R5, R6 see the following table:

	01 04 02 05	03 06
C1	7pF	1.7pF
C2	7pF	1.7pF
R5	7.2kΩ	3.6kΩ
R6	7.2kΩ	3.6kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range ..... ±22V
Input Voltage Range (Note 1) ..... ±20V
Differential Input Voltage Range ..... ±40V
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... T_j = 175°C (Note 3)
Storage Temperature Range ..... −65°C to +150°C
Output Short-Circuit Duration ..... Unlimited (Note 2)

NOTES:
1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Short circuit may be to ground to either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), T_j = 275°C.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... ±5 to ±20 VDC
Ambient Temperature Range ..... −55°C to +125°C

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

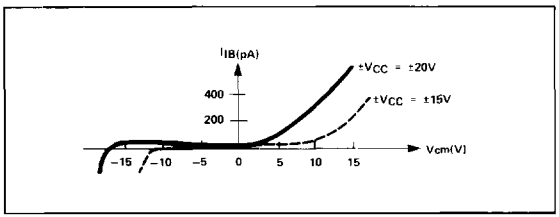
PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	04 LIMITS MIN	04 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC}$ = ±5V, V_{CM} = 0V, T_A = 25°C	−5	5	−2	2	mV
		$\pm V_{CC}$ = ±20V, V_{CM} = ±15V, 0V, −55°C ≤ T_A ≤ +125°C	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC}$ = ±20V, V_{CM} = 0V	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC}$ = ±20V, V_{CM} = 0V, T_j = 25°C	−20	20	−20	20	pA
		T_j = 125°C	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC}$ = ±20V, V_{CM} = +15V, T_j = 25°C	−100	3500	−100	3500	pA
		t ≤ 25ms T_j = 125°C	−10	60	−10	60	nA
	$-I_{IB}$	$\pm V_{CC}$ = ±15V, V_{CM} = +10V, T_j = 25°C	−100	300	−100	300	pA
		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
		$\pm V_{CC}$ = ±20V, −15V ≤ V_{CM} ≤ 0V, T_j = 25°C	−100	100	−100	100	pA
		t ≤ 25ms T_j = 125°C	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC}$ = 10V, $-V_{CC}$ = −20V	85	—	85	—	dB
	−PSRR	$+V_{CC}$ = 20V, $-V_{CC}$ = −10V					
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC}$ = ±20V, V_{IN} = ±15V	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC}$ = ±20V	+8	—	+8	—	mV
	V_{IO} ADJ (−)	$\pm V_{CC}$ = ±20V	—	−8	—	−8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC}$ = ±15V, t ≤ 25ms (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	T_A = −55°C	—	11	—	11	mA
		$\pm V_{CC}$ = ±15V, T_A = +25°C	—	4	—	4	
		T_A = +125°C	—	4	—	4	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC}$ = ±20V, R_L = 10kΩ	±16	—	±16	—	V
		$\pm V_{CC}$ = ±20V, R_L = 2kΩ	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$	$\pm V_{CC}$ = ±20V, V_{OUT} = ±15V, R_L = 2kΩ, T_A = 25°C	50	—	50	—	V/mV
	$A_{VS(-)}$	−55°C ≤ T_A ≤ +125°C	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC}$ = ±5V, R_L = 2kΩ, V_{OUT} = ±2V	10	—	10	—	V/mV

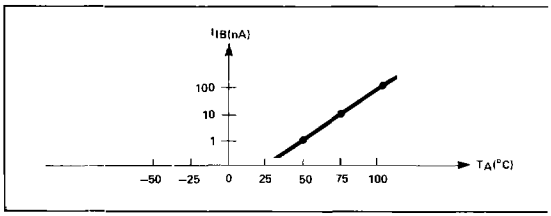
ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS MIN	01 LIMITS MAX	04 LIMITS MIN	04 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC}$ = ±15V, R_L = 2kΩ, A_V = 1 C_L = 100pF, See Figure 2 V_{IN} = 50mV	—	150	—	150	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC}$ = ±15V, R_L = 2kΩ, A_V = 1 C_L = 100pF, See Figure 2 V_{IN} = 50mV	—	40	—	40	%
Slew Rate	SR(+) and SR(−)	V_{IN} = ±5V, $\pm V_{CC}$ = ±15V A_V = 1, See Figure 2 T_A = 25°C T_A = −55°C, +125°C	2 1	— —	3 1.5	— —	V/μs
Settling Time	ts(+) and ts(−)	$\pm V_{CC}$ = ±15V (0.1% error) T_A = 25°C, A_V = −1 See Figure 3	—	4000	—	4000	ns
Noise (Referred to Input) Broadband	N_I(BB)	$\pm V_{CC}$ = ±20V, T_A = 25°C Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	N_I(PC)	$\pm V_{CC}$ = ±20V, T_A = 25°C Bandwidth = 5kHz	—	40	—	40	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_j. Measurement of bias current is specified at T_j rather than T_A, since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at T_A = −55°C is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:





3. Negative I_{IB} minimum limits reflect the characteristics of device with bi current compensation.
4. CMR is calculated from V_{IO} measurements at V_{CM} = +15V and −15V.
5. Continuous limits shall be considerably lower. Protection for shorts either supply exists providing that T_j(max) ≤ 175°C.
6. Because of thermal feedback effects from output to input, open-loop ga is not guaranteed to be linear or positive over the operating range. The requirements, if needed, should be specified by the user in addition procurement documents.

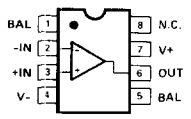
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can), Package Type Designator "G"; and Appendix C, Case Outline D-4 (8 Lead Dual-in-Line) Package Type Designator "P".

POWER AND THERMAL CHARACTERISTICS

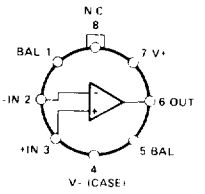
Package	Case outline	Maximum allowable power dissipation	Maximum θJ—C	Maximum θJ—A
8 Lead Can (TO-99)	G	330mW at T_A = 125°C	40°C/W	150°C/W
8 Lead Hermetic DIP (Dual-in-Line)	P	417mW at T_A = 125°C	50°C/W	120°C/W

PIN CONNECTIONS



8-PIN HERMETIC DIP
TIN-REFLOW LEAD TYPE
(Z2-Suffix)

SOLDER-DIPPED LEAD TYPE
(Z5-Suffix)



TO-99
GOLD-PLATE LEAD TYPE
(J1-Suffix)

SOLDER-DIPPED LEAD TYPE
(J5-Suffix)

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

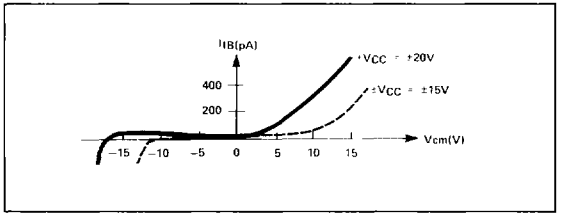
PARAMETER	SYMBOL	CONDITIONS	02 LIMITS MIN	02 LIMITS MAX	05 LIMITS MIN	05 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V$, $V_{CM} = 0V$, $T_A = 25°C$	−5	5	−2	2	mV
		$\pm V_{CC} = \pm 20V$, $V_{CM} = \pm 15V, 0V$, $-55°C \le T_A \le +125°C$	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $T_j = 25°C$	−20	20	−20	20	pA
		$T_j = 125°C$	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC} = \pm 20V$, $V_{CM} = +15V$, $T_j = 25°C$	−100	3500	−100	3500	pA
		$t \le 25ms$ $T_j = 125°C$	−10	60	−10	60	nA
	$-I_{IB}$	$\pm V_{CC} = \pm 15V$, $V_{CM} = +10V$, $T_j = 25°C$	−100	300	−100	300	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
		$\pm V_{CC} = \pm 20V$, $-15V \le V_{CM} \le 0V$, $T_j = 25°C$	−100	100	−100	100	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V, -V_{CC} = -20V$	85	—	85	—	dB
	−PSRR	$+V_{CC} = 20V, -V_{CC} = -10V$					
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$, $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ(+)	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	V_{IO} ADJ(−)	$\pm V_{CC} = \pm 20V$	—	−8	—	−8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$, $t \le 25ms$ (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$, $t \le 25ms$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55°C$	—	11	—	11	mA
		$\pm V_{CC} = \pm 15V$, $T_A = +25°C$	—	7	—	7	
		$T_A = +125°C$	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V$, $R_L = 10k\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V$, $R_L = 2k\Omega$	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$	$\pm V_{CC} = \pm 20V$, $V_{OUT} = \pm 15V$, $R_L = 2k\Omega$, $T_A = 25°C$	50	—	50	—	V/mV
	$A_{VS(-)}$	$-55°C \le T_A \le +125°C$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$, $R_L = 2k\Omega$, $V_{OUT} = \pm 2V$	10	—	10	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$, $C_L = 100pF$, See Figure 2, $V_{IN} = 50mV$	—	100	—	100	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$, $C_L = 100pF$, See Figure 2, $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	SR(+) and SR(−)	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$, $A_V = 1$, See Figure 2, $T_A = 25°C$	7.5	—	10	—	V/µs
		$T_A = -55°C, +125°C$	5	—	7	—	
Settling Time	ts(+) and ts(−)	$\pm V_{CC} = \pm 15V$ (0.1% error), $T_A = 25°C$, $A_V = -1$, See Figure 3	—	4000	—	4000	ns

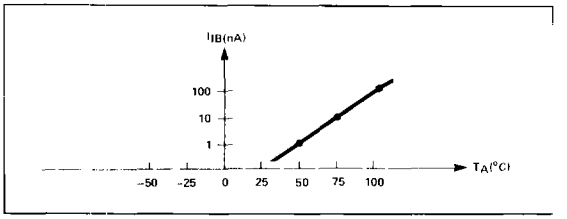
ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	02 LIMITS MIN	02 LIMITS MAX	05 LIMITS MIN	05 LIMITS MAX	UNITS
Noise (Referred to Input) Broadband	N_I(BB)	$\pm V_{CC}$ = ±20V, T_A = 25°C Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	N_I(PC)	$\pm V_{CC}$ = ±20V, T_A = 25°C Bandwidth = 5kHz	—	40	—	40	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_j. Measurement of bias current is specified at T_j rather than T_A, since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at T_A = −55°C is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:





3. Negative I_{IB} minimum limits reflect the characteristics of device with bias current compensation.
4. CMR is calculated from V_{IO} measurements at V_{CM} = +15V and −15V.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that T_j(max) ≤ 175°C.
6. Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/11401BGC	PM155J1/38510
JM38510/11401BGA	PM155J5/38510
JM38510/11401BPB	PM155Z2/38510
JM38510/11401BPA	PM155Z5/38510
JM38510/11404BGC	PM155AJ1/38510
JM38510/11404BGA	PM155AJ5/38510
JM38510/11404BPB	PM155AZ2/38510
JM38510/11404BPA	PM155AZ5/38510
JM38510/11402BGC	PM156J1/38510
JM38510/11402BGA	PM156J5/38510
JM38510/11402BPB	PM156Z2/38510
JM38510/11402BPA	PM156Z5/38510
JM38510/11401SGA	PM155SJ5/38510
JM38510/11402SGA	PM156SJ5/38510*
JM38510/11404SGA	PM155SAJ5/38510
JM38510/11405SGA	PM156SAJ5/38510

* Undergoing Part 1 qualification as of 1/90.

JAN SLASH SHEET	PMI DEVICE
JM38510/11405BGC	PM156AJ1/38510
JM38510/11405BGA	PM156AJ5/38510
JM38510/11405BPB	PM156AZ2/38510
JM38510/11405BPA	PM156AZ5/38510
JM38510/11403BGC	PM157J1/38510
JM38510/11403BGA	PM157J5/38510
JM38510/11403BPB	PM157Z2/38510
JM38510/11403BPA	PM157Z5/38510
JM38510/11406BGC	PM157AJ1/38510
JM38510/11406BGA	PM157AJ5/38510
JM38510/11406BPB	PM157AZ2/38510
JM38510/11406BPA	PM157AZ5/38510

ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted.

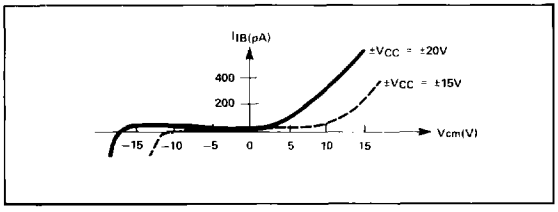
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS MIN	03 LIMITS MAX	06 LIMITS MIN	06 LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V$, $V_{CM} = 0V$ $T_A = 25°C$	−5	5	−2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V, 0V$ $-55°C \le T_A \le +125°C$	−7	7	−2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	−30	30	−10	10	µV/°C
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $T_j = 25°C$	−20	20	−20	20	pA
		$T_j = 125°C$	−20	20	−20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC} = \pm 20V$, $V_{CM} = +15V$ $T_j = 25°C$	−100	3500	−100	3500	pA
		$t \le 25ms$ $T_j = 125°C$	−10	60	−10	60	nA
	$-I_{IB}$	$\pm V_{CC} = \pm 15V$, $V_{CM} = +10V$ $T_j = 25°C$	−100	300	−100	300	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
		$\pm V_{CC} = \pm 20V$, $-15V \le V_{CM} \le 0V$ $T_j = 25°C$	−100	100	−100	100	pA
		$t \le 25ms$ $T_j = 125°C$	−10	50	−10	50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V$, $-V_{CC} = -20V$	85	—	85	—	dB
	−PSRR	$+V_{CC} = 20V$, $-V_{CC} = -10V$					
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	V_{IO} ADJ(+)	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	V_{IO} ADJ(−)	$\pm V_{CC} = \pm 20V$	—	−8	—	−8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	−50	—	−50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \le 25ms$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55°C$	—	11	—	11	mA
		$\pm V_{CC} = \pm 15V$, $T_A = +25°C$	—	7	—	7	
		$T_A = +125°C$	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V$, $R_L = 10k\Omega$	±16	—	±16	—	V
		$\pm V_{CC} = \pm 20V$, $R_L = 2k\Omega$	±15	—	±15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$	$\pm V_{CC} = \pm 20V$, $V_{OUT} = \pm 15V$ $R_L = 2k\Omega$, $T_A = 25°C$	50	—	50	—	V/mV
	$A_{VS(-)}$	$-55°C \le T_A \le +125°C$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

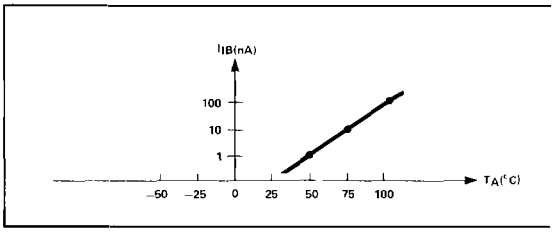
ELECTRICAL CHARACTERISTICS at V_{CC} from ±5V to ±20V; source resistance = 50 ohm; ambient temperature range = −55°C to +125°C and figure 1, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	03 LIMITS MIN	03 LIMITS MAX	06 LIMITS MIN	06 LIMITS MAX	UNITS
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	450	—	450	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	25	—	25	%
Slew Rate	$SR(+)$ and $SR(-)$	$V_{IN} = \pm 1V$, $\pm V_{CC} = \pm 15V$ $A_V = 5$, See Figure 2 $T_A = 25°C$ $T_A = -55°C, +125°C$	30 20	— —	40 25	— —	V/μs
Settling Time	$ts(+)$ and $ts(-)$	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25°C$, $A_V = -5$ See Figure 3	—	800	—	800	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25°C$ Bandwidth = 5kHz	—	40	—	40	μV_{pk}

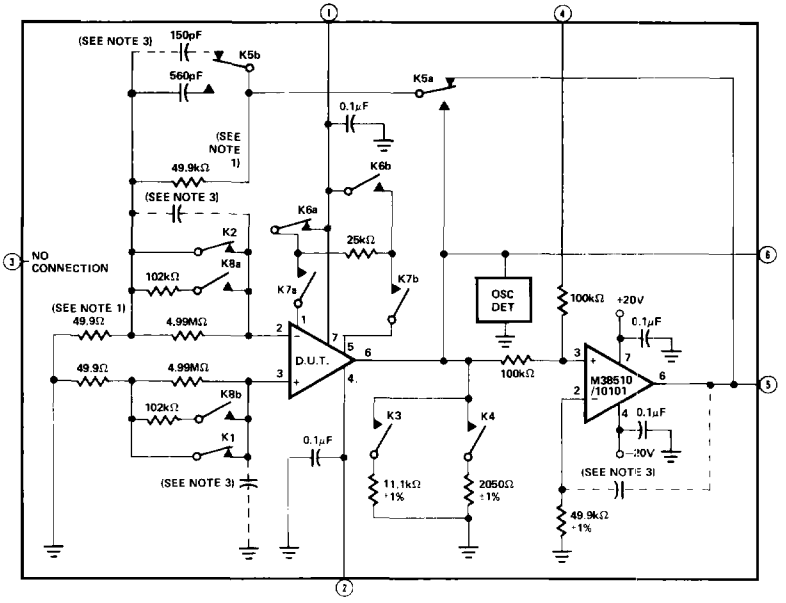
NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at $T_A = -55°C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:





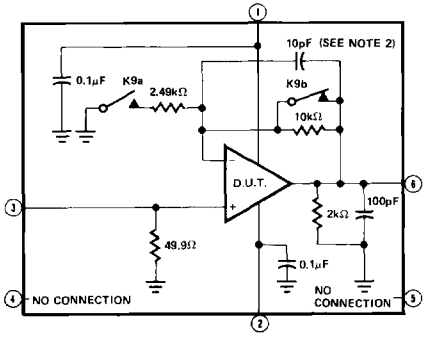
3. Negative I_{IB} minimum limits reflect the characteristics of device with bia current compensation.
4. CMR is ca culated from V_{IO} measurements at $V_{CM} = +15V$ and −15V.
5. Continuous limits shall be considerably lower. Protection for shorts t either supply exists providing that T_J (max) ≤ 175°C.
6. Because of thermal feedback effects from output to input, open-loop gai is not guaranteed to be linear or positive over the operating range. Thes requirements, if needed, should be specified by the user in additiona procurement documents.

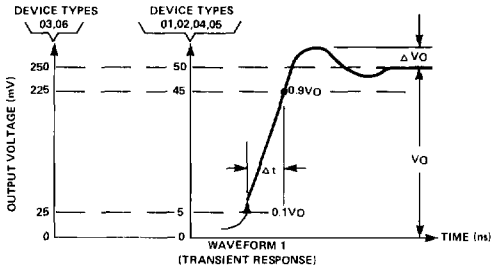


NOTES:

1. All resistors are ±0.1% tolerance and all capacitors are ±10% tolerance, unless otherwise specified.
2. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit $\pm V_{CC}$, etc.).
3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feedback. The other method is with a capacitor in parallel with the 49.9kΩ closed-loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least five loop time constants before the value is measured.
4. Adequate settling time should be allowed such that each parameter has settled to within 5% of its final value.
5. All relays are shown in the normal de-energized state.
6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (Pin 5) value is measured.
7. The load resistors 2050Ω and 11.1kΩ yield effective load resistances of 2kΩ and 10kΩ respectively.
8. Any oscillation greater than 300mV in amplitude (peak-to-peak) shall be cause for device failure.

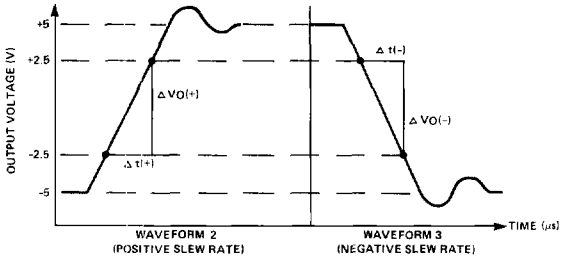
Figure 1. Test Circuit for Static Tests





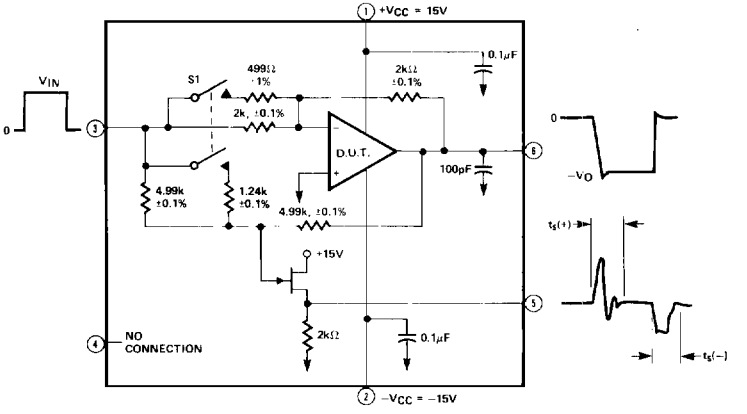
NOTES:

1. Resistors are ±1.0% tolerance and capacitors are ± 10% tolerance.
2. This capacitance includes the actual measured value with stray and wire capacitance.
3. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.



PARAMETER SYMBOL	DEVICE TYPE	INPUT PULSE SIGNAL AT $t_r \leq 50ns$	OUTPUT PULSE SIGNAL	EQUATION
TR (t_r)	ALL	+50mV	WAVEFORM 1	TR (t_r) = Δt
TR (O_S)	ALL	+50mV	WAVEFORM 1	TR (O_S) = 100 ($\Delta V_O/V_O$) %
SR (+)	01, 02, 04, 05 03, 06	−5V to +5V STEP −1V to +1V STEP	WAVEFORM 2 WAVEFORM 2	SR (+) = $\Delta V_O(+)/\Delta t(+)$
SR (−)	01, 02, 04, 05 03, 06	+5V to −5V STEP −1V to +1V STEP	WAVEFORM 3 WAVEFORM 3	SR (−) = $\Delta V_O(-)/\Delta t(-)$

Figure 2. Test Circuit for Transient Response and Slew Rate.



NOTES:

1. Resistors are ±1.0% and capacitors are ±10%, unless otherwise specified.
2. Precaution shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.
3. For device types 01, 02, 04 and 05, S1 is open, $A_V = -1$ and $V_{IN} = 10V$.
4. For device types 03 and 06, S1 is closed, $A_V = -5$ and $V_{IN} = 2V$.
5. Settling time, t_s measured on Pin 5, is the interval during which the summing node is not nulled within the specified accuracy referred to the output.

Figure 3. Test Circuit for Settling Time

BURN-IN

Devices supplied by PMI have been subjected to burn-in per Method 1015 of MIL-STD-883 using test condition C with circuit shown on Figure 4 or test condition F using circuit shown on Figure 5.

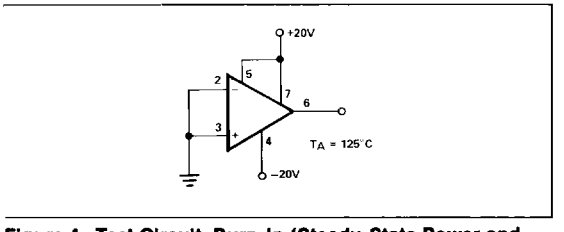


Figure 4. Test Circuit, Burn-In (Steady-State Power and Reverse Bias) and Operating Life Test

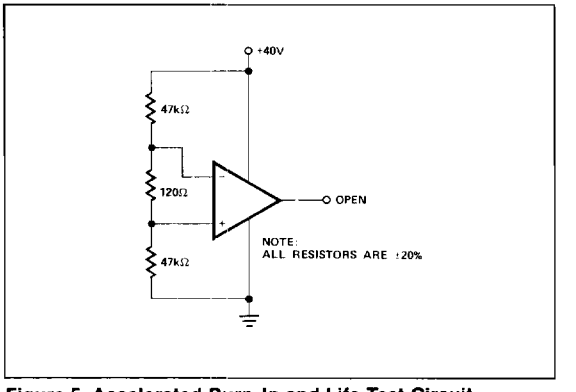


Figure 5. Accelerated Burn-In and Life Test Circuit