JMD330 Serial ATA Bridge Chip

Overview

The JMicron JMD330 Bridge is a single chip solution for serial and parallel ATA translation. It includes the Serial ATA PHY, Link, Transport, and parallel ATA (application layer) controller. The main applications are for legacy IDE storage devices connecting to newer chipset supporting serial ATA, such as the iCH5 south bridge of Intel chipset.

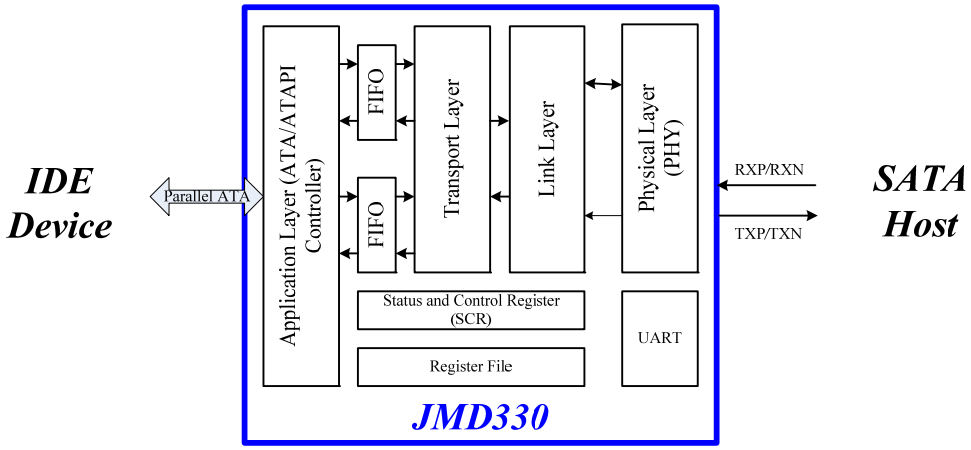
The Serial ATA physical, link, and transport layer are compliance to Serial ATA Generation 1, which supports a 1.5Gbps data rate. The application layer supports both the ATA register command set and PACKET command set, which could drive both the Hard Disk Drive and ATAPI Optical Storage such as CR-ROM, CD-RW, DVD-ROM, DVD-RW, etc.

This chip is designed by 0.18um CMOS technology and 64-pin TQFP or QFN package.

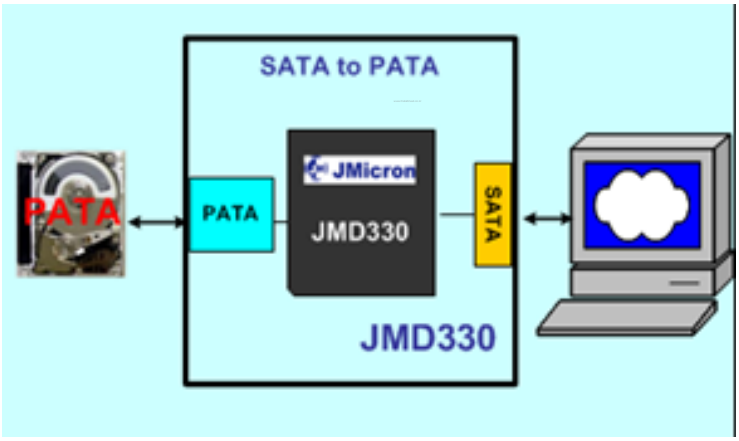
Features

- 0.18um CMOS technology.
- Compliance with Gen1i/Gen1m of Serial ATA II Electrical Specification 2.6.
- 1.8V and 3.3V power system.
- 25MHz external reference clock.
- 64-pin TQFP and QFN packages.
- Support ATA/ATAPI-7 specification.
- ATA/ATAPI PIO Mode 0, 1, 2, 3, 4.
- ATA/ATAPI Multi-Word DMA Mode 0, 1, 2.
- ATA/ATAPI Ultra DMA Mode 0, 1, 2, 3, 4, 5, 6, 7.
- ATA/ATAPI PACKET command feature set.
- ATA/ATAPI LBA48 addressing mode associated with 2-byte sector count.
- Serial ATA power saving modes.
- Serial ATA hot-plug.
- SATA II Asynchronous Signal Recovery support.

Functional Block Diagram



Application



Product Information

Name	Description
JMD330	Serial ATA Bridge Chip

Design Kit

1	JMD330 Data Sheet
2	JMD330 Design Guide
3	*Application EVB*

Contact Information

Department	Email
Sales	sales@jmicron.com
Tech. Support	*fae@jmicron.com*