JMF605

ARM Base SATAII to Flash Controller

Overview

JMF605 is a single chip, supports SATA II to NAND flash interface. It is native design to provide higher bandwidth for flash memory access.

JMF605 can support the maximum read and write speed to drive the limit of flash memory. JMF605 has the best supporting to the latest NAND flash memory, including Samsung, Toshiba, Hynix, Micron and IM Flash. It also provides the embedded hardware error correction code (ECC), wear leveling, and bad block management technology in this chip. In order to resolve compatibility issue, JMF605 provides the on line firmware upgrade ability.

JMF605 provides embedded processor, internal masked ROM, data SRAM, SATA link/transport layer, SATA PHY. Data swap between different interfaces can be done very efficiency by DMA without CPU involvement. Based on the efficient architecture, the JMF605 can provide the best performance.

Features

Compliance

- Compliant with Serial ATA International Organization: Serial ATA Revision 2.6.

SATA I/II

- Supports 1-port 1.5/3.0Gbps SATA I/II interface.

CPU

- Embedded processor.
- Embedded masked program ROM.
- Embedded system RAM.

FLASH

- Supports maximum CEs to 16 CEs.
- Support 5x/4x/3x/2x nm Flash
- Enhanced endurance by dynamic/static wear-leveling.
- Supports 4K/8K bytes page size.
- Supports dynamic power management.
- SMART (Self-Monitoring, Analysis and Reporting Technology).

- Data integrity under power-cycling.
- Supports 8 bits Flash interface.
- Supports BCH ECC 16 bits or 24 bits in 1024 bytes

SYSTEM

- Integrated 1-SATA II port and 4-channels Flash controller.
- LED indicator for SATA read/write access.
- LED indicator for SATA PHY link up.
- Provides 8 GPIO pins for customer.
- Provides UART and JTAG for S/W debugging.
- Built-in power-up self-test (BIST).
- Manual and automatic self-diagnostics.
- Provides voltage low detect interrupt.
- 130-ball LFBGA package.

Firmware

- Support NCQ on this controller.
- Support LBA24 & LBA48 on this controller.
- Support 1 to 8 banks selected free.
- Support 2 to 4 channels selected free.

Block Diagram

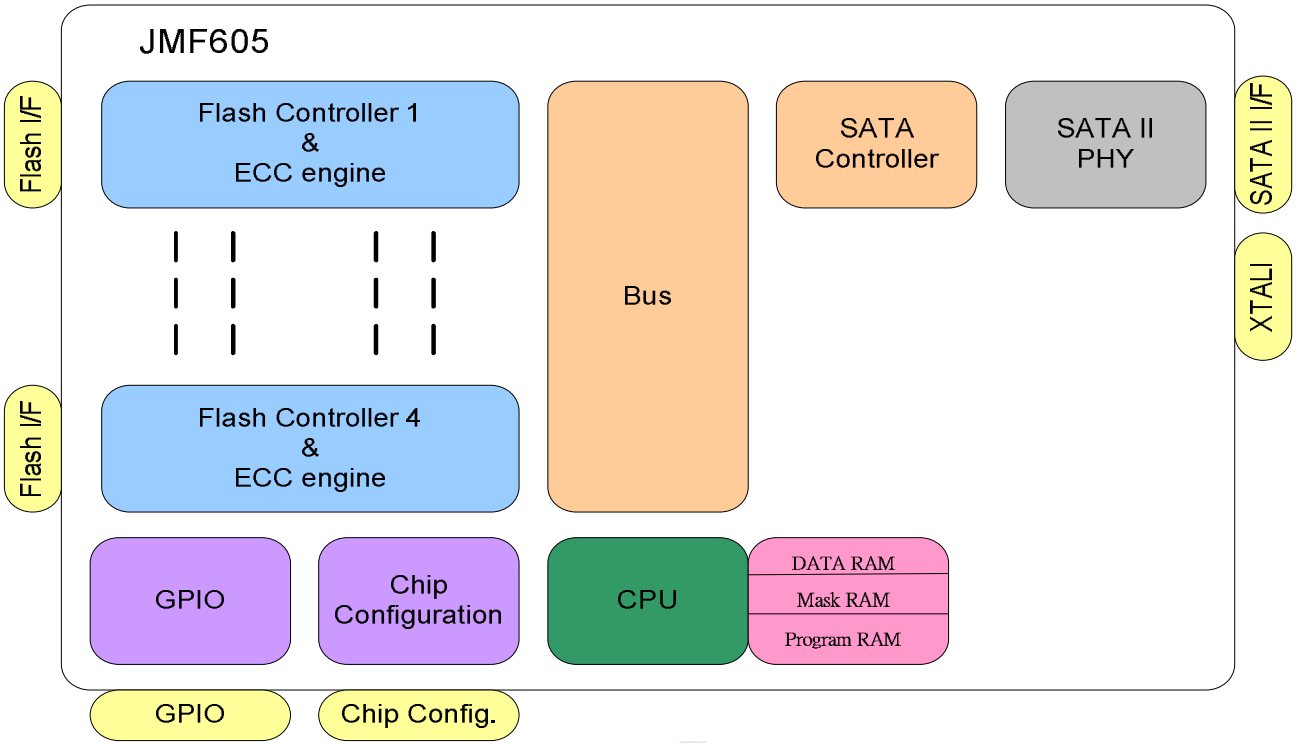

Figure 1: JMF605 Block Diagram

Total capacity

density/per flash	Support CE pins/per flash	maximum flash number	Total capacity
1G x 8 Bits (8Gb)	1 CE pin	16	16G Bytes
2G x 8 Bits (16Gb)	1 CE/ 2 CE pin	16	32G Bytes
4G x 8 Bits (32Gb)	1 CE/ 2 CE pin	16	64G Bytes
8G x 8 Bits (64Gb)	2 CE pin	16	128G Bytes
16G x 8 Bits (128Gb)	4 CE pin	8	128G Bytes

Table 1: JMF605 Total capacity table

Product Information

Name	Description
JMF605	ARM Base SATA-II to Flash Controller

Document

1	JMF605 Data Sheet
2	JMF605 Specification
3	JMF605 Hardware Design Guide
4	JMF605 Hardware Sehcmatic

Contact Information

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