JMS551

SuperSpeed USB to 2 ports

SATA II 3.0G Bridge

Datasheet

Revision 1.0.3

Revision History

Version	Date	Revision Description
1.0.3	2010/01/19	Add performance benchmark
1.0.2	2010/01/13	Modify SSRXP/SSRXN constraint.
1.0.1	2009/12/21	Add power-on sequence definition
1.0.0	2009/11/12	Version 1.0.0 released

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http://www.JMicron.com or send email to sales@jmicron.com

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1. Overviews

1.1 FUNCTION OVERVIEW

1.1.1 FEATURES

- ➤ Complies with Gen2i/Gen2m of Serial ATA II Electrical Specification 2.6
- ➤ Supports SATA II Asynchronous Signal Recovery (Hot Plug) feature
- ➤ Supports SATA to SATA pass through
- ➤ Complies with USB 3.0 Specification, USB Mass Storage Class, Bulk-Only Transport Specification
- ➤ Supports USB Super-Speed/High-Speed/Full-Speed Operation
- ➤ Supports USB HID operation
- ➤ Supports USB2.0/USB3.0/eSATA power saving mode
- ➤ Supports Dual LUN for USB2.0/USB3.0
- ➤ Supports Hardware RAID for RAID0 (striping) and RAID1 (spanning) over USB2.0/USB3.0
- ➤ Supports AES-128/256 for data encryption over USB2.0/USB3.0/eSATA
- ➤ Supports external SPI NVRAM for Vendor VID/PID of USB2.0/USB3.0/eSATA device controller
- ➤ Supports ATA/ATAPI PACKET command set
- ➤ 30 GPIOs for customization
- ➤ Provides hardware control PWM
- ➤ Provides software utilities for downloading the upgraded firmware code under USB2.0/USB3.0
- ➤ Design for Win2000, WinXP, WinVista, Win7, MAC 9.2 or later version.
- ➤ Supports 25MHz external crystal
- ➤ Embedded 3.3V to 1.2V voltage regulator
- ➤ 0.13um CMOS technology
- ➤ 100 LQFP package (14x14)

1.1.2 BLOCK DIAGRAM
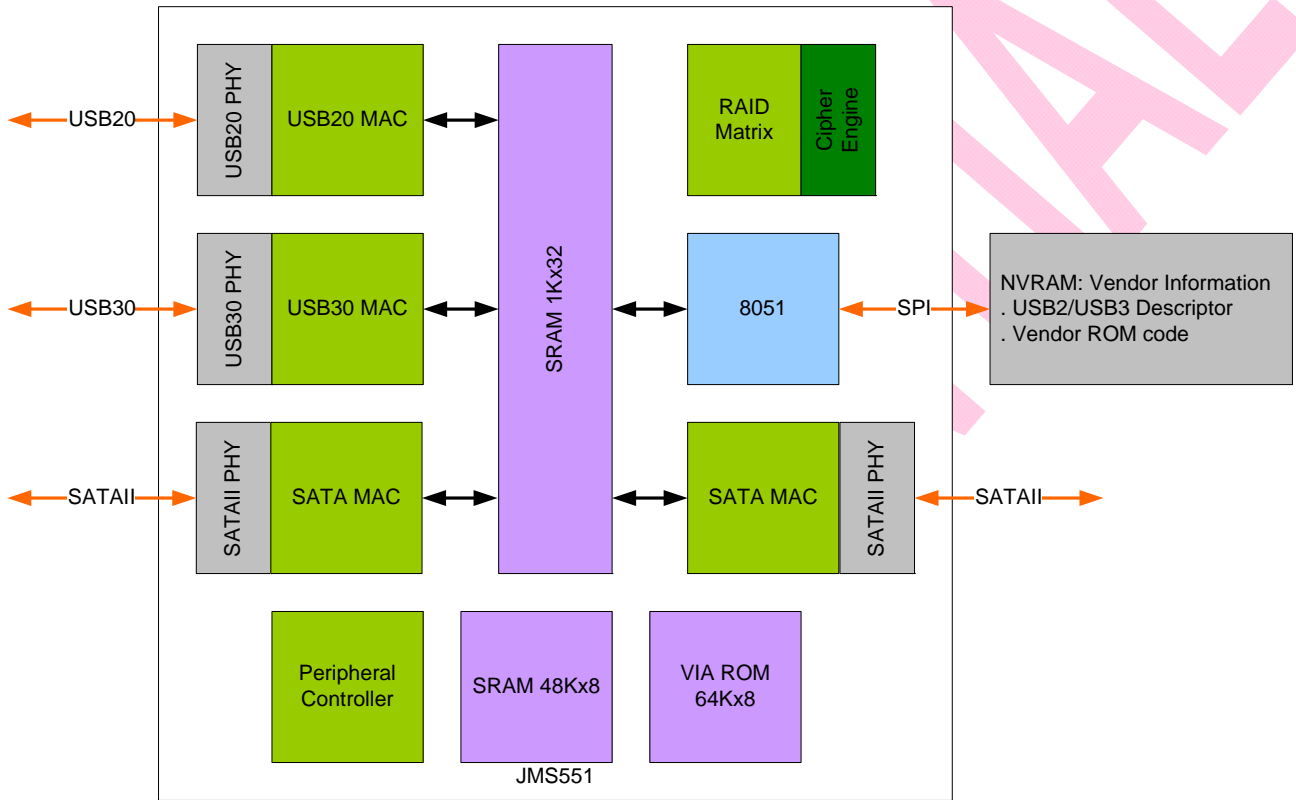
1.2 PACKAGE DIMENSION

1.2.1   100 LQFP 14x14mm^2

DETAIL A

WITH PLATING

BASE METAL
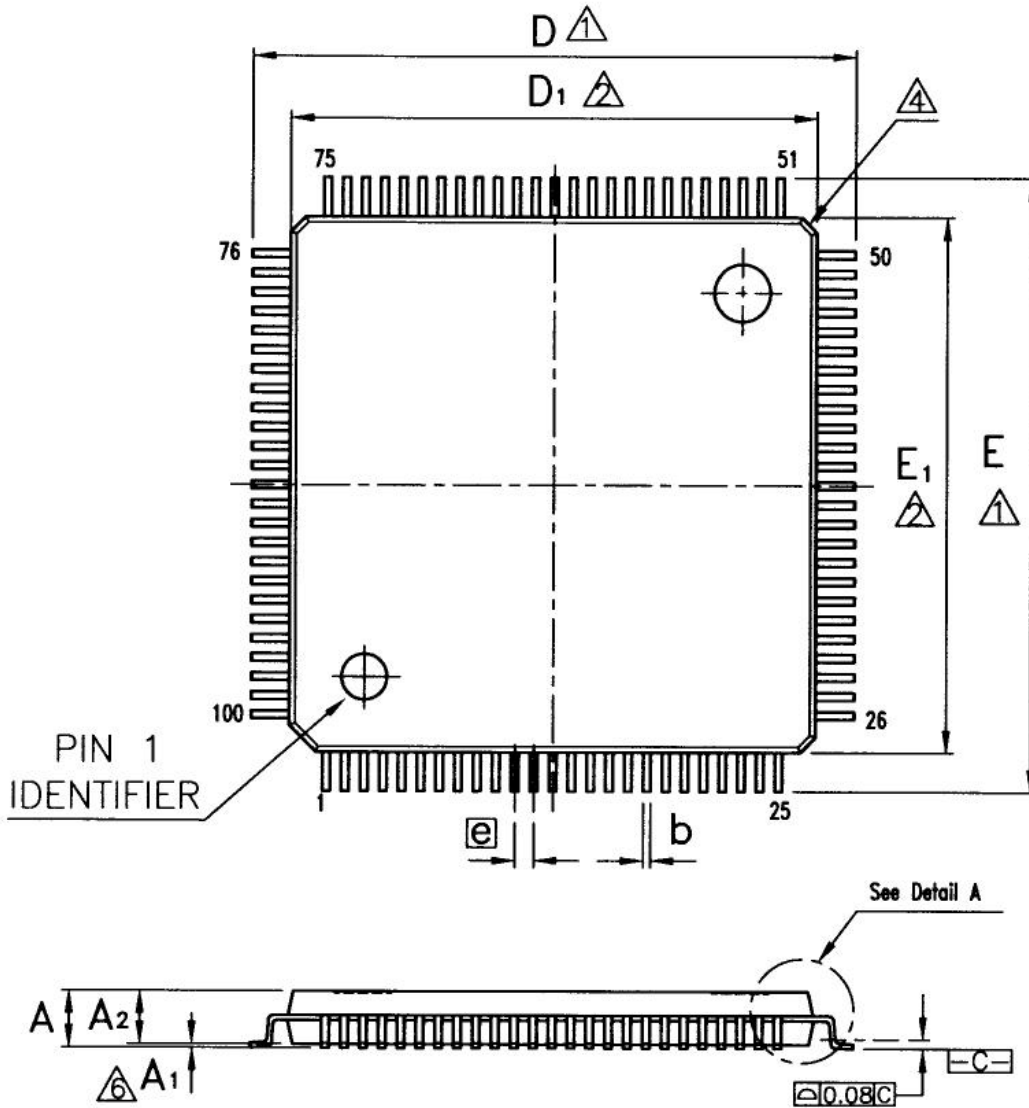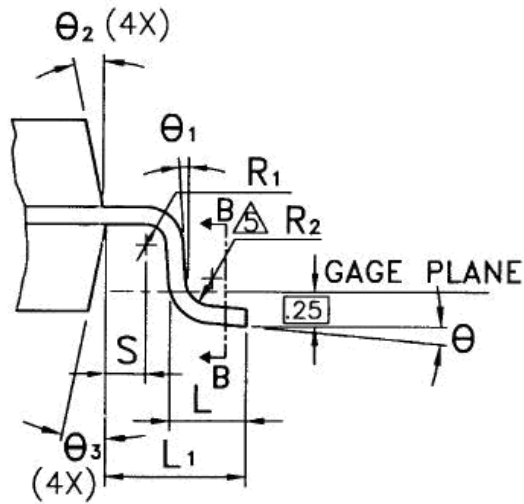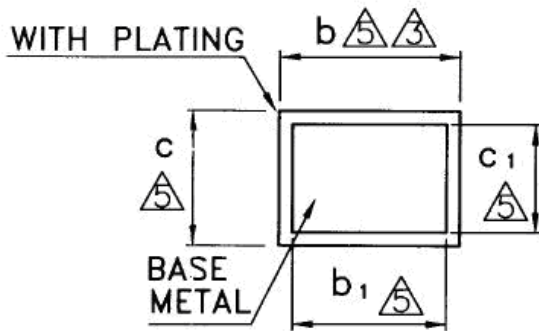
SECTION B-B

Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.60
A_1	0.05	—	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
b_1	0.17	0.20	0.23
c	0.09	—	0.20
c_1	0.09	—	0.16
D	15.85	16.00	16.15
D_1	13.90	14.00	14.10
E	15.85	16.00	16.15
E_1	13.90	14.00	14.10
e	0.50 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	—	—
R_2	0.08	—	0.20
S	0.20	—	—
Θ	0°	3.5°	7°
Θ_1	0°	—	—
Θ_2	12°TYP		
Θ_3	12°TYP		

1.3 SUPPORT DEVICES

- Hard disk drivers

- Optical disk drivers

- Removable media devices

1.4 APPLICATION EXAMPLES

1.4.1 USB2.0, USB3.0, eSATA combo to SATA bridge
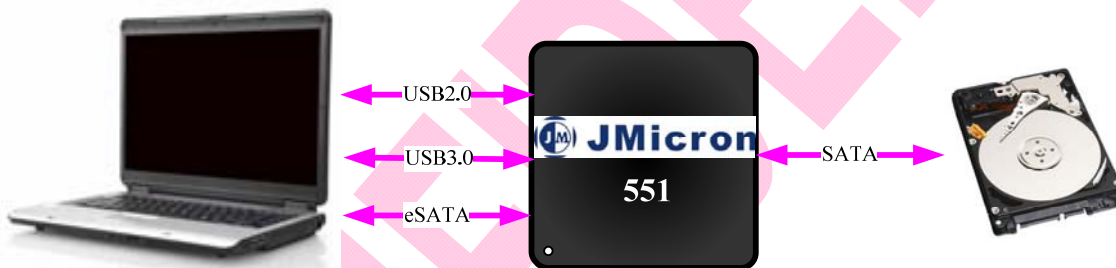
An example of one SATA application is illustrated.

1.4.2 USB2.0, USB3.0 to Dual SATAs bridge
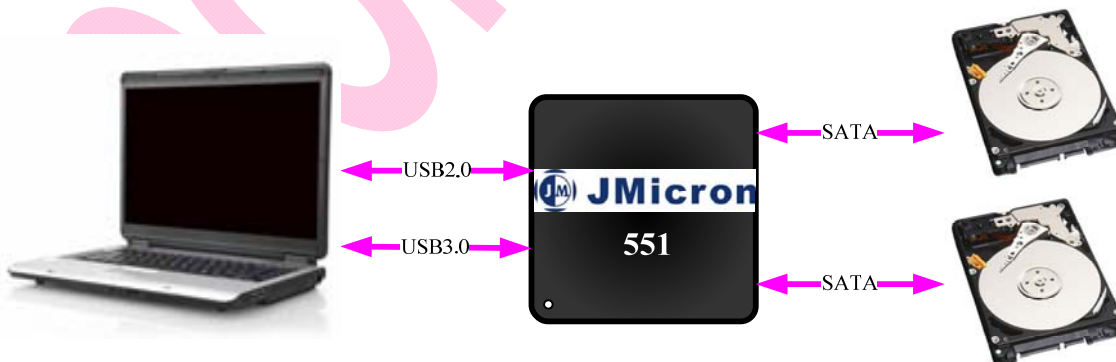
RAID0 and RAID1 functions are available in this example.

1.4.3 Adapt to IDE Hard Disk
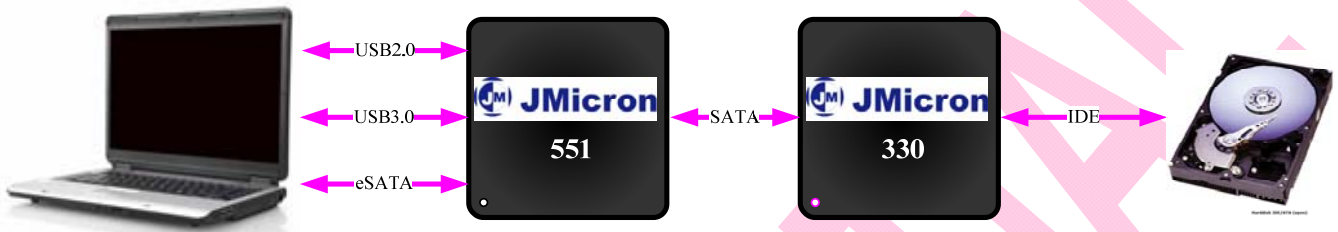
JMicron 330 is recommended to adapt to IDE HDD.

1.4.4 Adapt to Port Multiplier
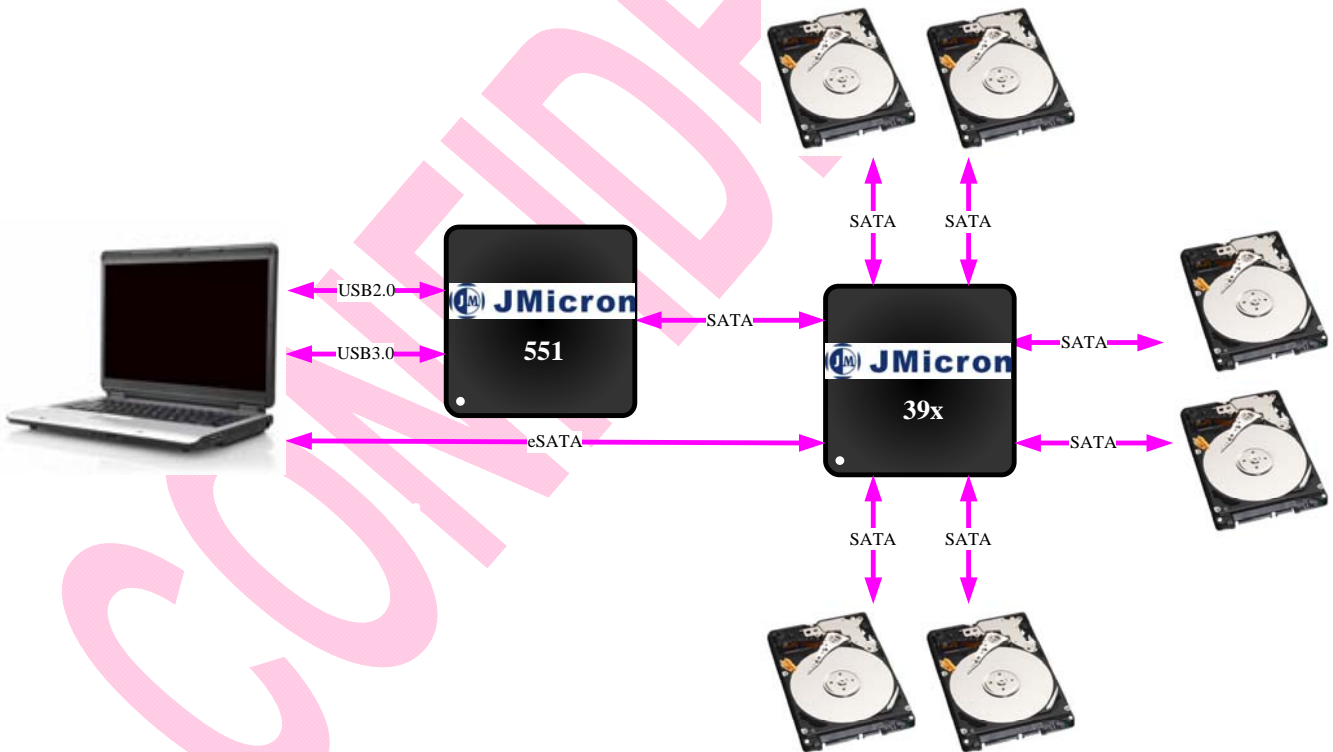
JMicron 39x provides RAID and Port Multiplier function. User can use it for RAID box production application.

2. Package Pin-Out

2.1 Package Pin-Out

2.1.1 100 LQFP

VCCO: 3.3V
VCCK: 1.2V
AVDDH: 3.3V
AVDDL: 1.2V
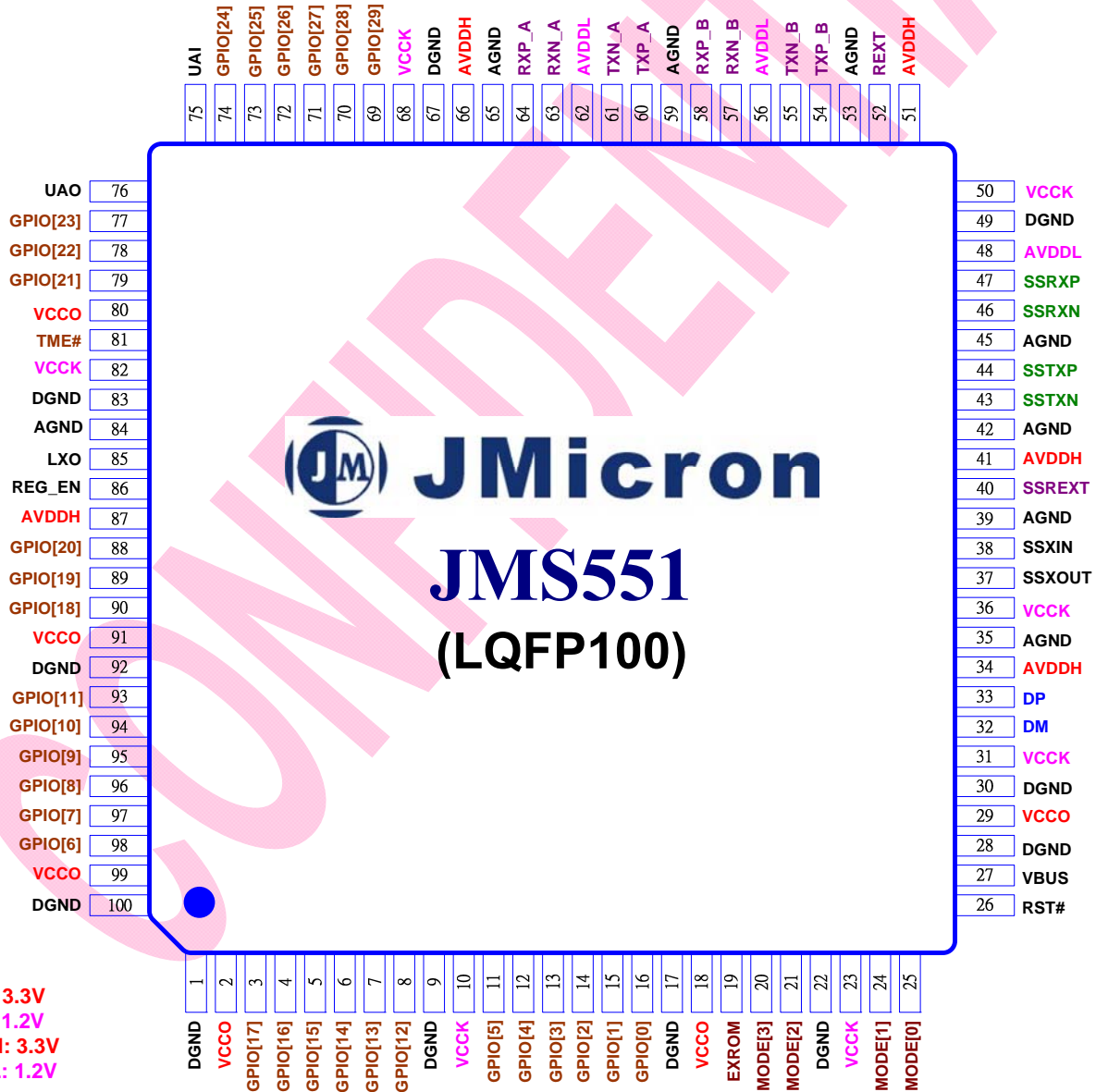
2.2 PIN TYPE DEFINITION

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
L	Internal weak pull-low (Max. 78KΩ, Typical 49 KΩ, Min. 34KΩ)
H	Internal weak pull-high (Max. 66KΩ, Typical 49 KΩ, Min. 39KΩ)

2.3 SERIAL ATA INTERFACE (16 PINs)

Signal Name	Pin No.	Type	Description
RXP_A	64	AI	**Serial ATA PortA RX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
RXN_A	63	AI	**Serial ATA PortA RX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXP_A	60	AO	**Serial ATA PortA TX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXN_A	61	AO	**Serial ATA PortA TX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
RXP_B	58	AI	**Serial ATA PortB RX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
RXN_B	57	AI	**Serial ATA PortB RX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXP_B	54	AO	**Serial ATA PortB TX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXN_B	55	AO	**Serial ATA PortB TX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
AGND	53, 59, 65	AI	**SATA Analog Ground.**
AVDDH	51, 66	AI	**SATA Analog 3.3V Power Supply.**
AVDDL	56, 62	AI	**SATA Analog 1.2V Power Supply.**
REXT	52	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.

2.4   USB3.0 INTERFACE (10 PINs)

Signal Name	Pin No.	Type	Description
SSRXP	47	AI	**Super Speed RX+ signal.** A 470nF CAP should be connected between this pin and USB connector.
SSRXN	46	AI	**Super Speed RX- signal.** A 470nF CAP should be connected between this pin and USB connector.
SSTXP	44	AO	**Super Speed TX+ signal.** A 100nF CAP should be connected between this pin and USB connector.
SSTXN	43	AO	**Super Speed TX- signal.** A 100nF CAP should be connected between this pin and USB connector.
SSREXT	40	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.
AVDDH	41	AI	**USB3.0Analog 3.3V Power Supply.**
AVDDL	48	AI	**USB3.0 Analog 1.2V Power Supply.**
AGND	39, 42, 45	AI	**USB3.0 Analog Ground.**

2.5 USB2.0 INTERFACE (5 PINs)

Signal Name	Pin No.	Type	Description
DM	32	AIO	**USB2.0 Bus D- Signal.**
DP	33	AIO	**USB2.0 Bus D+ Signal.**
VBUS	27	DIL	**USB2.0/3.0 Cable Power Detector.** The 4.7KΩ and 10KΩ resistances should be connected to divide the 5V cable power into 3.3V.
AVDDH	34	AI	**USB2.0 Analog 3.3V Power Supply.**
AGND	35	AI	**USB Analog Ground.**

2.6 CRYSTAL INTERFACE (2 PINs)

Signal Name	Pin No.	Type	Description
SSXIN	38	AI	**Crystal Input/Oscillator Input.** It is connected to a 25MHz crystal or crystal oscillator.
SSXOUT	37	AO	**Crystal Output.** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved as No Connection (NC).

2.7 VOLTAGE REGULATOR (4 PINs)

Signal Name	Pin No.	Type	Description
REG_EN	86	AI	**Voltage Regulator Enable** 1: Enable; 0: Disable
AVDDH	87	AI	**Voltage Regulator 3.3V Power Supply**
AGND	84	AI	**Voltage Regulator Ground**

Signal Name	Pin No.	Type	Description
LXO	85	AO	**Voltage Regulator 1.2V Output**

2.8   DIGITAL POWER AND SYSTEM CONTROL INTERFACE (63 PINs)

Signal Name	Pin No.	Type	Description
VCCO	2, 18, 29, 80, 91, 99	DI	**3.3V I/O Power Supply.**
VCCK	10, 23, 31, 36, 50, 68, 82	DI	**1.2V Core Power Supply.**
DGND	1, 9, 17, 22, 28, 30, 49, 67, 83, 92, 100	DI	**Digital Ground.**
RST#	26	DIH	**System Global Reset Input.** Active-low to reset the entire chip. An external RC should be connected to this pin. Refer to 6.4.1 for detailed description.
TME#	81	DIH	**MP Test Mode Enable.** This pin is reserved for IC mass production testing. Keep this pin to logic "1" in normal operation. Refer to 6.4.1 for detailed description.
MODE[3:0]	20, 21, 24, 25	DIL	**Chip Operation Mode Selection.** [3]: Test mode enable (reserve), must pull to low in normal mode. [2:0]: 000, USB3.0/USB2.0 to 2 SATA [2:0]: 001, USB3.0/USB2.0 to 2 SATA (JBOD) [2:0]: 010, USB3.0/USB2.0 to 2 SATA (RAID 0) [2:0]: 011, USB3.0/USB2.0 to 2 SATA (RAID 1) [2:0]: 100, eSATA /USB3.0/USB2.0 to 1 SATA others: reserve
EXROM	19	DIL	**External Firmware Selection.** 1:External firmware enable 0:External firmware disable
UAI	75	DIH	**8051 UART interface**
UAO	76	DO	**8051 UART interface**

GPIO[0]	16	DIOH	**ATA/ATAPI Power Down Mode Enable/ Serial Flash(SO)/GPIO[0]**
			(1) At Power on MCU will detect this pin.
			  0: Enable MCU issue spin down command to HDD in suspend mode.
			  1: Disable MCU issue spin down command to HDD in suspend mode.
			(2) After power on status detecting, this pin becomes Data Output of serial flash. This pin is default set to input.
			(3) While Serial Flash detection is complete, this pin is default set to input, and could act as GPIO pin by SCSI-2 vender command (button input).

Signal Name	Pin No.	Type	Description
GPIO[1]	15	DIOH	**Serial Flash(SI)/ GPIO[1]** (1) Serial Flash Data Input (SI) of serial flash. This pin is default set to output. (2) While Serial Flash detection is complete, this pin is default set to input, and could act as GPIO pin by SCSI-2 vender command.
GPIO[2]	14	DIOH	**USB Attach Sequence/ Serial Flash(SCK)/ GPIO[2]** (1) This pin is Serial Flash Data Clock (SCK) of serial flash. This pin is default set to output. (2) While Serial Flash detection is complete, this pin is default set to input, and could act as GPIO pin by SCSI-2 vender command.
GPIO[3]	13	DIOH	**Serial Flash(CE#)/ GPIO[3]** (1) This pin functions as Chip Enable (CE#) of Serial Flash (2) While Serial Flash detection is complete, this pin is default set to input, and could act as GPIO pin by SCSI-2 vender command.
GPIO[4]	12	DIO	**2Tera Byte Control** When input high indicates maximum size is 2 tera bytes. When input low, indicates over 2 tera is supported.
GPIO[5]	11	DIO	**USB2.0/3.0 Indicator (high active)** This pin will go high while the USB3.0 attached. It will go low only in USB2.0 is attached or USB is not attached.
GPIO[6]	98	DIO	**GPIO** Can be configured by customer firmware. Don't connect to VCC or Ground directly.
GPIO[7]	97	DIOL	**USB Active** This pin will go high while the USB2.0/3.0 V_{BUS} is applied. It will go low only in V_{BUS} is attached and USB is configured and enter suspend state.
GPIO[8]	96	DIO	**PWM 0 / GPIO[8]** (1) PWM 0 output. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**
GPIO[9]	95	DIO	**PWM 1 / GPIO[9]** (1) PWM 1 output. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**
GPIO[10]	94	DIO	**PWM 2 / GPIO[10]** (1) PWM 2 output. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**
GPIO[11]	93	DIO	**PWM 3 / GPIO[11]** (1) PWM 3 output. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**

Signal Name	Pin No.	Type	Description
GPIO[12]	8	DIO	**Indictor LED(HDD access)** (1) Indictor LED output for HDD access. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**
GPIO[13]	7	DIO	**PWM / GPIO[13]** (1) PWM 5 output. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**
GPIO[14]	6	DIO	**PWM / GPIO[14]** (1) PWM 6 output. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**
GPIO[15]	5	DIO	**PWM / GPIO[15]** (1) PWM 7 output. (2) Can be configured by customer firmware. Don't connect to VCC or Ground directly. **OUTPUT mode is recommended.**
GPIO[23:16]	77, 78, 79, 88, 89, 90, 4, 3	DIO	**General purposes I/O** Can be configured by customer firmware. Don't connect to VCC or Ground directly.
GPIO[29:24]	69, 70, 71, 72, 73, 74	DIO	**General purposes I/O** Can be configured by customer firmware. Don't connect to VCC or Ground directly.

LED Indicator

By default, GPIO[5] is used as USB2.0/USB3.0 active indicator. And GPIO[12] is used as HDD access indicator. The function of GPIO[5] is always ON/OFF and the function of GPIO[12] is fading. If user has different application for LED function, please contact JMicron's AE before PCB layout.

3. External SPI Flash

3.1 EXTERNAL FLASH PROM/EPROM

Vendor Name	Model Name	Comment
PMC	Pm25LV512	
	Pm25LV010	
	Pm25LV020	
SST	SST25VF512	
ST	STM25P10	
	STM25P05	
ATMEL	AT25F1024	
MXIC	MX25L512MC	
Winbond	W25X10	
AMIC	A25L10P	
	A25L20P	
EON	EN25P05	
	EN25P10	

4. Clock & Reset

4.1 Crystal input

Single crystal input (25MHz) is needed.

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Parameter	Symbol	Condition	Min	Max	Unit
Digital 3.3V power supply	VCCO$_{(ABS)}$		-0.3	4.0	V
Digital 1.2V power supply	VCCK$_{(ABS)}$		-0.3	1.44	V
Analog 3.3V power supply	AVDDH$_{(ABS)}$		-0.3	4.0	V
Analog 1.2V power supply	AVDDL$_{(ABS)}$		-0.3	1.44	V
Digital I/O input voltage	V$_{I(D)}$		-0.3	4.0	V
Storage Temperature	T$_{STORAGE}$		-40	150	^{o}C

5.2 Recommended Power Supply Operation Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO		2.97	3.3	3.63	V
Digital 1.2V power supply	VCCK		1.08	1.2	1.32	V
Analog 3.3V power supply	AVDDH		2.97	3.3	3.63	V
Analog 1.2V power supply	AVDDL		1.08	1.2	1.32	V
Digital I/O input voltage	V$_{I(D)}$		0	3.3	3.63	V
Ambient operation temperature	T$_{A}$		0		70	^{o}C
Junction Temperature	T$_{J}$		-40		125	^{o}C

5.3 Recommended External Clock Source Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				25		MHz
Clock Duty Cycle			45	50	55	%

5.4 Power Supply DC Characteristics

5.4.1 Power On Sequence

The Power-On sequence rules is defined in this section. Designers should follow all the rules for external power designs. Detail explanations are listed as below.
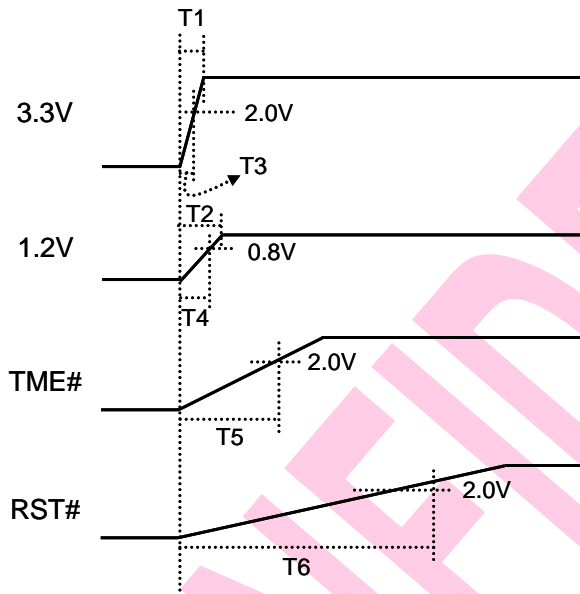
1. T1 : Rise time for 3.3V power rail from 0.0V to 3.3V
2. T2 : Rise time for 1.2V power rail from 0.0V to 1.2V
3. T3 : Rise time for 3.3V power rail from 0.0V to 2.0V
4. T4 : Rise time for 1.2V power rail from 0.0V to 0.8V
5. T5 : Rise time for TME# signal from 0.0V to 2.0V
6. T6 : Rise time for RST# signal from 0.0V to 2.0V

The recommended power sequence and timing requirements are listed as below.

Time	Minimum	Maximum
T1	0.0 ms	1.0 ms
T2	0.0 ms	2.5 ms
T3	0.0 ms	0.67 ms
T4	0.0 ms	1.67 ms
T5	5.0 ms	5.5 ms
T6	12 ms	40 ms

5.4.2 USB2.0 to SATA RAID 0/1 mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO		2	10	20	mA
Digital 1.2V power supply	VCCK		75	85	100	mA
Analog 3.3V power supply	AVDDH		55	75	100	mA
Analog 1.2V power supply	AVDDL		70	90	100	mA

5.4.3 USB3.0 to SATA RAID 0/1 mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO		2	10	16	mA
Digital 1.2V power supply	VCCK		120	135	150	mA
Analog 3.3V power supply	AVDDH		80	95	110	mA
Analog 1.2V power supply	AVDDL		150	190	240	mA

5.5 I/O DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.0			V
Output low voltage	V_{OL}				0.4	V
Output high voltage	V_{IH}		2.4			V

6. Performance Benchmark

6.1 ATTO Disk Benchmark
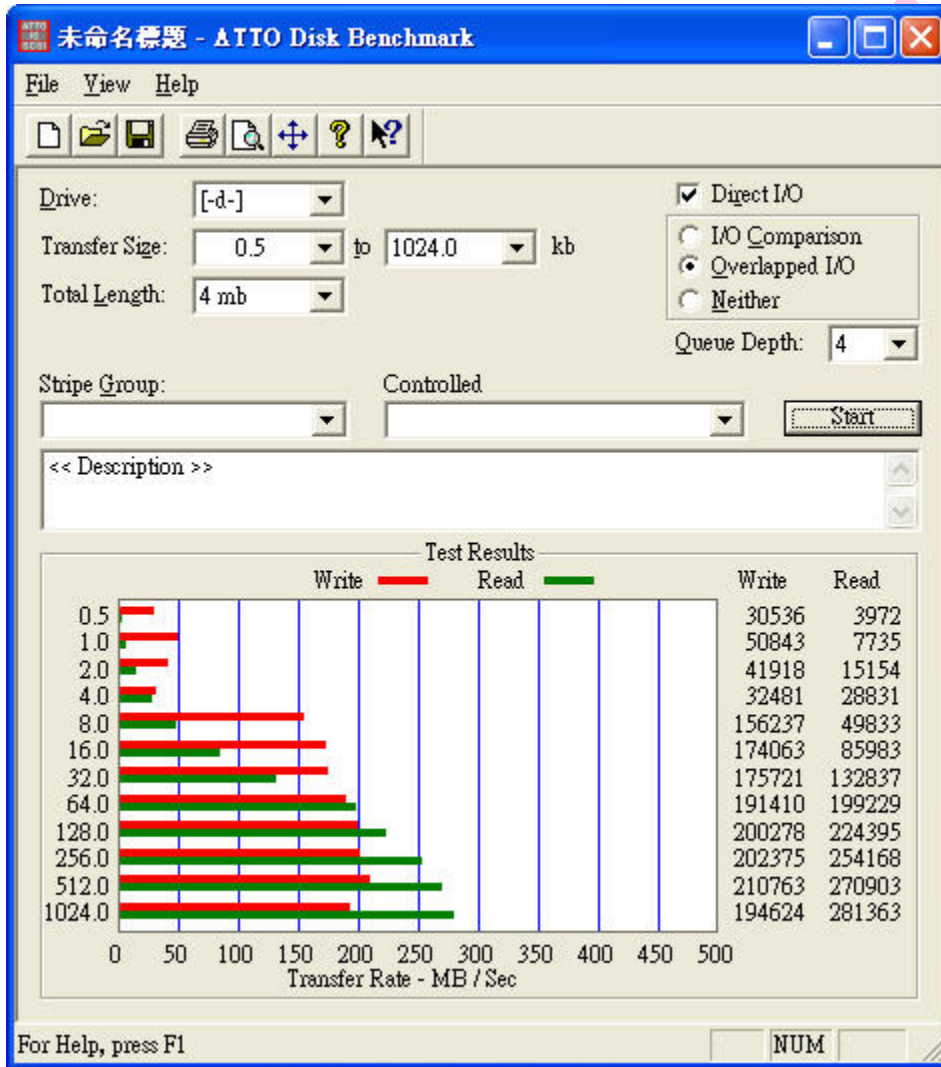
6.2 HDBench Disk Benchmark