JMS561

SuperSpeed USB to Dual SATA Gen3 Ports Bridge

Preliminary Datasheet

Revision 1.0.1

Revision History

Version	Date yyyy/mm/dd	Revision Description
1.0.1	2014/04/20	1. Correct 1.1.1 typo 2. Correct “XIN” description 3. Correct “XOUT” description 4. Correct “VREG-IN” description 5. Correct “FB” description 6. Correct Reset Timing
1.0.0	2013/10/31	Release revision 1.0.0

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http://www.JMicron.com or send email to sales@jmicron.com

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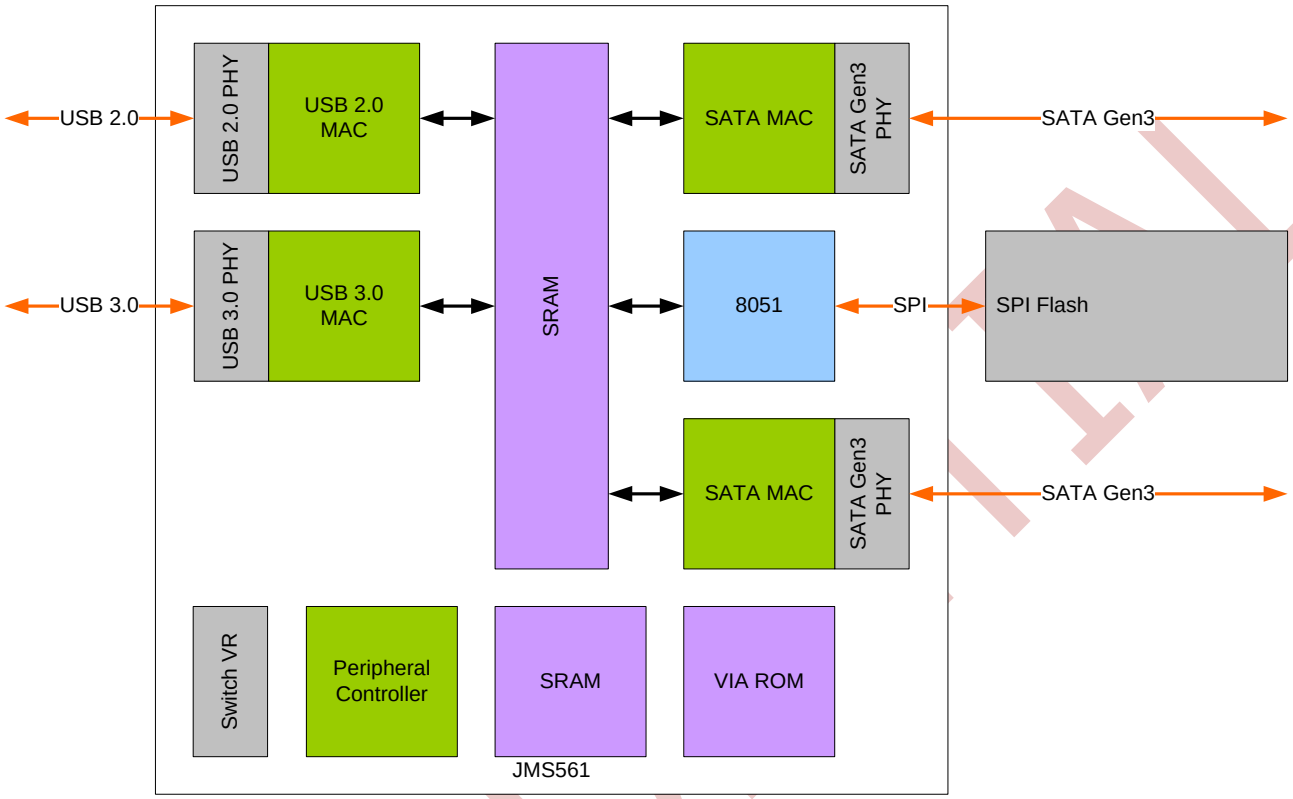
1. Overviews

1.1 FUNCTION OVERVIEW

1.1.1 FEATURES

- Complies with Serial ATA International Organization: Serial ATA Revision 3.1
- Complies with Universal Serial Bus 3.0 Specification Revision 1.0
- Complies with USB Mass Storage Class Bulk-Only Transport (BOT) Rev. 1.0 Specification
- Complies with USB Attached SCSI Protocol (UASP) Rev. 1.0 Specification
- Supports USB Super-Speed/High-Speed/Full-Speed Operation
- Supports USB 2.0/USB 3.0 power saving mode
- Supports multi LUNs for USB 2.0/USB 3.0
- Supports port multiplier for eSATA
- Supports hardware RAID0 (striping) and RAID1 (mirror) over USB 2.0/USB 3.0/eSATA
- Flexible GPIOs for customized functions
- Provides a hardware control PWM
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB3.0/eSATA
- Design for Windows XP, Windows 7, Windows 8, MAC 10.3 or later versions
- 30MHz external crystal
- An embedded 3.3V to 1.2V voltage regulator
- An embedded 5.0V to 3.3V voltage regulator
- QFN 64 package

1.1.2 BLOCK DIAGRAM

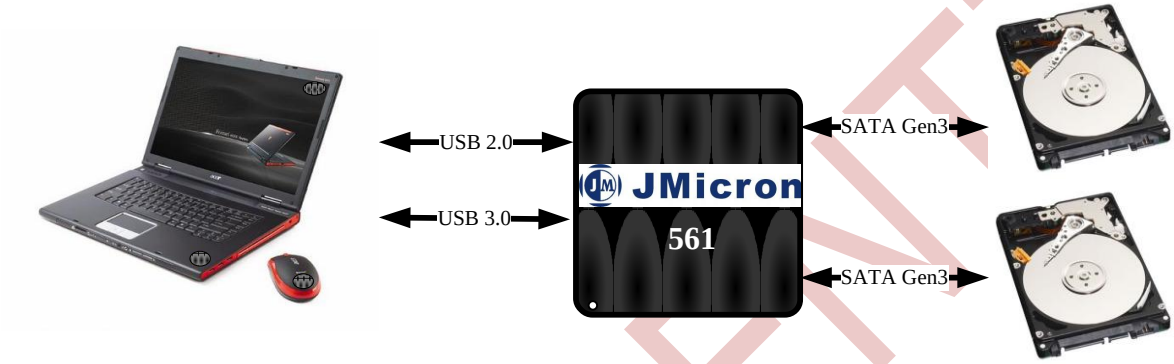


1.2 SUPPORT DEVICES

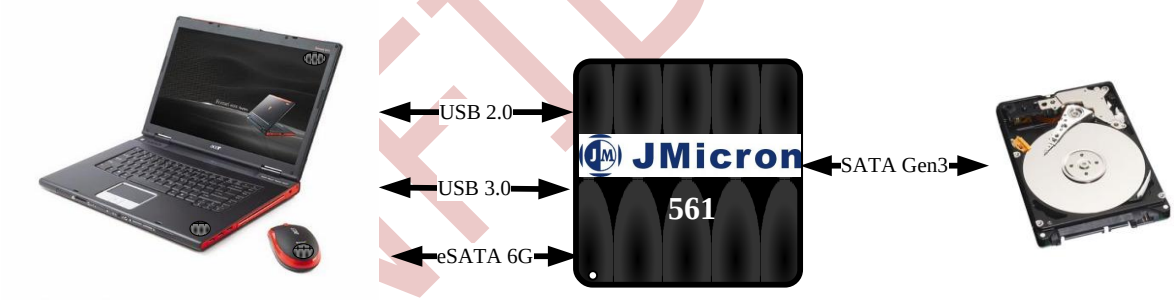
- Hard disk drives

1.3 APPLICATION EXAMPLES

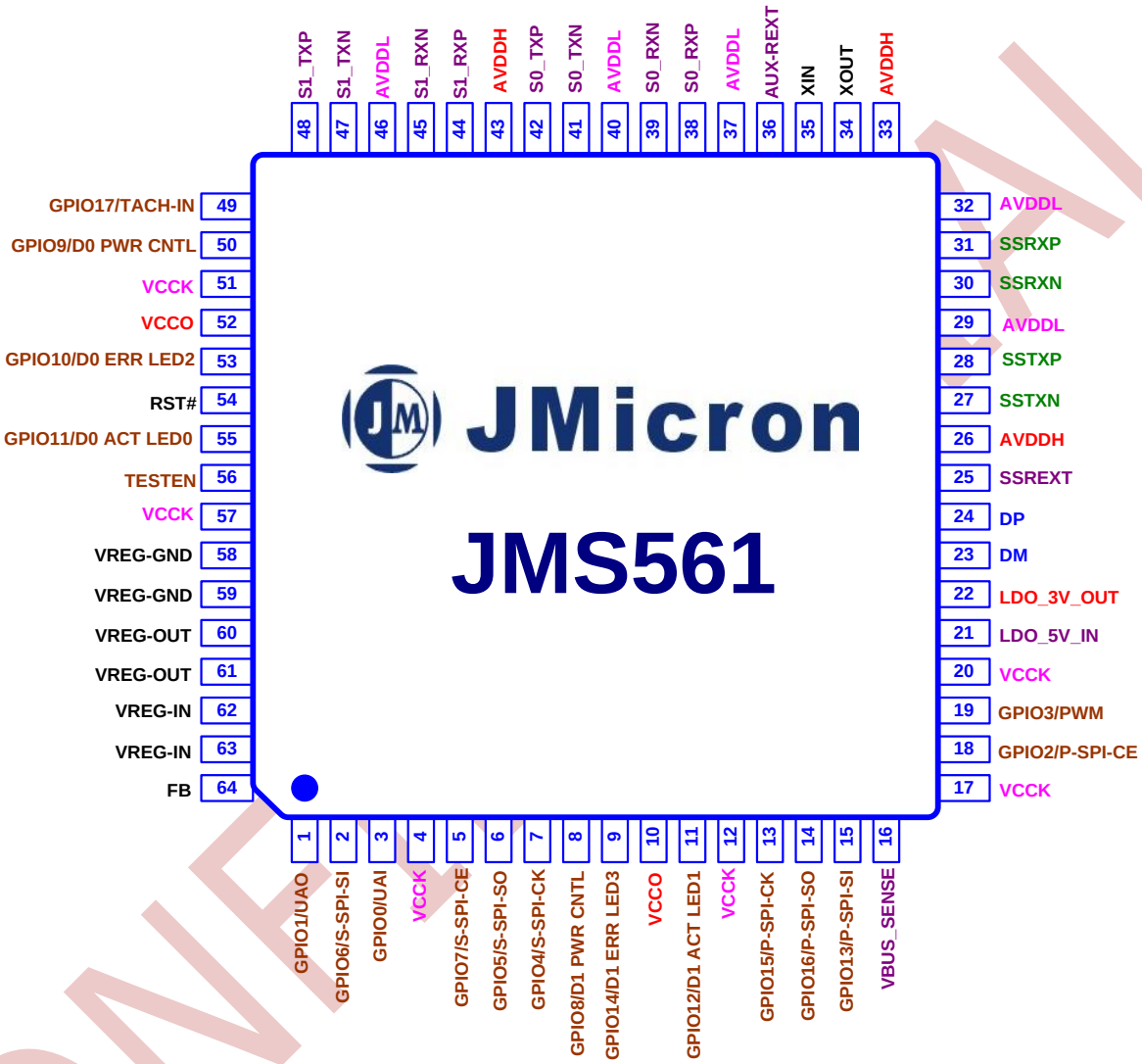
1.3.1 USB 2.0 and USB 3.0 to two SATA Gen3 HDDs



1.3.2 USB 2.0, USB 3.0 and eSATA 6G to one SATA Gen3 HDD



2. Package Pin-Out



2.1 PIN TYPE DEFINITION

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
S	Internal Schmitt Trigger Circuit is used
L	Internal weak pull-low (Max. 164KΩ, Typical 96 KΩ, Min. 61KΩ)
H	Internal weak pull-high (Max. 141KΩ, Typical 93 KΩ, Min. 66KΩ)

2.2 PIN DESCRIPTION

Signal Name	QFN 64	Type	Description
Serial ATA interface			
S0_RXP	38	AI	**SATA Port RX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S0_RXN	39	AI	**SATA Port RX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S0_TXP	42	AO	**SATA Port TX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S0_TXN	41	AO	**SATA Port TX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S1_RXP	44	AI	**SATA Port RX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S1_RXN	45	AI	**SATA Port RX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S1_TXP	48	AO	**SATA Port TX+ Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
S1_TXN	47	AO	**SATA Port TX- Signal.** A 10nF capacitor should be connected between this pin and SATA connector.
REXT	36	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.
USB 3.0 interface			

Signal Name	QFN 64	Type	Description
SSRXP	31	AI	**Super Speed RX+ Signal.**
SSRXN	30	AI	**Super Speed RX- Signal.**
SSTXP	28	AO	**Super Speed TX+ Signal.** A 100nF capacitor should be connected between this pin and USB connector.
SSTXN	27	AO	**Super Speed TX- Signal.** A 100nF capacitor should be connected between this pin and USB connector.
SSREXT	25	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.
USB 2.0 interface			
DM	23	AIO	**USB 2.0 Bus D- Signal.**
DP	24	AIO	**USB 2.0 Bus D+ Signal.**
LDO_5V_IN	21	AI	**5.0V to 3.3V LDO Power Input.** This pin should be connected to the 5V input or USB connector 5V.
LDO_3V_ OUT	22	AO	**Capacitance for internal LDO of USB 2.0.** A capacitance to ground is recommended on this pin. The value should be 1uF. The output voltage range is 3.3V±10%.
VBUS_ SENSE	16	AI	**USB 2.0/USB 3.0 Cable Power Input** This pin should be connected to USB connector 5V.
Crystal Interface			
XIN	35	AI	**Crystal Input/Oscillator Input.** It is connected to a 30MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage should range in 3.3V±5%.
XOUT	34	AO	**Crystal Output.** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved as No Connection (NC). The output variation range is around ±30ppm (input dependent). And the output voltage range is 3.3V±5% (input dependent).
Switching Regulator			
VREG-GND	58,59	AI	**Switching Regulator Ground.**
VREG-OUT	60,61	AO	**Switch Output Pin.** An external inductor should be connected to this pin.
VREG-IN	62,63	AI	**Switching Regulator 3.3V Power Supply.**
FB	64	AI	**Feedback pin which is connected to 1.2V core voltage.**

Signal Name	QFN 64	Type	Description
Control and GPIOs			
RST#	54	DIS	**System Global Reset Input.** Active-low to reset the entire chip. An external RC should be connected to this pin. Please refer to the following section for detailed description.
TESTEN	56	DIS	**MP Test Mode Enable.** This pin is reserved for IC mass production testing. Please set this pin to low under normal operation.
GPIO[0]	3	DIOH	**8051 UART Output / GPIO [0].** This pin only preserves for UART TX function.
GPIO[1]	1	DIOH	**8051 UART Input / GPIO [1].** This pin only preserves for UART RX function.
GPIO[2]	18	DIOH	**Primary Serial Flash (CE) / GPIO [2]** This pin only preserves for SPI chip enable.
GPIO[3]	19	DIOH	**GPIO [3].** This pin only preserves for FAN function.
GPIO[4]	7	DIOH	**Secondary Serial Flash (SCK) / GPIO [4]** This pin can be programmed as special function or normal GPIO function.
GPIO[5]	6	DIOH	**Secondary Serial Flash (SO) / GPIO [5]** This pin can be programmed as special function or normal GPIO function.
GPIO[6]	2	DIOH	**Secondary Serial Flash (SI) / GPIO [6]** This pin only preserves for UART function.
GPIO[7]	5	DIOH	**Secondary Serial Flash (CE) / GPIO [7]** This pin can be programmed as special function or normal GPIO function.
GPIO[8]	8	DIOH	**GPIO [8].** This pin only preserves for enable hard drive power.
GPIO[9]	50	DIOH	**GPIO [9].** This pin only preserves for enable hard drive power.
GPIO[10]	53	DIOH	**GPIO [10].** This pin can be programmed by customized firmware.
GPIO[11]	55	DIOH	**GPIO [11].** This pin can be programmed by customized firmware.
GPIO[12]	11	DIOH	**GPIO [12].** This pin can be programmed by customized firmware.
GPIO[13]	15	DIOH	**Primary Serial Flash (SI) / GPIO [13]** This pin can be programmed as special function or normal GPIO function.
GPIO[14]	9	DIOH	**GPIO [14].** This pin can be programmed by customized firmware.

Signal Name	QFN 64	Type	Description
GPIO[15]	13	DIOH	**Primary Serial Flash (SCK) / GPIO [15]** This pin can be programmed as special function or normal GPIO function.
GPIO[16]	14	DIOH	**Primary Serial Flash (SO) / GPIO [16]** This pin can be programmed as special function or normal GPIO function.
GPIO[17]	49	DIOH	**GPIO [17].** This pin only preserves for FAN TACH In function.
Power and Ground			
VCCO	10,52	P	Digital I/O Power Supply.
VCCK	4,12,17 20,51,57	P	Digital Core Power Supply.
AVDDH	26,33,43	P	Analog I/O Power Supply.
AVDDL	29,32,37 40,46	P	Analog Core Power Supply.

LED Indicator

If user has an application for LED function, please contact JMicron's AE before PCB layout.

GPIO initial value

All GPIOs set as input mode with pull-high resistor while in reset.

3. External SPI Flash

Vendor Name	Model Name	Comment
MXIC	25L400 1E	
MXIC	25L4005 AMC	
MXIC	25L1605 DM2I	
MXIC	25L8005 MC	
MXIC	25L4006E	
MXIC	25L8006E	
MXIC	25L8035E	
AMIC	A25L040M-F	
AMIC	A25L016M-F	
AMIC	A25L032M-F	
Winbond	W25X40BLSNIG	
Winbond	25X40CLNIG	
Winbond	25Q80BLNIG	
Winbond	25X40CLVIG	
Giga Device	25Q40T	
vpowerwins	FM25F04	
ESMT	F25L04PAG1SM	

4. Clock & Reset

4.1 Crystal input

Single crystal input at 30MHz is needed.

4.2 Reset input

The reset input pin is the Schmitt trigger input pin. All functions will be initialized by reset except the Analog Power-On Reset Circuit depending on the Power on-off.

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Parameter	Symbol	Condition	Min	Max	Unit
Digital I/O power supply	$VCCO_{(ABS)}$		-0.3	3.47	V
Digital core power supply	$VCCK_{(ABS)}$		-0.3	1.26	V
Analog I/O power supply	$AVDDH_{(ABS)}$		-0.3	3.47	V
Analog core power supply	$AVDDL_{(ABS)}$		-0.3	1.26	V
USB VBUS power supply	VBUS		-0.3	5.5	V
Digital I/O input voltage	$V_{I(D)}$		-0.3	3.47	V
Storage Temperature	$T_{STORAGE}$		-40	150	^oC

5.2 Recommended Power Supply Operation Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital I/O power supply	VCCO		3.13	3.3	3.47	V
Digital core power supply	VCCK		1.14	1.2	1.26	V
Analog I/O power supply	AVDDH		3.13	3.3	3.47	V
Analog core power supply	AVDDL		1.14	1.2	1.26	V
Digital I/O input voltage	$V_{I(D)}$		0	3.3	3.47	V
Ambient operation temperature	T_A		0		70	^oC
Junction Temperature	T_J		-40		125	^oC

5.3 Recommended External Clock Source Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				30		MHz
Clock Duty Cycle			45	50	55	%

5.4 Power Supply DC Characteristics

The maximum and minimum values are measured at the max and min power supply levels respectively.

5.4.1 USB2.0 to SATAx2 mode

@S0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V power supply	VCCO and ACDDH	Operate @3.3V	40.5	48.6	56.0	mA
1.2V power supply	VCCK and AVDDL	Operate @1.2V	325.4	328.3	332.4	mA

@S4 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V power supply	VCCO and ACDDH	Operate @3.3V	3.0	3.0	3.0	mA
1.2V power supply	VCCK and AVDDL	Operate @1.2V	4.0	4.0	4.1	mA

5.4.2 USB3.0 to SATAx2 mode

@U0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V power supply	VCCO and ACDDH	Operate @3.3V	45.9	53.9	61.3	mA
1.2V power supply	VCCK and AVDDL	Operate @1.2V	450.6	455.4	477.7	mA

@U3 state (suspend @S4)

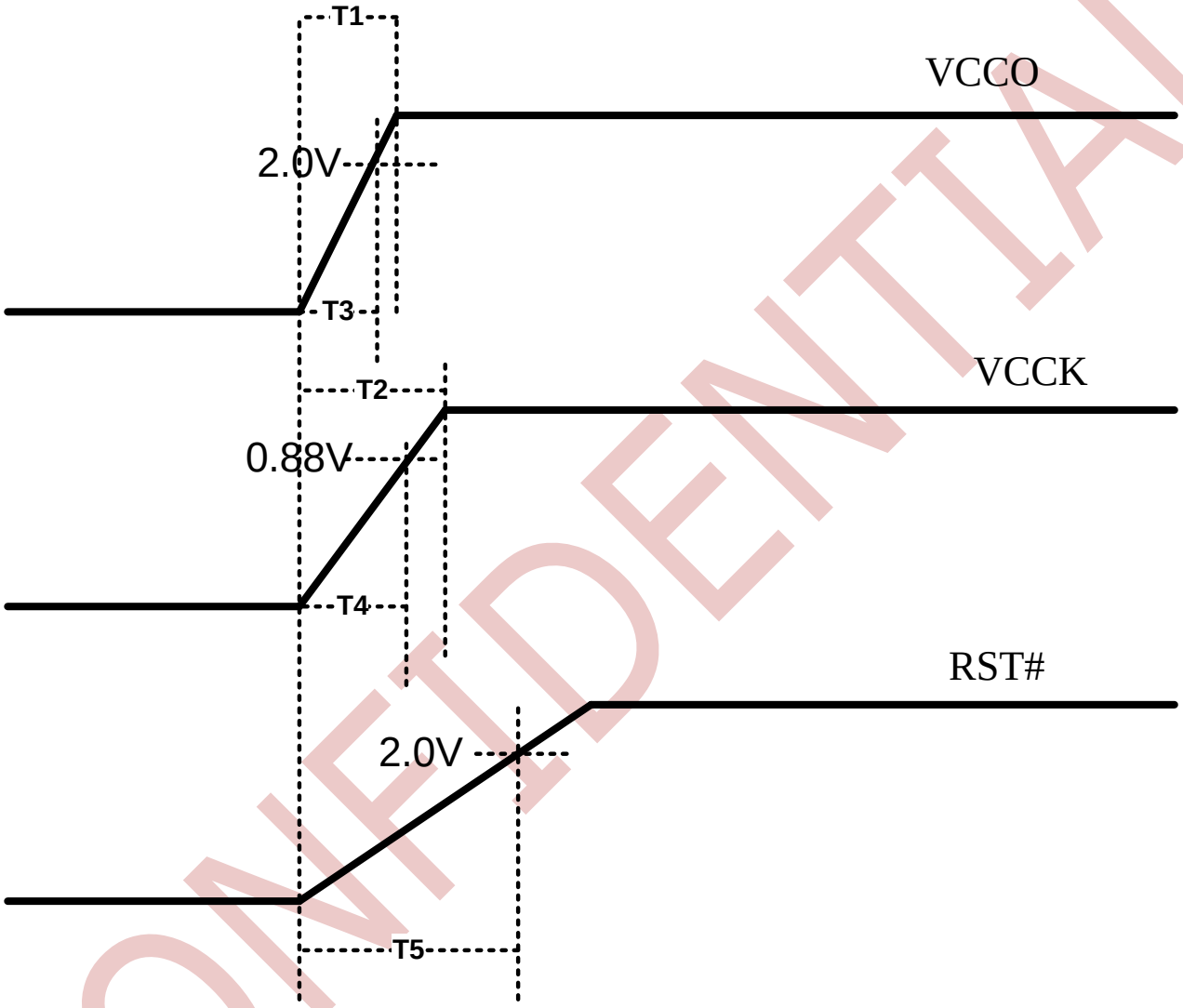
Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V power supply	VCCO and ACDDH	Operate @3.3V	3.0	3.0	3.1	mA
1.2V power supply	VCCK and AVDDL	Operate @1.2V	7.0	7.0	7.1	mA

5.5 I/O DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}				0.7	V
Input high voltage	V_{IH}		1.5			V
Output low voltage	V_{OL}				0.3	V
Output high voltage	V_{OH}		1.9			V

5.6 Power-On Sequence

The Power-On sequence rules are defined in this section. Designers should follow all the rules for external power designs. Detailed explanations are listed as below.



T1: Rise time for 3.3V power rail from 0.0V to 3.3V
T2: Rise time for 1.2V power rail from 0.0V to 1.2V
T3: Rise time for 3.3V power rail from 0.0V to 2.0V
T4: Rise time for 1.2V power rail from 0.0V to 0.88V
T5: Rise time for RST# signal from 0.0V to 2.0V

The recommended power sequence and timing requirements are listed as below.

Time	Minimum	Maximum
T1	0.0 ms	10 ms
T2	0.0 ms	10 ms
T3	0.0 ms	8 ms
T4	0.0 ms	8 ms
T5	100 ms	500 ms

The RESET timing constrain is based on the external RC reset circuits. In order to control the charge and discharge time for RC circuits, minimum and maximum requirements are listed. If designers apply timing control chip to control the reset signal, the only requirement will be minimum value. In other words, the maximum value can be skipped without problems.

6. Internal Switch Regulator

Input Voltage Range: 2.375V ~ 5.500V
Output Voltage Range: 1.0V ~ 1.4 (programmable)
Output Voltage Accuracy : I_{LOAD}= 650mA, V_{OUT}±10%
Max. Output Current : 650mA
Over-Current Protection (OCP): Yes (1,500mA)
Output Capacitor: 20uF
Output Inductor: 3.3uH
Start-up Time : < 1.5 ms
Thermal Shutdown: No
Faster Shutdown: No

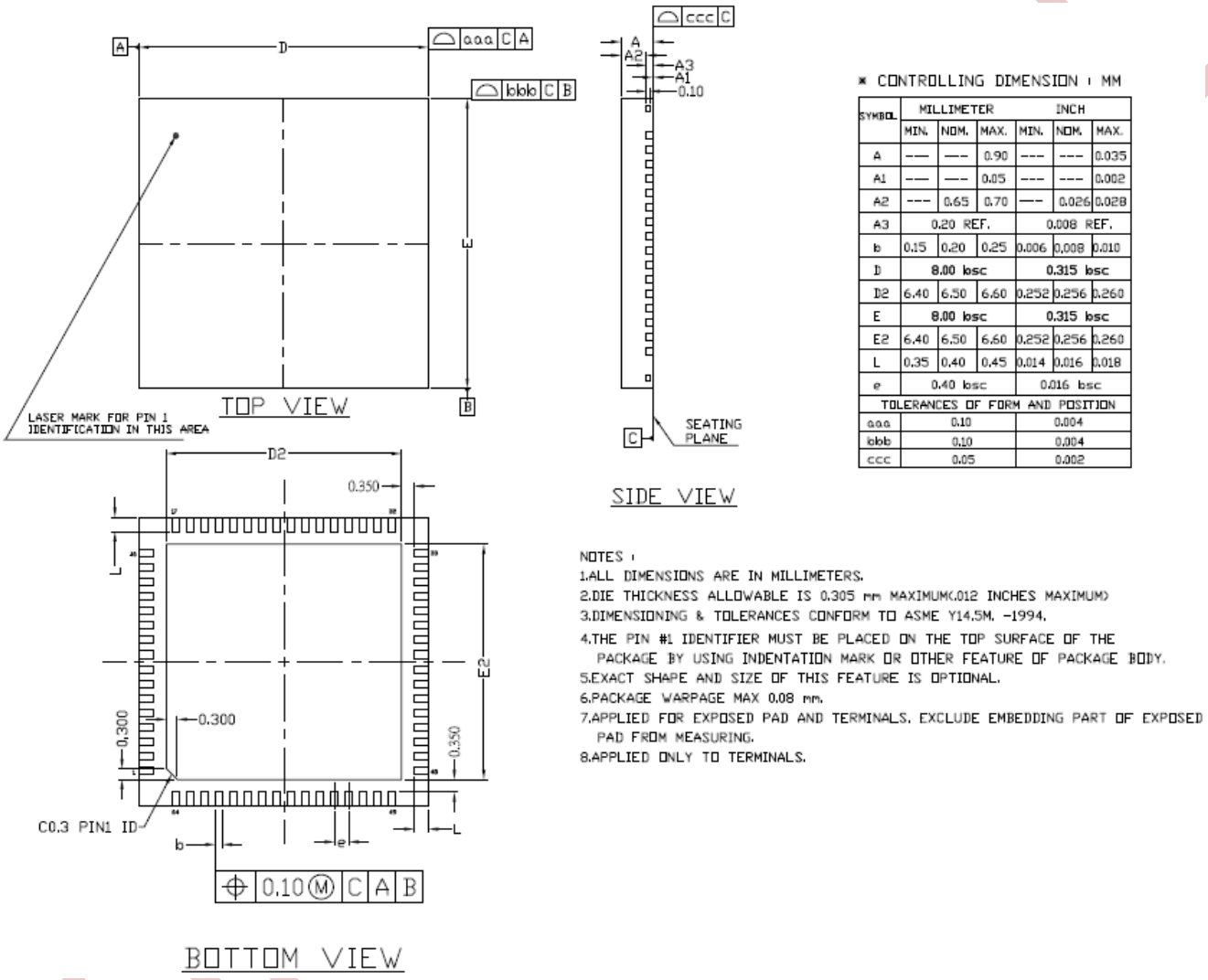
7. Performance Benchmark

USB3.0 UAS Performance 400 MB/s

USB2.0 UAS Performance 42 MB/s

8. Package Dimension

- QFN 64 8x8 mm^2



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	8.00 bsc			0.315 bsc		
D2	6.40	6.50	6.60	0.252	0.256	0.260
E	8.00 bsc			0.315 bsc		
E2	6.40	6.50	6.60	0.252	0.256	0.260
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.