Datasheet

JMS578

SuperSpeed USB 3.0 to SATA 6.0Gb/s Bridge Controller

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Revision History

Version	Date	Revision Description
1.00	1/13/2015	Formal release
1.01	9/2/2016	Removed SPI list and performance benchmark chapter

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1. Overviews

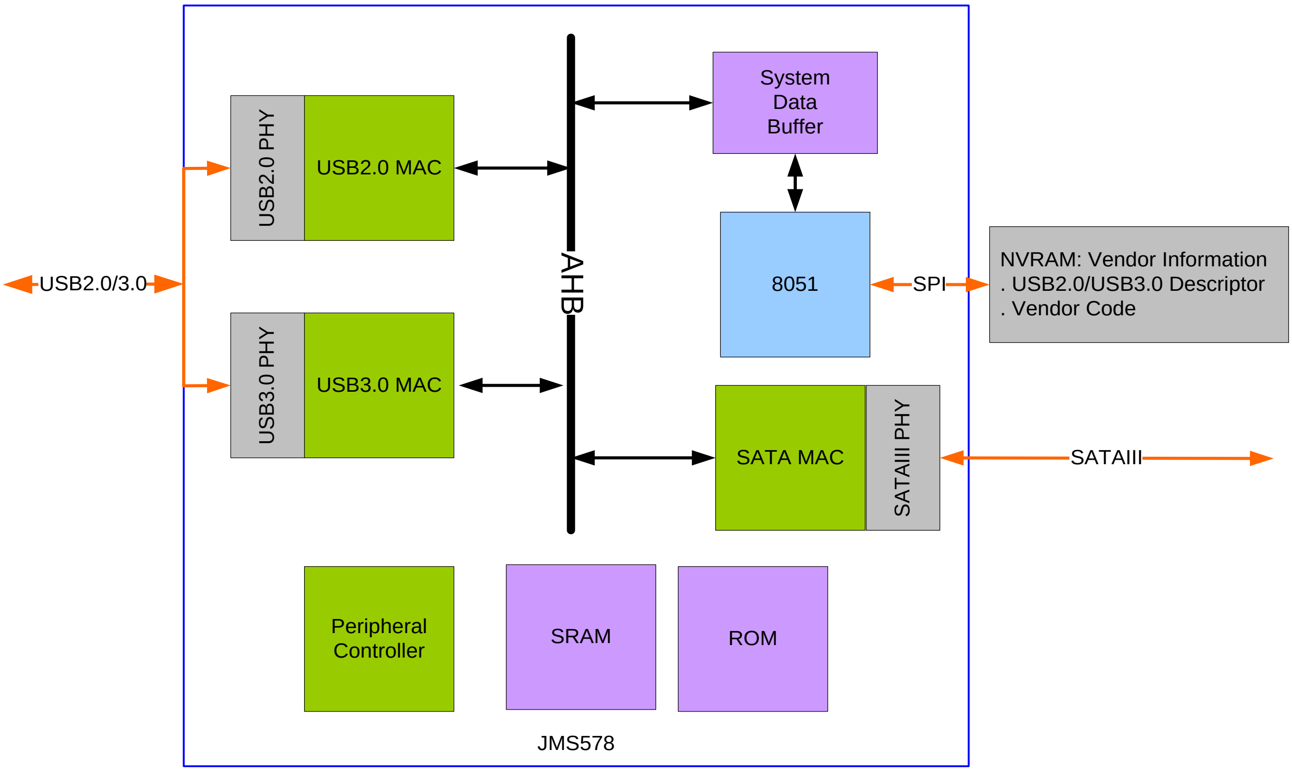
JMS578 is a USB3.0 to SATA III 6Gps bridge controller with high performance and low power consumption. It can support external SPI NVRAM for Vendor VID/PID of USB2.0/USB3.0 device controller. It has 10 GPIOs to do customization for various applications. It supports software utilities for downloading the upgraded firmware code under USB2.0/USB3.0. It complies with both the USB Mass Storage Class Bulk-Only Transport (BOT) Specification and USB Attached SCSI Protocol (UASP) Specification.

1.1 FUNCTION OVERVIEW

1.1.1 FEATURES

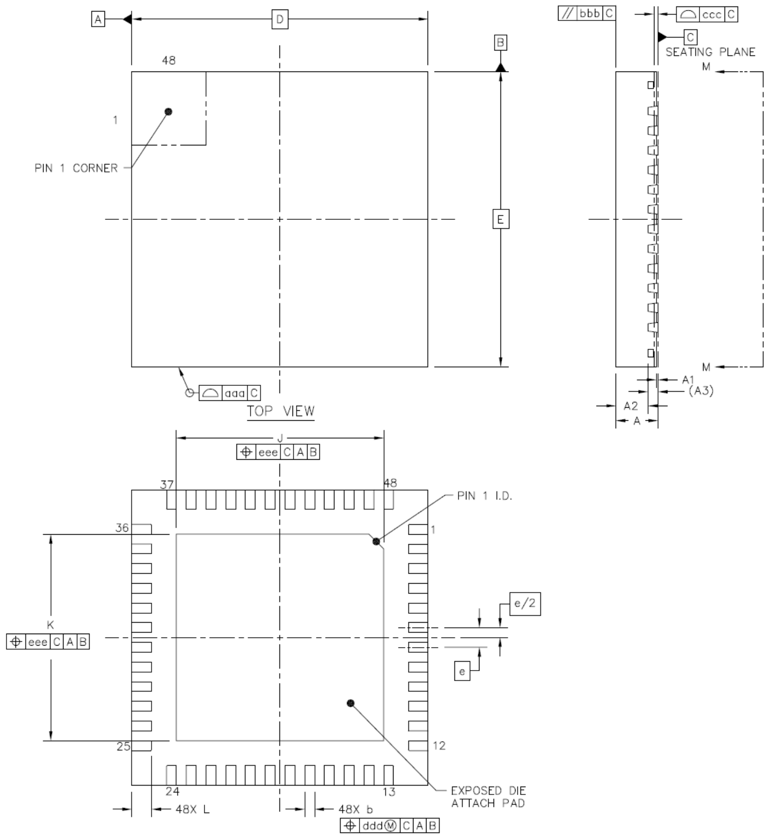
- Complies with Gen2i/Gen2m of Serial ATA II Electrical Specification 2.6
- Complies with Gen3 of Serial ATA III Electrical Specification 3.2
- Complies with USB 3.0 Specification, USB Mass Storage Class, Bulk-Only Transport Specification
- Complies with USB Attached SCSI Protocol (UASP) Specification
- Supports USB Super-Speed/High-Speed/Full-Speed Operation
- Supports USB2.0/USB3.0 power saving mode
- Supports SHA-1/SHA-256 for IEEE-1667 digest calculation
- Supports external SPI NVRAM for Vendor VID/PID of USB2.0/USB3.0 device controller
- Supports ATA/ATAPI PACKET command set
- 10 GPIOs for customization
- Provides hardware control PWM
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB3.0
- Design for Windows 7, Windows 10 and MAC 10.9.5 or later version.
- Supports 30MHz external crystal
- Embedded 5V to 1.2V voltage regulator
- Embedded 5V to 3.3V linear voltage regulator (LDO)
- QFN48 package (6x6)

1.1.2 BLOCK DIAGRAM



1.2 PACKAGE DIMENSION

1.2.1 QFN48 6x6mm^2 (JMS578-QGBA0A)



Unit: mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	6 BSC		
	Y	E	6 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	J	4.1	4.2	4.3
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

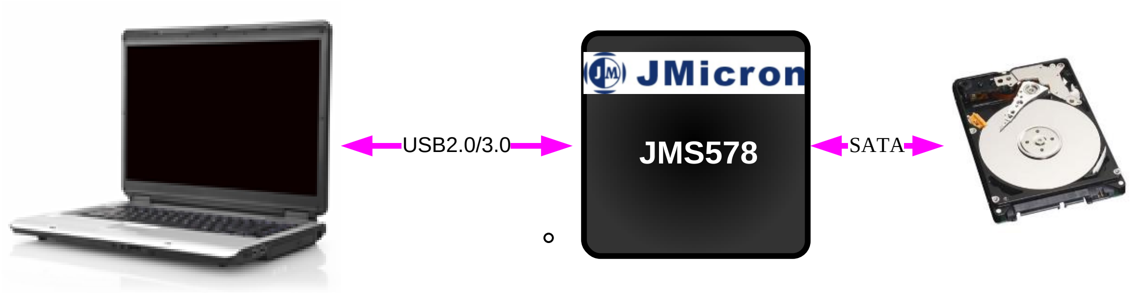
Note: The ground pad size is (J * K)

1.3 SUPPORT DEVICES

- Hard disk drivers
- Removable media devices

1.4 APPLICATION EXAMPLES

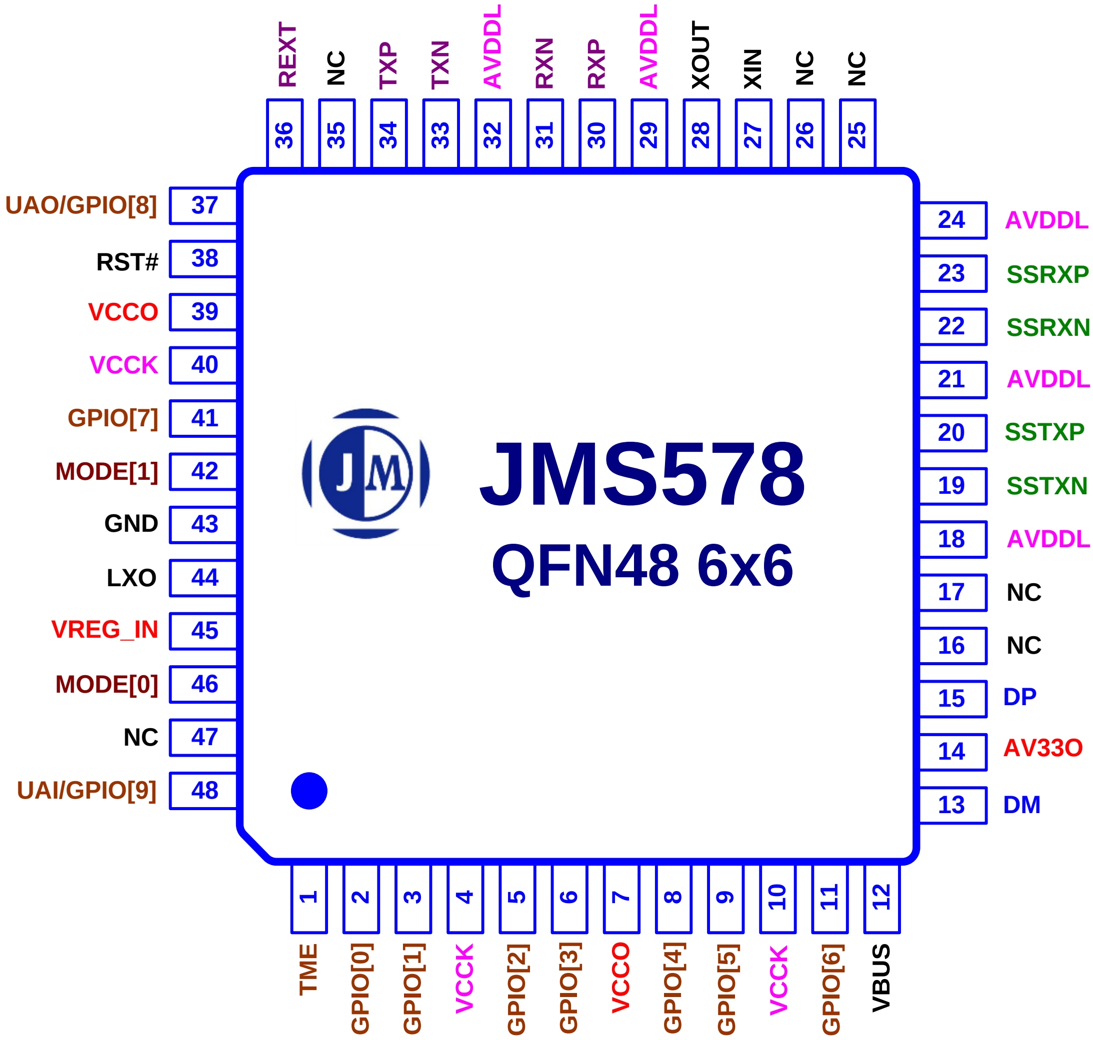
1.4.1 USB2.0, USB3.0 to SATA Bridge



An example of one SATA application is illustrated.

2. Package Pin-Out

2.1 QFN48



2.2 PIN TYPE DEFINITION

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
L	Internal weak pull-low (Max. 164KΩ, Typical 96 KΩ, Min. 61KΩ)
H	Internal weak pull-high (Max. 141KΩ, Typical 93 KΩ, Min. 66KΩ)

2.3 SERIAL ATA INTERFACE

Signal Name	Pin No.	Type	Description
RXP	30	AI	**Serial ATA Port RX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
RXN	31	AI	**Serial ATA Port RX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXP	34	AO	**Serial ATA Port TX+ signal.** A 10nF CAP should be connected between this pin and SATA connector.
TXN	33	AO	**Serial ATA Port TX- signal.** A 10nF CAP should be connected between this pin and SATA connector.
NC	35	AI	**Non Connect** Don't Care on the connectivity
AVDDL	32	AI	**SATA Analog 1.2V Power Supply.**
REXT	36	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.

2.4 USB3.0 INTERFACE

Signal Name	Pin No.	Type	Description
SSRXP	23	AI	**Super Speed RX+ signal.**
SSRXN	22	AI	**Super Speed RX- signal.**
SSTXP	20	AO	**Super Speed TX+ signal.** A 100nF CAP should be connected between this pin and USB connector.
SSTXN	19	AO	**Super Speed TX- signal.** A 100nF CAP should be connected between this pin and USB connector.
NC	16	N/A	**Non Connect** Don't Care on the connectivity

Signal Name	Pin No.	Type	Description
NC	17	N/A	**Non Connect** Don’t Care on the connectivity
AVDDL	18,21,24	AI	**USB3.0 Analog 1.2V Power Supply.**

2.5 USB2.0 INTERFACE

Signal Name	Pin No.	Type	Description
DM	13	AIO	**USB2.0 Bus D- Signal.**
DP	15	AIO	**USB2.0 Bus D+ Signal.**
VBUS	12	AI	**USB2.0/3.0 Cable Power Input.**
AV33O	14	AO	**USB2.0 Analog 3.3V Output.** A capacitance to ground is recommended on this pin. The value should be 1uF. The output voltage range is 3.3V±10%. Note: 1. This PIN provides power less than 100mA @ 3.3V. 2. This pin can afford chip internal power usage only.

2.6 CRYSTAL INTERFACE

Signal Name	Pin No.	Type	Description
XIN	27	AI	**Crystal Input/Oscillator Input.** It is connected to a 30MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage should range in 1.2V±5%.
XOUT	28	AO	**Crystal Output.** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved as No Connection (NC). The output variation range is around ±30ppm (input dependent). And the output voltage range is 1.2V±5% (input dependent).
NC	25	N/A	**Non Connect** Don’t Care on the connectivity
AVDDL	29	AI	**1.2V Analog Power Supply**

2.7 VOLTAGE REGULATOR

Signal Name	Pin No.	Type	Description
VREG_IN	45	AI	**Voltage Regulator Power Supply**
GND	43	AI	**Voltage Regulator Ground**
LXO	44	AO	**Voltage Regulator Output** Switch node. Connect with external power inductor with a value of 4.7uH.

2.8 DIGITAL POWER AND SYSTEM CONTROL INTERFACE

Signal Name	Pin No.	Type	Description
VCCO	7, 39	P	**3.3V I/O Power Supply.**
VCCK	4, 10, 40	P	**1.2V Core Power Supply.**
GND	E-PAD	P	**Ground.**
RST#	38	DI	**System Global Reset Input.** Schmitt trigger input pin. Active-low to reset the entire chip. An external RC should be connected to this pin.
TME	1	DI	**MP Test Mode Enable.** Schmitt trigger input pin. This pin is reserved for IC mass production testing. Keep this pin to logic "0" in normal operation.
MODE[1:0]	42, 46	DIL	**Chip Operation Mode Selection.** Value MODE[1:0] = 2'b01 is recommended in normal operation. For the others, they are using in IC mass production testing.
GPIO[0]	2	DIOH	**Serial Flash (SO)** After power on status detecting, this pin becomes Data Output of serial flash. This pin is by default set to input.
GPIO[1]	3	DIOH	**Serial Flash (SCK)** This pin is Serial Flash Data Clock (SCK) of serial flash. This pin is by default set to output.
GPIO[2]	5	DIOH	**Serial Flash(SI)** Serial Flash Data Input (SI) of serial flash. This pin is by default set to output.
GPIO[3]	6	DIOH	**Serial Flash(CE0#)** This pin functions as Chip Enable (CE0#) of Serial Flash
GPIO[4]	8	DIOH	**GPIO[4]** Can be configured by customer firmware.
GPIO[5]	9	DIOH	**GPIO[5]** Can be configured by customer firmware.
GPIO[6]	11	DIOH	**GPIO[6]** Can be configured by customer firmware.
GPIO[7]	41	DIOH	**GPIO[7]** Can be configured by customer firmware.
UAO/GPIO[8]	37	DIOH	**8051 UART interface/GPIO[8]** Can be configured by customer firmware.
UAI/GPIO[9]	48	DIOH	**8051 UART interface/GPIO[9]** Can be configured by customer firmware.
NC	26, 47	N/A	**Non Connect** Don't Care on the connectivity

LED Indicator

By default, GPIO[4] is used as HDD access indicator. If user has different application for LED function, please contact JMicron's AE before PCB layout.

GPIO initial value

All GPIOs are set as input mode and their internal pull-up function is enabled during reset. After reset, the firmware code programs all of GPIOs as input mode, and then the initial values of GPIOs are read and stored in the system RAM for future usage.

3. Clock & Reset

3.1 Crystal input

Parameter	Symbol	Min	Typical	Max	Unit
Crystal start up time v.s AVDDL	$\mathbf{T}_{Crystal}$			150	mS
Crystal Frequency	f_{clk}		30		MHz
Long term stability (Crystal Only)	$\Delta\mathbf{f}_{MAX\_Crystal}$	-30		30	ppm
Long term stability (On Board)	$\Delta\mathbf{f}_{MAX\_OnBoard}$	-150		150	ppm
Equivalent Series Resistance	**ESR**			55	OHM
Drive Level	**DL**		50		uW

3.2 Reset input

All functions will be initialized by reset except the Analog Power-On Reset Circuit depending on the Power on-off.

The reset input pin is the Schmitt trigger input pin. VT+ Schmitt Trigger Low to High Threshold Point is 1.31V and VT- Schmitt Trigger High to Low Threshold Point is 0.96V.

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Digital 3.3V power supply	$VCCO_{(ABS)}$	-0.3	3.6	V
Digital 1.2V power supply	$VCCK_{(ABS)}$	-0.3	1.32	V
Analog 1.2V power supply	$AVDDL_{(ABS)}$	-0.3	1.32	V
Digital I/O input voltage	$V_{I(D)}$	-0.3	3.6	V
USB VBUS power supply	VBUS	4.0	5.5	V
Storage Temperature	$T_{STORAGE}$	-40	150	^oC

4.2 Recommended Power Supply Operation Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	3.0	3.3	3.6	V
Digital 1.2V power supply	VCCK	1.08	1.2	1.32	V
Analog 1.2V power supply	AVDDL	1.08	1.2	1.32	V
Digital I/O input voltage	$V_{I(D)}$	0	3.3	3.6	V
Ambient operation temperature	T_A	0		70	^oC
Case operation temperature	T_C	0		90	^oC
Junction Temperature	T_J			125	^oC

4.3 Recommended External Clock Source Conditions

Parameter	Symbol	Min	Typical	Max	Unit
External reference clock			30		MHz
Clock Duty Cycle		45	50	55	%

4.4 Power Supply DC Characteristics

4.4.1 Power On (No USB Connected)

USB2.0 PHY, USB3.0 PHY, SATA PHY will be OFF

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.01	0.1	0.3	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	22	26.5	35	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	20	22	30	mA

4.4.2 USB2.0 to SATA mode

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	50	55	65	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	110	117	130	mA

4.4.3 USB3.0 to SATA mode

@U0 state

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	75	82	90	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	160	175	185	mA

@U3 state (suspend @S4)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.5	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	1	2	4	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	2	3	6	mA

@U1/U2 state (No pending commands, SATA OFF, USB2 OFF)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO	Operate @3.3V	0.1	0.2	0.3	mA
Digital 1.2V power supply	VCCK	Operate @1.2V	19	24	29	mA
Analog 1.2V power supply	AVDDL	Operate @1.2V	15	20	25	mA

4.5 I/O DC Characteristics

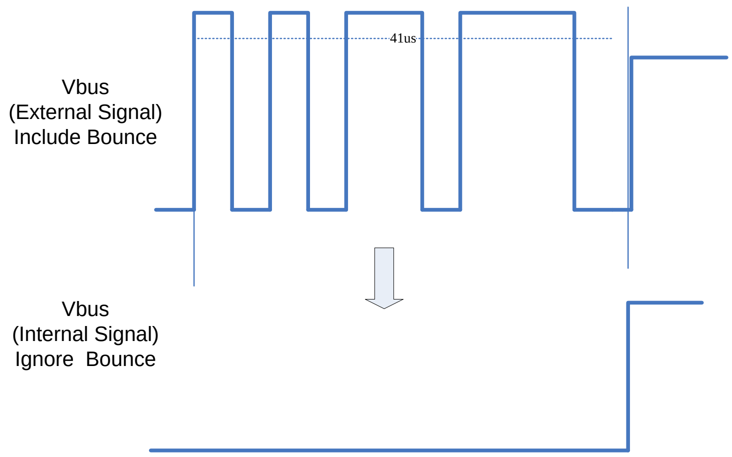
Parameter	Symbol	Min	Typical	Max	Unit
Input low voltage	V_{IL}			0.7	V
Input high voltage	V_{IH}	1.5			V
Output low voltage	V_{OL}			0.3	V
Output high voltage	V_{OH}	1.9			V
Output Current	I_O		10	12	mA

4.6 VBus Detector

There are two parts for VBUS de-bounce by VBUS (Pin 12). One is hysteresis and the other one is logic glitch filter.

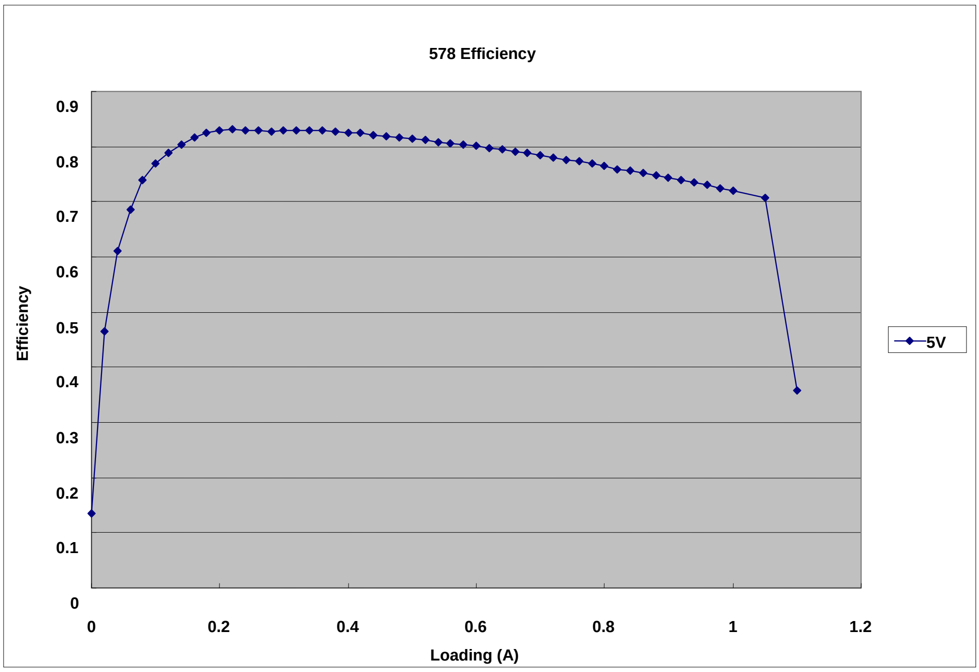
Hysteresis: switching threshold is 2.45V for high to low
switching threshold is 3.08V for low to high

And a 41us logical glitch filter is also implemented for VBUS de-bounce. If the logic high level is maintained for more than 41 us, the period will be treated as a HIGH period. Otherwise, the period will be LOW. The sample rate of VBUS is 100MH and checked status per 12 ms.



4.7 Switching Power efficiency (VREG_IN)

Efficiency = $Vout \times Iout / Vin \times Iin$, *Vin = 5V, Vout = 1.2V*



4.8 Internal Linear Regulator

Parameter	Symbol	Min	Typical	Max	Unit
Input Voltage Range	V_{IN_LINEAR}	4	5	5.5	V
Output Voltage Range	V_{OUT_LINEAR}	3.10	3.3	3.45	V
Max Output Current	I_{MAX}	-	-	100	mA

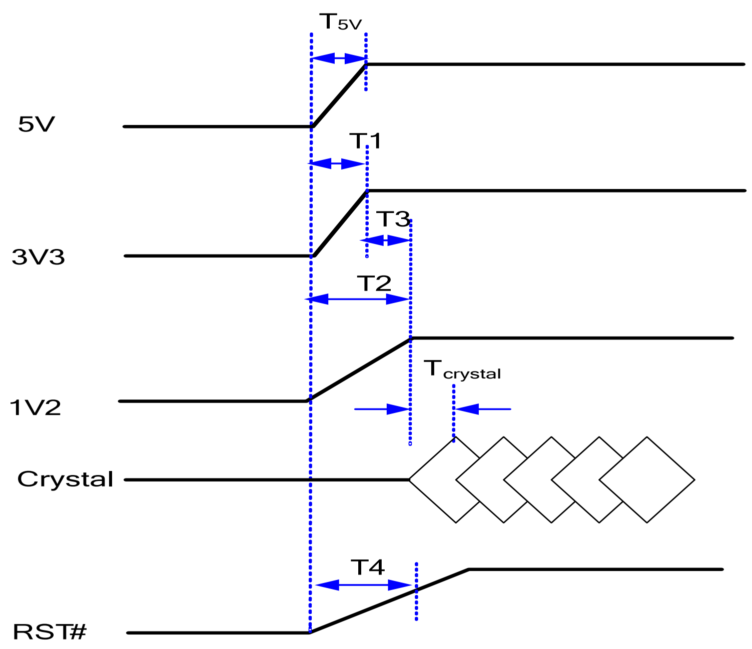
4.9 Power Ripple

Parameter	Symbol	Condition	Min	Typical	Max	Unit
5V Power Supply [1]	P_{5V}	Operate @ USB3.0	-	80	150	mV
3.3V Power Supply [2]	P_{3V3}	Operate @ USB3.0	-	80	150	mV
1.2V Power Supply [3]	P_{1V2}	Operate @ USB3.0	-	80	100	mV

Note: 1. Test point near Vbus capacitor.
2. Test point at LDO output capacitor.
3. Test point at AVDDL bypass capacitor.

4.10 Power-On Sequence

The Power-On sequence rules are defined in this section. Designers should follow all the rules for external power designs. Detailed explanations are listed as below.



T_{5V}: Rise time for 5V power rail from 10% to 90%
T1: Rise time for 3V3 power rail from 10% to 90%
T2: Rise time for 1V2 power rail from 10% to 90%

T3: Time interval between 3.3V power and 1.2V Power

T4: Rise time for RST# signal from 0.0V to 2.2V

$T_{Crystal:}$ Time interval between 1.2V and 90% clock swing

Note: Clock must meet 30MHz +/-30ppm in the mean time

The recommended power sequence and timing requirements are listed as below.

Time	Minimum	Maximum
T_{5V}	-	20 ms
T1	0.0 ms	10 ms
T2	0.0 ms	10 ms
T3	-10 ms	10 ms
T4	100 ms	500 ms
Tcrystal	-	150.0 ms

The RESET timing constrain is based on the external RC reset circuits. In order to control the charge and discharge time for RC circuits, minimum and maximum requirements are listed. If designers apply timing control chip to control the reset signal, the only requirement will be minimum value. In other words, the maximum value can be skipped without problems.

5. Internal Switch Regulator

Input Voltage Range: 2.25V ~ 5.50V
Output Voltage Range: 1.05V ~ 1.32V (programmable)
Output Voltage Accuracy : I_{LOAD}= 700 mA, V_{OUT}±10%
Max. Output Current : 700 mA
Over-Current Protection (OCP): Yes (1,500mA)
Input Capacitor: 10uF
Output Capacitor: 10uF ~ 20uF
Output Inductor: 4.7uH
Start-up Time : < 500us
Thermal Shutdown: No
Faster Shutdown: No

5.1 PCB layout guidelines :

1. Route high speed switching node LXO away from sensitive analog area (as crystal, REXT … etc)
2. Connect input/output capacitors to power and ground plane and put input/output capacitors close to IC and keep the high-current paths as short and wide as possible.

6. Product Naming

QFN48 6X6 mm^2

JM S 578 – Q G B A0 A

Device revision number

Revision number of ROM code

Bonding type (6X6 48 Pin)

Green product with the operation ambient temperature ranged from 0°C to 70°C

Package type - QFN

Serial number

Product category – USB SuperSpeed

Provider name - JMicron