JMicron Technology Corporation

DATASHEET

JMS583
USB 3.1 Gen 2 to PCIe Gen3x2 Bridge

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Revision History

Revision Number	Effective Date	Description of Revision		Author
		Reference	Description of the Change	
0.1	11/9/2017	-	Draft release	Joe Chang
0.2	4/12/2018	Table 1 Table 9 Section 5.4	1. Modify the internal weak pull-high resistor (Max. 59k, Typical 38k, Min. 27k). 2. Add XAVDDH signal description. 3. GPIO[4] is used as LED indicator by default.	Joe Chang
0.3	6/6/2018	Figure 2 Chapter 6 Chapter 7	1. Package outline drawing of QFN64 8x8 2. Update crystal electrical and reset voltage 3. Update electrical characteristics	Joe Chang
1.0	6/30/2018	Chapter 2 Table 13	1. Support SCSI / NVMe Pass-through command. 2. Change the typical value of 1.0V power supply.	Joe Chang

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1 Introduction

The JMS583 is a bridge controller between the USB host and the storage devices with PCIe/NVMe interface. Its upstream port provides a USB which data speed can reach up to ten gigabits per second (10 Gb/s), or the data transmission rate for USB 3.1 Gen 2 specification. Meanwhile, its downstream port can connect to PCIe/NVMe storage devices, such as a solid-state drive (SSD). The data speed for the PCIe port can arrive at 16 Gb/s, or the data rate for the PCIe Gen 3x2 requirements.

Also, the JMS583 has USB Type-C™ connectivity built in to the controller that any device using the JMS583 can have a USB Type-C™ connector without adding any additional peripheral part. It can save costs to buy parts, and efforts to build inventory, and it can reduce printed circuit board area for the system designs.

The JMS583 supports TRIM to the SSD and can transmit and receive data by both of USB Mass Storage Class Bulk-Only Transport (BOT) and USB Attached SCSI Protocol (UASP) to and from the host respectively. The data storage devices can achieve its summit of performance by taking advantage of these built-in unmatched features.

The JMS583 is well equipped for power management that it can meet a wide variety of power requirements from different scales of data storage systems: those for data centers, network attached storage (NAS) systems, and portable SSDs, and even those for thumb-sized Internet-of-Thing (IoT) devices.

Owing to its USB Type-C™ connectivity, the JMS583 can work with some power management controllers to a USB Power Delivery (PD) enabled data storage device. The data storage devices having SSDs of large capacity can accept the electrical power from sources of energy, such as hosts acting as a power provider of USB PD to supply sufficient electricity to the device after they negotiate with each other, without plugging in.

Finally, the JMS583 is a new product that almost reaches USB3.1 G2 line bandwidth. Using the JMS583, the security system can transfer higher quality video, such as 4K or even 8K, and quicker to their data storage devices than ever.

2 Features

- Integrates with USB Type-C™ multiplexer & configuration channel (CC) logic
- Supports TRIM to the SSD
- Complies with PCI Express Base Specification Revision 3.1a
- Complies with NVM Express 1.3
- Complies with USB 3.1 Gen 1 and Gen 2 Specification, USB Mass Storage Class, Bulk-Only Transport Specification (Revision 1.0)
- Complies with USB Attached SCSI Protocol (UASP) Specification (Revision 4)
- Supports USB Super-Speed/High-Speed/Full-Speed Operation
- Supports USB2.0/USB 3.1 Gen 1/2 power saving mode
- Supports external SPI NVRAM for Vendor VID/PID of USB2.0/USB 3.1 Gen 1/2 device controller
- Thirteen GPIOs for customization
- Provides hardware controlled PWMs
- Provides software utilities for downloading the upgraded firmware code under USB2.0/USB 3.1 Gen1,2
- Design for Windows 7, Windows 10 and MAC 10.10.5 or later version
- Support SCSI / NVMe Pass-through command to allow an application client to transmit a NVMe command to a NVMe device.
- Supports 25MHz external crystal
- Supports 3.3V I/O
- Embedded 5V to 1.0V voltage regulator
- Embedded 5V to 3.3V linear voltage regulator (LDO)
- QFN64 8x8 package

3 Block diagram

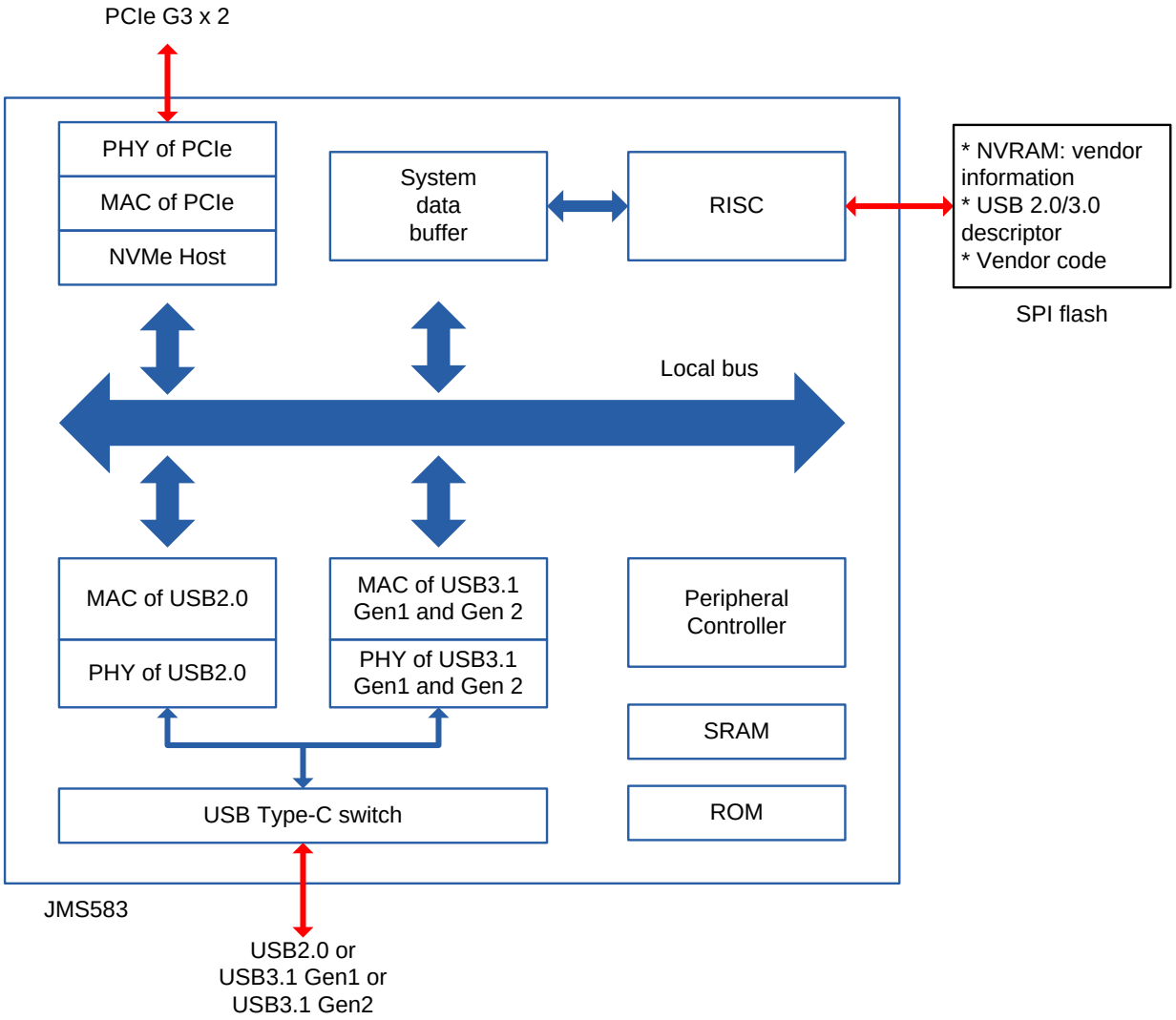
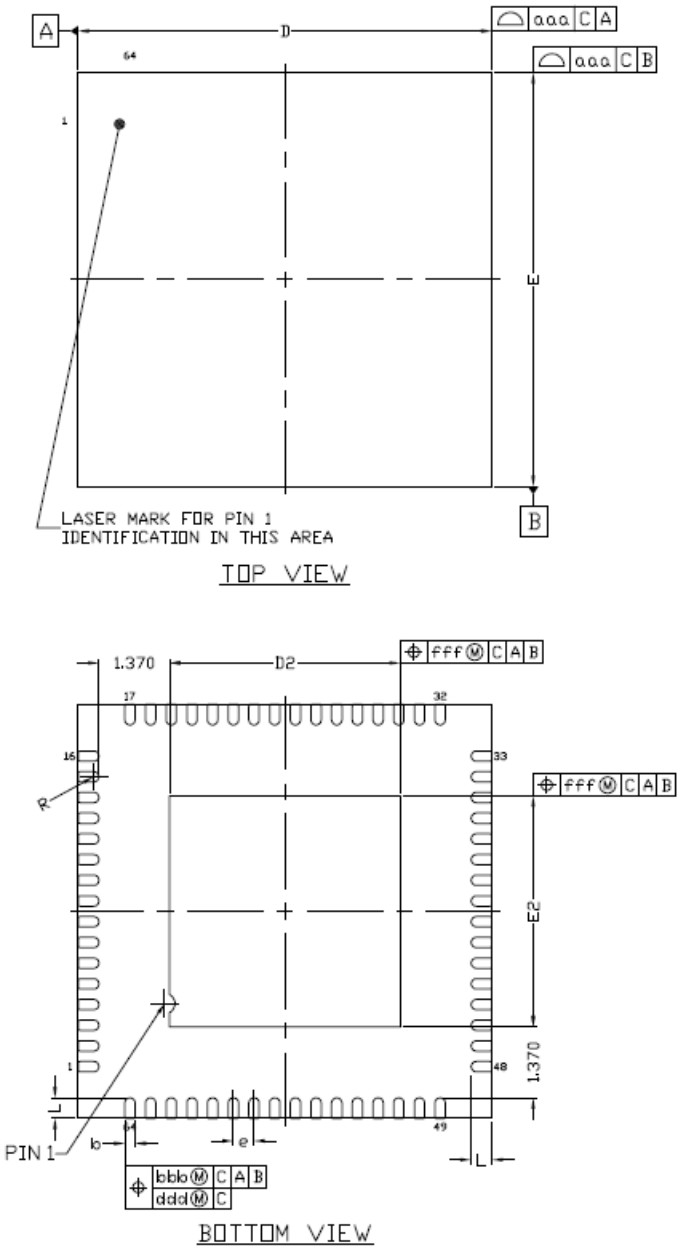


Figure 1 Block diagram

4 Package dimension



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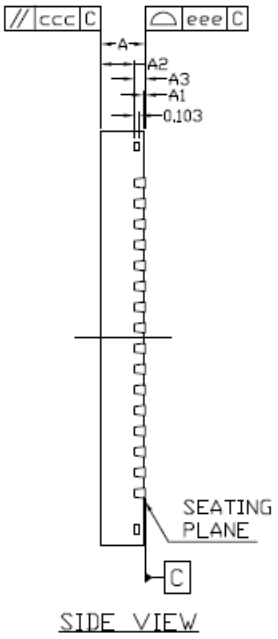

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.900	---	---	0.035
A1	0.000	---	0.050	0.000	---	0.002
A2	---	0.650	0.700	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	8.000 BSC			0.315 BSC		
D2	4.360	4.460	4.560	0.172	0.176	0.180
E	8.000 BSC			0.315 BSC		
E2	4.360	4.460	4.560	0.172	0.176	0.180
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

(2)

Figure 2 Package outline drawing of QFN64 8x8

5 Package pin-out

5.1 Pin assignment

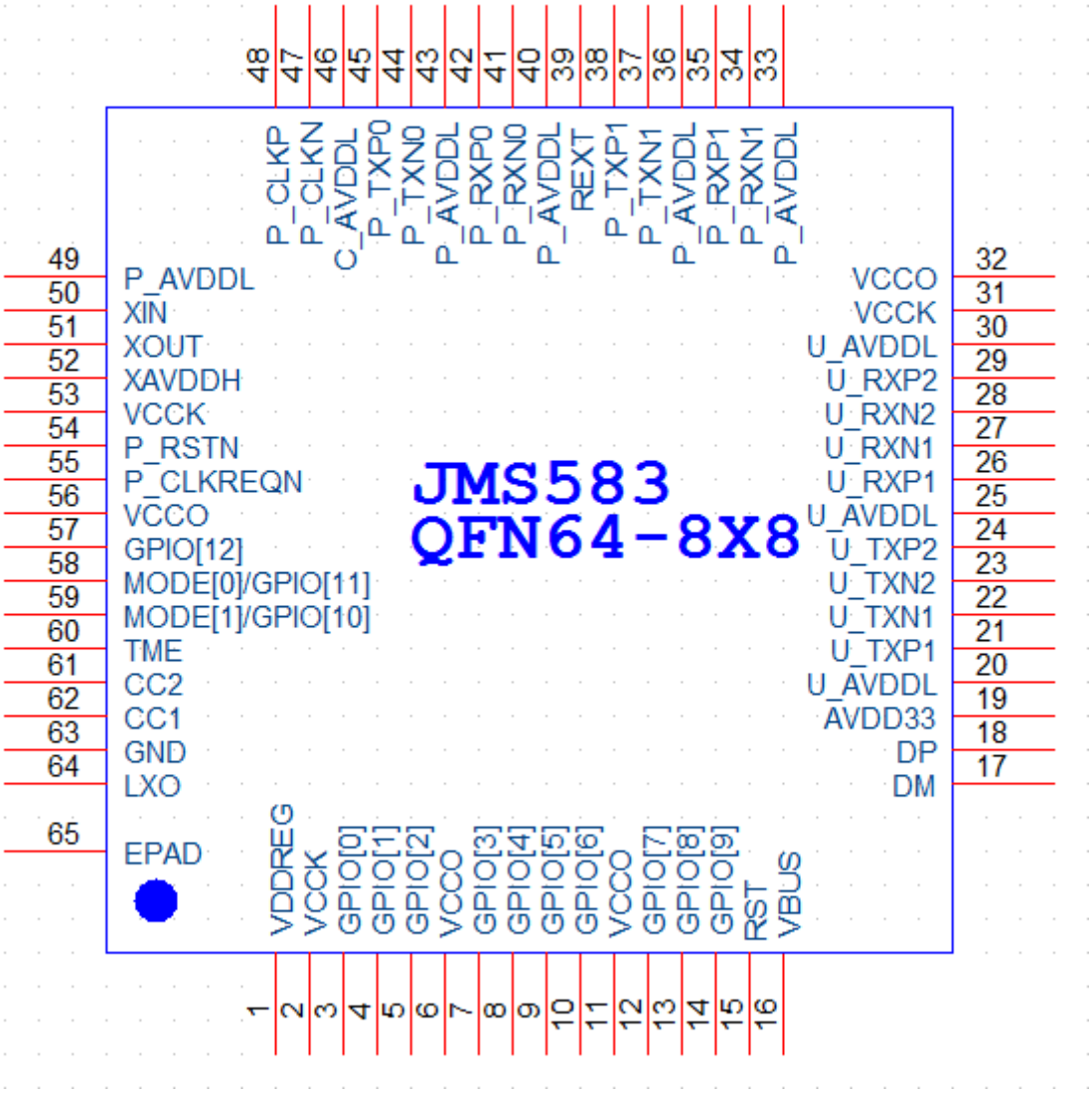

Figure 3 Pin assignment of JMS583

5.2 Pin type definition

Table 1 Pin type definition

Pin type	Definition
A	Analog
D	Digital
I	Input
O	Output
P	Power
IO	Bi-directional
H	Internal weak pull-high (Max. 59 kΩ, Typical 38 kΩ, Min. 27 kΩ)

5.3 Pin description

5.3.1 PCIe interface

Table 2 Pin description – PCIe interface

Signal Name	QFN 64	Type	Description
P_RXN1	34	AI	**PCIe Port RX- Signal of Lane 1**
P_RXP1	35	AI	**PCIe Port RX+ Signal of Lane 1**
P_TXN1	37	AO	**PCIe Port TX- Signal of Lane 1** A 220 nF capacitor should be connected between this pin and PCIe connector.
P_TXP1	38	AO	**PCIe Port TX+ Signal of Lane 1** A 220 nF capacitor should be connected between this pin and PCIe connector.
REXT	39	AI	**External Reference Resistance** A 12 kΩ±1% external resistor should be connected to this pin.
P_RXN0	41	AI	**PCIe Port RX- Signal of Lane 0**
P_RXP0	42	AI	**PCIe Port RX+ Signal of Lane 0**
P_TXN0	44	AO	**PCIe Port TX- Signal of Lane 0** A 220 nF capacitor should be connected between this pin and PCIe connector.
P_TXP0	45	AO	**PCIe Port TX+ Signal of Lane 0** A 220 nF capacitor should be connected between this pin and PCIe connector.
CLKP	48	DO	**Differential Clock P** 100Mhz reference clock for Device.
CLKN	47	DO	**Differential Clock N** 100Mhz reference clock for Device.
P_RSTN	54	DO	**PCIE Reset for Device**
P_CLKREQN	55	DIO	**This is for L1 substate**

5.3.2 USB 3.1 Gen 2 interface

Table 3 Pin description – USB 3.1 Gen 1 and Gen 2 shared interface

Signal Name	QFN 64	Type	Description
U_RXP2	29	AI	**Super Speed RX+ 2 signal**
U_RXN2	28	AI	**Super Speed RX- 2 signal**
U_RXN1	27	AI	**Super Speed RX- 1 signal**
U_RXP1	26	AI	**Super Speed RX+ 1 signal**
U_TXP2	24	AO	**Super Speed TX+ 2 signal** A 100 nF capacitor should be connected between this pin and USB connector.
U_TXN2	23	AO	**Super Speed TX- 2 signal** A 100 nF capacitor should be connected between this pin and USB connector.
U_TXN1	22	AO	**Super Speed TX- 1signal** A 100 nF capacitor should be connected between this pin and USB connector.
U_TXP1	21	AO	**Super Speed TX+1 signal** A 100 nF capacitor should be connected between this pin and USB connector.

5.3.3 USB 2.0 interface

Table 4 Pin description – USB 2.0 interface

Signal Name	QFN 64	Type	Description
DP	18	AIO	**USB 2.0 Bus D+ Signal**
DM	17	AIO	**USB 2.0 Bus D- Signal**
VBUS	16	PI	**USB 5V VBUS power for LDO input**

Signal Name	QFN 64	Type	Description
AVDD33	19	PO	**USB 2.0 Analog 3.3V Output** A capacitor to ground is recommended on this pin. The value should be one uF. The output voltage range is 3.3V±10%. Note: 1. This pin provides power less than 100mA @ 3.3V. 2. This pin can afford chip internal power usage only.

5.3.4 Crystal interface

Table 5 Pin description – Crystal interface

Signal Name	QFN 64	Type	Description
XIN	50	AI	**Crystal Input/Oscillator Input** It is connected to a 25MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage should range in 3.3V±5%.
XOUT	51	AO	**Crystal Output** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved for No Connection (NC). The output variation range is around ±30ppm (input dependent). And the output voltage range is 3.3V±5% (input dependent).

5.3.5 Switching regulator interface

Table 6 Pin description – Switching regulator interface

Signal Name	QFN 64	Type	Description
VDDREG	1	PI	**Voltage Regulator 5V Power Supply**
GND	63	PI	**Voltage Regulator Ground**
LXO	64	PO	**Voltage Regulator 1.0V Output** Switch node. Connect with external power inductor with a value of 4.7 uH.

5.3.6 USB Type-C™ configuration channel

Table 7 Pin description - USB Type-C™ configuration channel

Signal Name	QFN 64	Type	Description
CC1	62	AI	**CC pin1 input for voltage detection** The maximum tolerant input voltage is 3.3V.
CC2	61	AI	**CC pin2 input for voltage detection** The maximum tolerant input voltage is 3.3V.

5.3.7 Control and GPIO interface

Table 8 Pin description – Control and GPIO interface

Signal Name	QFN 64	Type	Description
RST	15	DI	**System Global Reset Input** Active-low to reset the entire chip. An external RC should be connected to this pin.
TME	60	DI	**MP Test Mode Enable** This pin is reserved for IC mass production testing. Keep this pin to logic “0” in normal operation.
GPIO[0]	3	DIOH	**Serial Flash (SO)** After power on status detecting, this pin becomes Data Output of serial flash. This pin is by default set to input.
GPIO[1]	4	DIOH	**Serial Flash (SCK)** This pin is Serial Flash Data Clock (SCK) of serial flash. This pin is by default set to output.
GPIO[2]	5	DIOH	**Serial Flash(SI)** Serial Flash Data Input (SI) of serial flash. This pin is by default set to output.
GPIO[3]	7	DIOH	**Serial Flash(CE0#)** This pin functions as Chip Enable (CE0#) of Serial Flash
GPIO[4]	8	DIOH	**GPIO[4]** Can be configured by customer firmware.
GPIO[5]	9	DIOH	**GPIO[5]** Can be configured by customer firmware.
GPIO[6]	10	DIOH	**GPIO[6]** Can be configured by customer firmware.
GPIO[7]	12	DIOH	**GPIO[7]** Can be configured by customer firmware.

Signal Name	QFN 64	Type	Description
UAO/GPIO[8]	13	DIOH	**RISC UART TX interface/GPIO[8]** Can be configured by customer firmware.
UAI/GPIO[9]	14	DIOH	**RISC UART RX interface/GPIO[9]** Can be configured by customer firmware.
GPIO[10]	59	DIOH	**GPIO[10]** Can be configured by customer firmware.
GPIO[11]	58	DIOH	**GPIO[11]** Can be configured by customer firmware.
GPIO[12]	57	DIOH	**GPIO[12]** Can be configured by customer firmware.

5.3.8 Power supply

Table 9 Pin description – Power supply interface

Signal Name	QFN 64	Type	Description
VCCO	6, 11, 32, 56	PI	**3.3V I/O power supply**
VCCK	2, 31, 53	PI	**1.0V core power supply**
AVDDL	20, 25, 30, 33, 36, 40, 43, 46, 49	PI	**Analog 1.0V power supply**
XAVDDH	52	PI	**3.3V crystal pad power (i.e., AVDDXTAL)**

5.4 LED indicator

By default, GPIO [4] is used as LED indicator. If the user has a different application for LED function, please contact JMicron's AE before PCB layout.

5.5 GPIO initial value

All GPIOs set as input mode and disable internal pull-up function while in reset. After reset, the firmware will program all GPIOs as input mode. Afterward, the initial value of GPIOs is read and stored in the system RAM for future using.

6 Clock and reset

6.1 Crystal input

Single crystal input (25MHz) is needed.

Table 10 Crystal electrical specification

Parameter	Symbol	Min	Typical	Max	Unit
Crystal start up time v.s AVDDL	$T_{Crystal}$			5	mS
Crystal Frequency	f_{clk}		25		MHz
Long term stability (Crystal Only)	$\Delta f_{MAX\_Crystal}$	-30		30	ppm
Long term stability (On Board)	$\Delta f_{MAX\_OnBoard}$	-150		150	ppm
Equivalent Series Resistance	**ESR**			55	Ω

6.2 Reset input

All functions will be initialized by reset except the Analog Power-On Reset Circuit depending on the Power on-off.

The reset input pin is the Schmitt trigger input pin. VT+ Schmitt Trigger Low to High Threshold Point is 1.61V(min) and VT- Schmitt Trigger High to Low Threshold Point is 1.35V(max).

Table 11 Reset voltage

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Reset voltage	V_{T+}	Low to High	1.61	1.69	1.77	V
Reset voltage	V_{T-}	High to Low	1.18	1.27	1.35	V

7 Electrical characteristics

7.1 Absolute maximum rating

Table 12 Absolute maximum rating

Parameter	Symbol	Condition	Min	Max	Unit
Digital 3.3V	$VCCO_{(ABS)}$		-0.3	4.13	V
Digital 1.0V	$VCCK_{(ABS)}$		-0.3	1.6	V
Switching regulator	$AVDDS_{(ABS)}$		-0.3	5.5	V
3.3V crystal pad power	$XAVDDH_{(ABS)}$		-0.3	4.13	V
Analog 1.0V	$AVDDL_{(ABS)}$		-0.3	1.6	V
USB VBUS	VBUS		-	5.5	V
Digital I/O input voltage	$V_{I(D)}$		-0.3	4.13	V
Storage temperature	$T_{STORAGE}$		-40	150	^{o}C

7.2 Operating voltage and temperature

Table 13 Operating voltage and temperature

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V power supply	VCCO		3.0	3.3	3.6	V
Digital 1.0V power supply	VCCK		0.95	1.0	1.1	V
Switching regulator	AVDDS		4.5	5.0	5.5	V
3.3V crystal pad power	XAVDDH		3.0	3.3	3.6	V
Analog 1.0V power supply	AVDDL		0.95	1.0	1.1	V
USB VBUS	VBUS		4.5	5.0	5.5	V
Digital I/O input voltage	$V_{I(D)}$		3.0	3.3	3.6	V
Ambient operation temperature	T_A		0		70	^{o}C

7.3 External clock source conditions

Table 14 External clock source conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				25		MHz
Clock Duty Cycle			45	50	55	%

7.4 Power dissipation

7.4.1 USB 2.0 to PCIe

7.4.1.1 Operation with PCIe L0 state

Table 15 Power dissipation – USB 2.0 to PCIe L0

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1.8		mA
Digital 1.0V	VCCK	Operate @ 1.0V		157.6		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1.3		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		292.8		mA

7.4.1.2 Idle with PCIe L0 state

Table 16 Power dissipation – USB 2.0 to PCIe L0

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1.6		mA
Digital 1.0V	VCCK	Operate @ 1.0V		152.1		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1.2		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		273.8		mA

7.4.1.3 Suspend with PCIe L2 state

Table 17 Power dissipation – USB 2.0 to PCIe L2

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		0.3		mA
Digital 1.0V	VCCK	Operate @ 1.0V		2.0		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		0.0		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		0.6		mA

7.4.2 USB 3.1 Gen 1 to PCIe

7.4.2.1 Operation with PCIe L0 state

Table 18 Power dissipation – USB 3.1 Gen 1 to PCIe L0

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1.6		mA
Digital 1.0V	VCCK	Operate @ 1.0V		177.3		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1.2		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		346.3		mA

7.4.2.2 Idle with PCIe L0 state

Table 19 Power dissipation – USB 3.1 Gen 1 to PCIe L0

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1.6		mA
Digital 1.0V	VCCK	Operate @ 1.0V		150.0		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1.2		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		344.6		mA

7.4.2.3 Suspend with PCIe L2 state

Table 20 Power dissipation – USB 3.1 Gen 1 to PCIe L2

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		0.3		mA
Digital 1.0V	VCCK	Operate @ 1.0V		2.0		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		0.0		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		2.0		mA

7.4.3 USB 3.1 Gen 2 to PCIe

7.4.3.1 Operation with PCIe L0 state

Table 21 Power dissipation – USB 3.1 Gen 2 to PCIe L0

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1.7		mA
Digital 1.0V	VCCK	Operate @ 1.0V		238.3		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1.2		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		422.6		mA

7.4.3.2 Idle with PCIe L0 state

Table 22 Power dissipation – USB 3.1 Gen 2 to PCIe L0

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		1.6		mA
Digital 1.0V	VCCK	Operate @ 1.0V		176.3		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		1.2		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		421.7		mA

7.4.3.3 Suspend with PCIe L2 state

Table 23 Power dissipation – USB 3.1 Gen 2 to PCIe L2

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital 3.3V	VCCO	Operate @ 3.3V		0.3		mA
Digital 1.0V	VCCK	Operate @ 1.0V		2.0		mA
Analog 3.3V	XAVDDH	Operate @ 3.3V		0.0		mA
Analog 1.0V	AVDDL	Operate @ 1.0V		2.0		mA

7.5 I/O DC characteristics

Table 24 I/O DC characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}		-0.3		0.8	V
Input high voltage	V_{IH}		2		5.5	V
Output low voltage	V_{OL}				0.4	V
Output high voltage	V_{OH}		2.4			V
Low Level Output Current	I_{OL}		9.7		21.5	mA
High Level Output Current	I_{OH}		17.0		56.5	mA

7.6 V_{BUS} detector

GPIO[6] is used for V_{BUS} detection. There is a voltage divider circuit on a board. Power source is connected from V_{BUS} 5V. The output is connected to GPIO[6] for V_{BUS} detection.

7.7 Internal linear regulator

Table 25 Internal linear regulator specification

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input Voltage Range	V_{IN_LINEAR}			5		V
Output Voltage Range	V_{OUT_LINEAR}			3.3		V
Max Output Current	I_{MAX}		-	-	150	mA

7.8 Power Ripple

Table 26 Power Ripple

Parameter	Symbol	Condition	Min	Typical	Max	Unit
5V Power Supply [1]	P_{5V}	Operate@USB3.1 G2	133	162	233	mV
3.3V Power Supply [2]	P_{3V3}	Operate@USB3.1 G2	17	19	22	mV
1V Power Supply [3]	P_{1V}	Operate@USB3.1 G2	19	22	29	mV

Note: 1. Test point near Vbus capacitor.

2. Test point at LDO output capacitor.
3. Test point at AVDDL bypass capacitor.

7.9 Power-on sequence

The power-on sequence is defined in Figure 4. Designers should follow all the rules for external power designs.

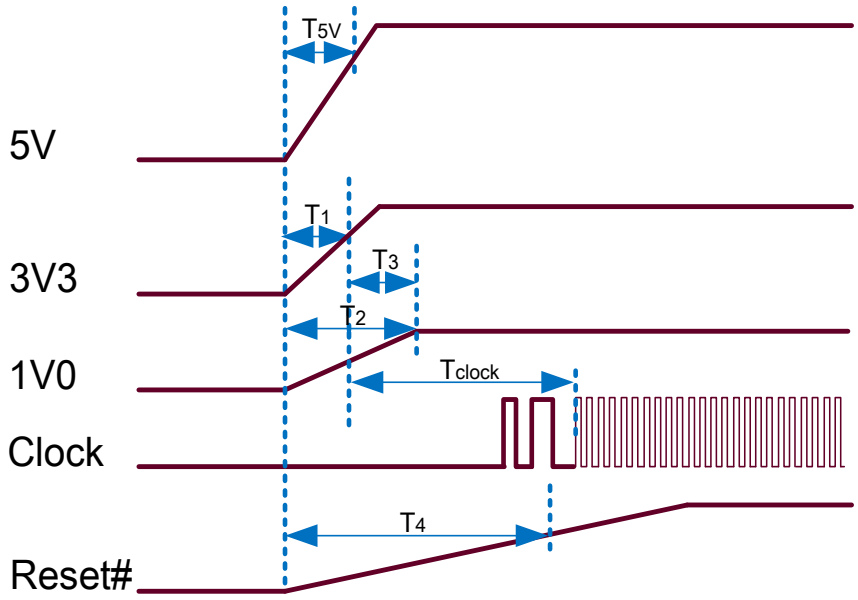

Figure 4 Power-on sequence

T_{5V}: Rise time for 5V power rail from 10% to 90%

T1: Rise time for 3V3 power rail from 10% to 90%

T2: Rise time for 1V0 power rail from 10% to 90%

T3: Time interval between 3V3 power and 1V0 Power

T4: Rise time for RST# signal from 0V to 2V2

$T_{Clock:}$ Time interval between 3V3 and 90% clock swing

Note: Clock must meet 25MHz +/-30ppm during the sequence.

The recommended power sequence and timing requirements are listed in Table 27.

Table 27 Power-on timing requirements

Time	Minimum	Maximum
T_{5V}	-	20 ms
T1	0 ms	10 ms
T2	0 ms	10 ms
T3	-5 ms	5 ms
T4	150 ms	500 ms
T_{CLOCK}	-	5 ms

The RESET timing constraint is based on the external RC reset circuits. To control the charge and discharge time for RC circuits, minimum, and maximum requirements are listed. If designers apply timing control chip to control the reset signal, the only requirement will be the minimum value. In other words, the maximum value can be ignored without problems.

8 Product naming rule and identification

8.1 Format of the part number

The part number consists of the information of provider, product category, device number, package type, material type, product grade (operating temperature), mask ROM version and device version. The format of the part number is illustrated in Figure 5 below.

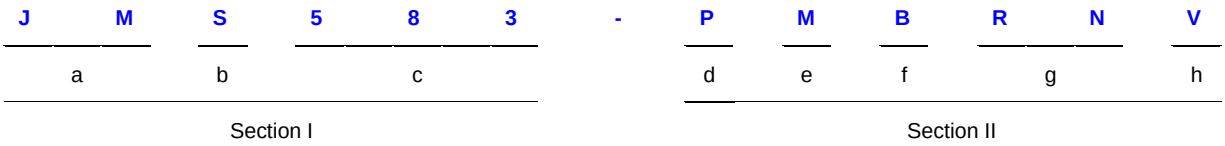

Figure 5 Format of the part number

8.2 Explanation of the part number

Table 28 explains each section of the part number illustrated in Figure 5 above.

Table 28 Explanation of the part number

Section	Length	Purpose	Code(s)	Meaning
a (JM)	2 digits	Brand name	JM	The provider **JM**icron
b (S)	1 digit	Product category	S	**S**oC, system-on-a-chip
c (583)	3 digits	Device number	583	The serial number assigned randomly to form the device name "**JMS583**" in conjunction with brand name and product category.
d (P)	1 digit	Package type	B, L, Q, T	B = **B**GA; L = **L**QFP; Q = **Q**FN; T = **T**QFP
e (M)	1 digit	Material & grade	G, H, I, J	**G** = Gold wired RoHS compliant halogen-free green product; Ta: 0 ~ 70°C. **H** = Copper wired RoHS compliant halogen-free green product; Ta: 0 ~ 70°C. **I** = Gold wired RoHS compliant halogen-free green product; Ta: -40 ~ 85°C. **J** = Copper wired RoHS compliant halogen-free green product; Ta: -40 ~ 85°C.

Section	Length	Purpose	Code(s)	Meaning
f (B)	1 digit	Internal bonding type	A, B, C, …	A, B, C, …
g (RN)	2 digit	Version of mask ROM	A0, A1, A2, … B0, B1, B2, … Z0	Version **A0**, **A1**, **A2**, … Version **B0**, **B1**, **B2**, … Version **Z0** = no mask ROM
h (V)	1 digit	Version of the IC	A, B, C, …	Version **A**, **B**, **C**, …

8.3 Top mark

Each device has its unique top mark containing the information of provider, device name, part number, manufacturing date code, lot number and pin one identifier for identification. The top mark is illustrated in Figure 6 below.

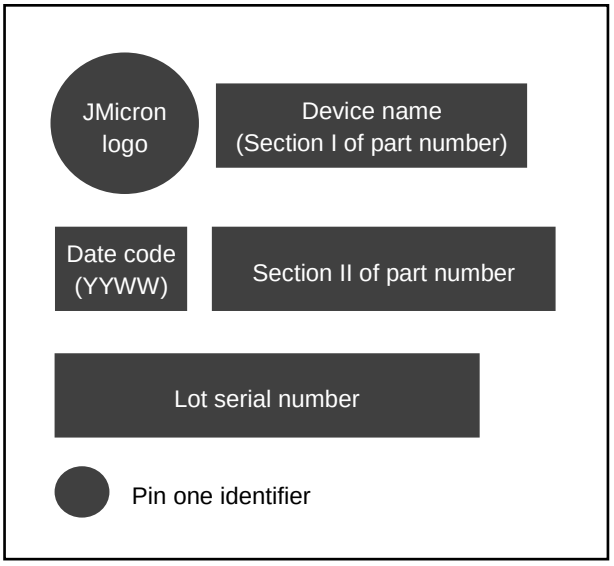

Figure 6 Illustration of device top mark