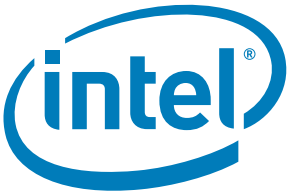


Intel® SD74 NAND Flash Memory

JS29F04G08AANB1, JS29F08G08CANB2, JS29F16G08FANB1

Datasheet

Product Features

- Single-level cell (SLC) Technology
- Organization:
  - — Page size:
    x8: 2,112 bytes (2,048 + 64 bytes)
  - — Block size: 64 pages (128K + 4K bytes)
  - — Plane size: 2,048 blocks
  - — Device size: 4Gb: 4,096 blocks; 8Gb: 8,192 blocks; 16Gb: 16,384 blocks
- Read performance:
  - — Random read: 25µs (MAX)
  - — Sequential read: 25ns (MIN)
- Write performance:
  - — Page program: 220µs (TYP)
- Block erase: 1.5ms (TYP)
- Data Retention:
  - — 10 years
- Endurance:
  - — 100,000 PROGRAM/ERASE cycles
- First block (block address 00h):
  - — Guaranteed to be valid up to 1,000 PROGRAM/ERASE cycles
- Vcc:
  - — 2.7V – 3.6V
- Operating Temperature:
  - — -25 ^{o}C to 85 ^{o}C
- Command set:
  - — Industry-standard basic NAND Flash command set
- Advanced Command Set:
  - — Two-plane commands
  - — Interleaved die operation
  - — READ UNIQUE ID (contact factory)
  - — Internal Data Move: Operations supported within the plane from which data is read
- Operation status byte:
  - — Provides software method for detecting:
    - — Operation completion
    - — Pass/fail condition
    - — Write-protect status
- Ready/busy# (R/B#) signal:
  - — Provides a hardware method for detecting PROGRAM or ERASE cycle completion
- WP# signal:
  - — Write protect entire device
- RESET:
  - — Required after power-up
- Package Types:
  - — 48-pin TSOP Type 1
- Configuration:

# of Die	# of CE#	# of R/B#	I/O
1	1	1	Common
2	2	2	Common
4	2	2	Common

Order Number: 312774-012US
March 2007

Contents

Revision History

Date	Revision	Description
March 2007	012	• Added missing Test Conditions table.
February 2007	011	• Changed comment for the NVB spec for the 16Gb device. Edited some typos in rev 010.
February 2007	010	• Deleted line item JS29F08G08CANB1. • Added notes about 81H in second command cycle of dual plane program operations in Section 7.7.4, “TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h or 80h-11h-81h-10h” on page 41.
November 2006	009	• Updated the Table 20, “Intel® NAND Flash Memory Ordering Information” on page 69. • Deleted the OCPL figure in the package section.
13-Sep-06	008	• Updated the R/B# and R/B2# description in Section 3.0, “Signal Assignments and Descriptions” on page 11. • Updated the part number decoder in Section 10.0, “Ordering Information” on page 69.
8-Sep-06	007	• Added configuration table to title page. • Updated the ordering information and part number decoder in Section 10.0, “Ordering Information” on page 69. • Changed the 8 Gb part number from JS29F08G08BANB1 to JS29F08G08CANB1 throughout the document to reflect the change to 2 CEs.
22-Aug-06	006	• Updated document to reflect 2 CE#s for the dual-die package device. • Section 7.2.4, “READ ID 90h” on page 27: Revised description. • Package diagrams have been updated. • Figure 1, “Intel® SD74 NAND Flash Memory Functional Block Diagram” on page 7: Added “(2 planes)” to the NAND Flash Array. • Table 16, “Two-Plane Command Set” on page 25: Deleted “MULTIPLE-DIE READ STATUS” from command 06h and updated note 3. • Section 7.7.2, “TWO-PLANE PAGE READ 00h-00h-30h” on page 39: Updated the fourth paragraph. • Section 7.7.10, “TWO-PLANE/MULTIPLE-DIE READ STATUS 78h” on page 47: Updated first paragraph and added a new paragraph at the end of the section. • Section 7.8, “Interleaved Die Operations” on page 48: Updated final paragraph. • Section 7.9.1, “RESET FFh” on page 54: Added “to all CE#s” and “and OTP operations” to the last paragraph. • Section 6.1, “Vcc Power Cycling” on page 19: Changed 1ms to 10µs in first paragraph; added “to all CE#s” in last paragraph. • Figure 13, “AC Waveforms During Power Transitions” on page 20: Updated WE# signal. • Table 14, “PROGRAM/ERASE Characteristics” on page 23: Added note 4. • Figure 36, “TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle” on page 48: Added figure showing all timing parameters. • Section 4.0, “Package Information” on page 13: Inserted recently updated versions of package diagrams.
1-Aug-06	005	Updated the Operating Temperature range. Updated with new product naming convention, and document title change.
29-Jun-06	004	Corrected typos in Section 6.0, “Electrical Characteristics”.
15-Jun-06	003	The maximum number of programming operations before an erase is required has been reduced from 8 to 4. This change is reflected in Table 14, “PROGRAM/ERASE Characteristics” on page 23 in the Electrical Characteristics chapter and Section 7.3.1, “PROGRAM PAGE 80h–10h” on page 31.
02-Jun-06	002	• Adjusted Product Features section on page 1, including Write Performance Page Program values from to • Adjusted electrical specifications. See Section 6.0, “Electrical Characteristics” on page 19 and the product features section on page 1. • Changes to Section 7.0, “Command Definitions” on page 24.
March 2006	001	• Initial Release.

1.0 Introduction

NAND Flash technology provides a cost-effective solution for applications requiring high-density solid-state storage. The JS29F4G08AANB1 is a 4Gb NAND Flash memory device. The JS29F08G08CANB2 is a two-die stack that operate as two independent 4Gb devices, providing a total storage capacity of 8Gb in a single package. The JS29F16G08FANB1 is a four-die stack that operate as two independent 8Gb devices, providing a total storage capacity of 16Gb in a single, space-saving package. Intel® NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

Intel® NAND Flash device uses a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Additional pins control hardware write protection (WP#) and monitor device status (R/B#).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

The Intel® SD74 NAND Flash Memory device contains two planes per die. Each plane consists of 2,048 blocks. Each block is subdivided into 64 programmable pages. Each page consists of 2,112 bytes. The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area. The 64-byte area is typically used for error management functions.

The contents of each page can be programmed in 220µs, and an entire block can be erased in 1.5ms (TYP). The Intel® SD74 NAND Flash Memory device is a high performance part with a maximum tPROG specification of 500µs, a maximum tBERS specification of 2ms, and a maximum tR specification of 25µs. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/ PROGRAM endurance is specified at 100,000 cycles when using appropriate error correcting code (ECC) and error management.

2.0 Functional Overview

This section provides an overview of the device in the following sections:

- Section 2.1, “Architecture” on page 6
- Section 2.2, “Memory Map and Addressing” on page 7

2.1 Architecture

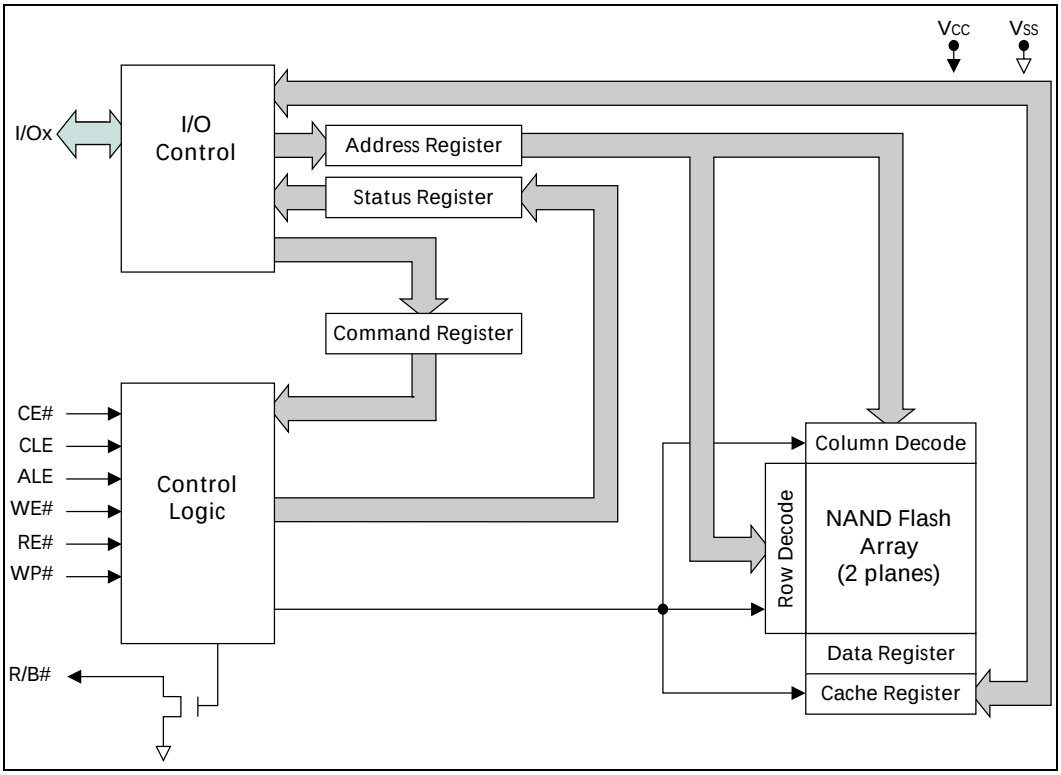
These devices use standard NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same signals and received by I/O control circuits. This provides a memory device with a low signal count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

The data is transferred to or from the NAND Flash memory array, byte by byte through a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data, whereas the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations and is erased in block-based operations. During normal page operations, the data and cache registers are tied together and act as a single register. During cache operations the data and cache registers operate independently to increase data throughput.

These devices also have a status register that reports the status of device operation.

Figure 1. Intel® SD74 NAND Flash Memory Functional Block Diagram



2.2 Memory Map and Addressing

This section includes the following sections describing memory mapping and array organization for the x8 device.

- Section 2.2.1, “Memory Map for the SD74 Device” on page 8
- Section 2.2.2, “Array Organization and Addressing for JS29F04G08AANB1 and JS29F08G08CANB2” on page 8
- Section 2.2.3, “Array Organization and Addressing for JS29F16G08FANB1” on page 9

2.2.1 Memory Map for the SD74 Device

Figure 2. Memory Map: SD74 Device

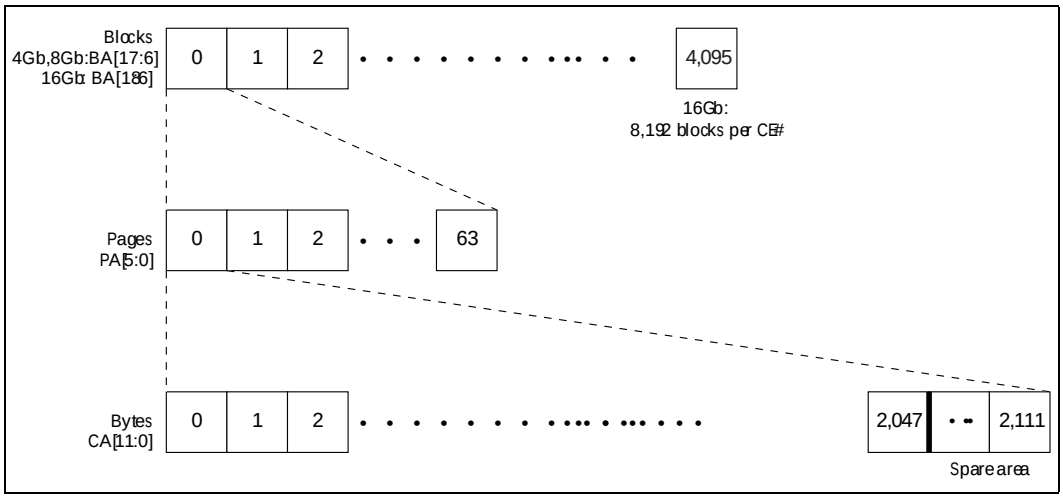


Table 1. Operational Example: SD74 Device

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x000000083F	0x0000000840–0x0000000FFF
0	1	0x0000010000	0x000001083F	0x0000010840–0x0000010FFF
0	2	0x0000020000	0x000002083F	0x0000020840–0x0000020FFF
...	...	...	...	
4,095	62	0x03FFFE0000	0x03FFFE083F	0x03FFFE0840–0x03FFFE0FFF
4,095	63	0x03FFFF0000	0x03FFFF083F	0x03FFFF0840–0x03FFFF0FFF

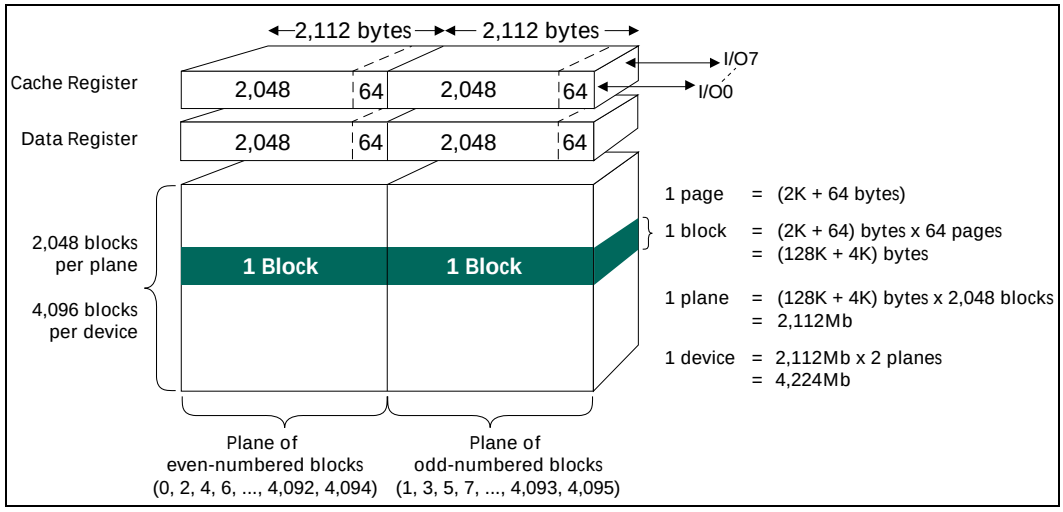
Note: As shown in Table 2, the high nibble of ADDRESS cycle 2 has no assigned address bits; however, these 4 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.

The 12-bit column address is capable of addressing from 0 to 4,095 bytes on a x8 device; however, only bytes 0 through 2,111 are valid. Bytes 2,112 through 4,095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

2.2.2 Array Organization and Addressing for JS29F04G08AANB1 and JS29F08G08CANB2

Addresses for JS29F04G08AANB1 and JS29F08G08CANB2 devices are loaded using a five-cycle sequence. The first two cycles contain the column address, and the last three cycles contain the page and block addresses. The column address is a 12-bit address. The page address is a 6-bit address used to address 64 pages in each block, and the block address is a 12-bit address used to address 4096 blocks per CE# in the device.

Figure 3. Array Organization: JS29F04G08AANB1 and JS29F08G08CANB2



Note: For the 8Gb JS29F08G08CANB2, the 4Gb array organization shown here applies to each chip enable (CE1# and CE2#).

Table 2. Array Addressing: JS29F04G08AANB1 and JS29F08G08CANB2

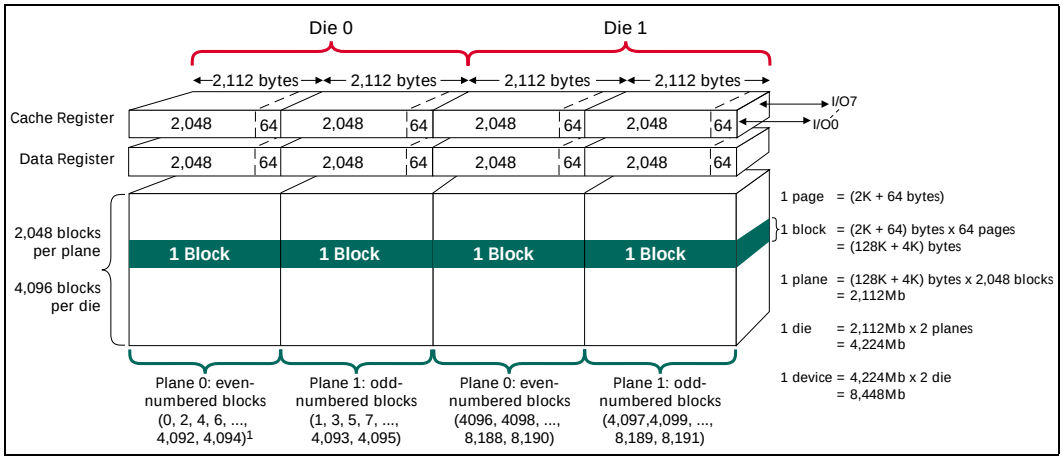
Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes:
1. Definitions:
   — CAx = column address
   — PAx = page address
   — BAx = block address
2. Block address concatenated with page address = actual page address.
3. If CA11 = "1" then CA[10:6] must be "0."

2.2.3 Array Organization and Addressing for JS29F16G08FANB1

Addresses for JS29F16G08FANB1 devices are loaded using a five-cycle sequence. The first two cycles contain the column address, and the last three cycles contain the page and block addresses. The column address is a 12-bit address. The page address is a 6-bit address used to address 64 pages in each block, and the block address is a 13-bit address used to address 8192 blocks per CE# in the device. The most significant block address bit is also a die selector.

Figure 4. Array Organization: JS29F16G08FANB1



Notes:

1. Die 0, Plane 0: BA18 = 0, BA6 = 0
   Die 0, Plane 1: BA18 = 0, BA6 = 1
   Die 1, Plane 0: BA18 = 1, BA6 = 0
   Die 1, Plane 1: BA18 = 1, BA6 = 1
2. For the JS29F16G08FANB1device, the 8Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 3. Array Addressing: JS29F16G08FANB1

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	BA18[3]	BA17	BA16

Note:

1. Definitions:
   — CAx = column address
   — PAx = page address
   — BAx = block address
2. If CA11 = “1” then CA[10:6] must be “0.”
3. Die address boundary: 0 = 0 – 4 Gb, 1 = 4 Gb – 8 Gb.

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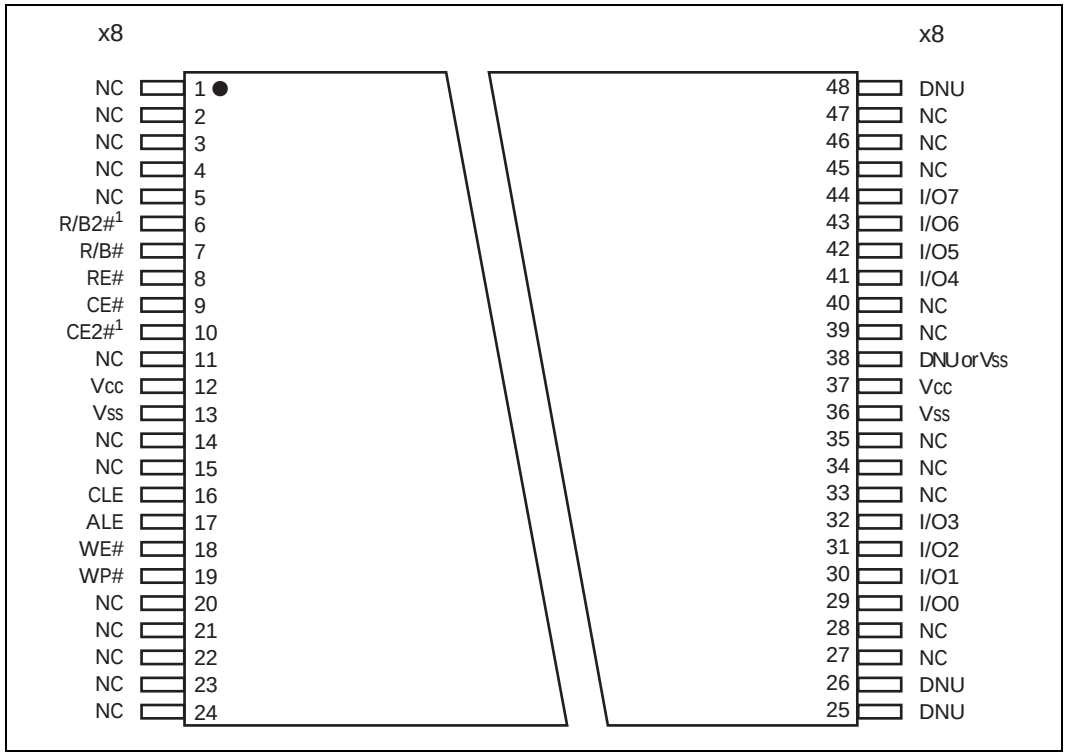
3.0 Signal Assignments and Descriptions

Figure 5. Signal Assignment (Top View) 48-Pin TSOP



Note:
1. CE2# and R/B2# are available on 8Gb and 16Gb devices only. These pins are NC for other configurations.

Table 4. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Description
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#, CE2#	Input	Chip enable: Gates transfers between the host system and the NAND Flash device. After the device starts a PROGRAM or ERASE operation, CE# can be de-asserted. For the 8Gb configuration, CE# controls the first 4Gb of memory; CE2# controls the second 4Gb of memory. For the 16Gb configuration, CE# controls the first 8Gb of memory; CE2# controls the second 8Gb. See the Bus Operation section, starting on page 14, for additional operational details.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#	Input	Read enable: Gates transfers from the NAND Flash device to the host system.
WE#	Input	Write enable: Gates transfers from the host system to the NAND Flash device.

Table 4. Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Description
WP#	Input	Write protect: Protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
I/O[7:0]	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#, R/B2#	Output	Ready/busy: An open-drain, active-LOW output, that uses an external pull-up resistor. R/B# is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during READ operations to indicate when data is being transferred from the array into the serial data register. When these operations have completed, R/B# returns to the high-Z state. In the 8Gb and 16Gb configurations, R/B# is for the memory enabled by CE#; R/B2# is for the memory enabled by CE2#.
VCC	Supply	VCC: Power supply.
VSS	Supply	VSS: Ground connection.
NC	–	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	–	Do not use: DNUs must be left unconnected.

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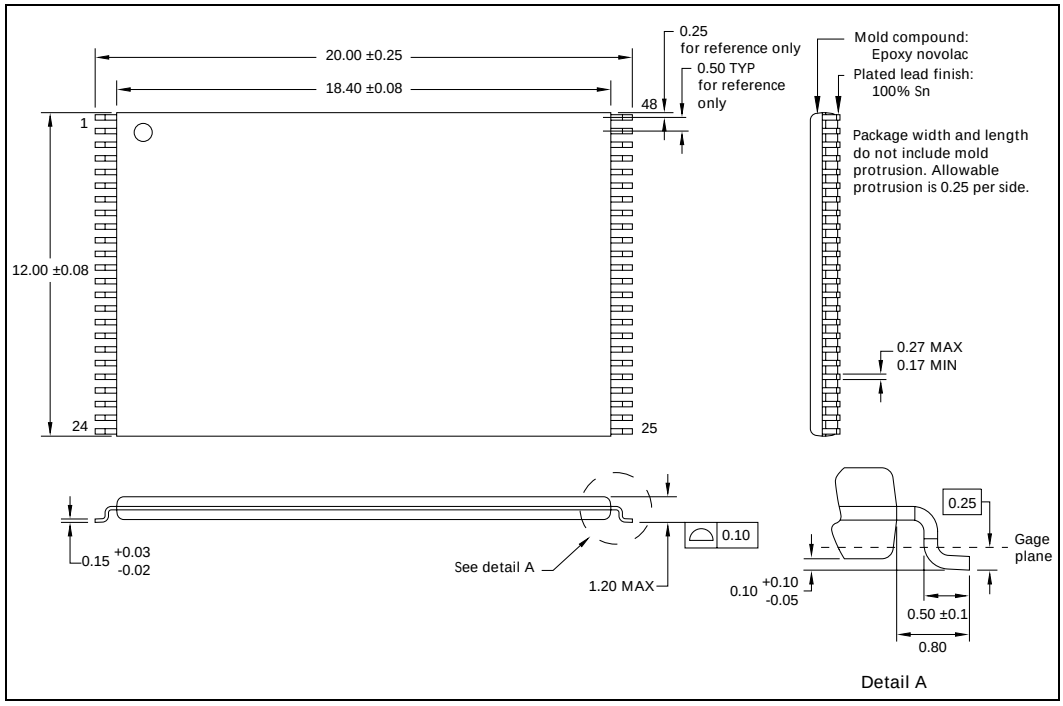
4.0 Package Information

Figure 6. 48-pin TSOP



Note:
1. All dimensions are in millimeters.

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5.0 NAND Flash Bus Operations

The bus on the Intel® SD74 NAND Flash Memory devices is multiplexed. Data I/O, addresses, and commands all share the same pins, I/O[7:0].

The command sequence normally consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and one or more DATA cycles—either READ or WRITE.

5.1 Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control the NAND Flash device READ and WRITE operations. On the 16Gb device, CE# and CE2# each control independent 8Gb arrays. On the 8Gb device, CE# and CE2# each control independent 4Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the NAND Flash memory will accept command, address, and data information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 62, “READ Operation with CE# “Don’t Care”” on page 62 and Figure 70, “Program Operation with CE# “Don’t Care”” on page 65 for examples of CE# “Don’t Care” operations.

The CE# “Don’t Care” operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

5.2 Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- The device is not busy

As exceptions, the device accepts the TWO-PLANE/MULTIPLE-DIE READ STATUS, and RESET commands when busy. Commands are transferred to the command register on the rising edge of WE# (see Figure 60, “TWO-PLANE/MULTIPLE-DIE READ STATUS Operation” on page 61). Commands are input on I/O[7:0].

5.3 Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH

Addresses are input on I/O[7:0]. Bits not part of the address space must be LOW.

The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Table 15, “Command Set” on page 24).

5.4 Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy.

Data is input on I/O[7:0]. See Figure 56, “INPUT DATA LATCH Cycle” on page 59 for additional data input details.

5.5 READs

After a READ command is issued, data is transferred from the memory array to the data register on the rising edge of WE#. R/B# goes LOW for tR and transitions HIGH after the transfer is complete. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 61, “PAGE READ Operation” on page 61 for detailed timing information.

The READ STATUS (70h) command, TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command, or the R/B# signal can be used to determine when the device is ready.

If a controller is using a timing of 30ns or longer for ^{t}RC, use Figure 57, “SERIAL ACCESS Cycle After READ” on page 59 for proper timing. If ^{t}RC is less than 30ns, use Figure 58, “SERIAL ACCESS Cycle After READ (EDO Mode)” on page 60 for extended data output (EDO) timing.

5.6 Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin’s open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 9 on page 16).

On the 8Gb JS29F08G08CANB2, R/B# provides a status indication for the 4Gb section enabled by CE#, and R/B2# does the same for the 4Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 4Gb section.

On the 16Gb JS29F16G08FANB1, R/B# provides a status indication for the 8Gb section enabled by CE#, and R/B2# does the same for the 8Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 8Gb section. On the 16Gb JS29F16G08FANB1, R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 4Gb and 8Gb section, respectively.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC).

Figure 7. Time Constants

$$TC = R \times C$$

Where R = Rp and C = total capacitive load

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figure 11 on page 17, and Figure 12 on page 18, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

Figure 8. Minimum Rp

$$Rp\ (MIN, 3.3V\ part) = \frac{V_{CC}\ (MAX) - V_{OL}\ (MAX)}{I_{OL} + \Sigma I_{IL}} = \frac{3.2V}{8mA + \Sigma I_{IL}}$$

Where ΣI_{IL} is the sum of the input currents of all devices tied to the R/B# pin.

Figure 9. READY/BUSY# Open Drain

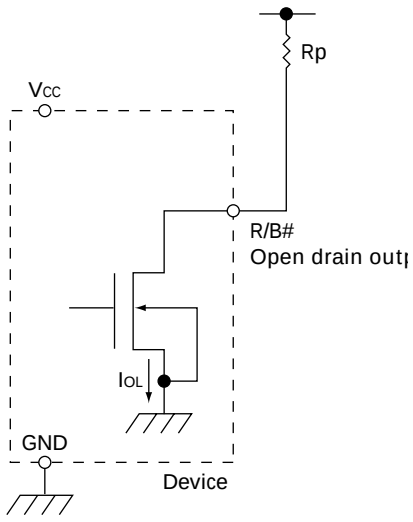
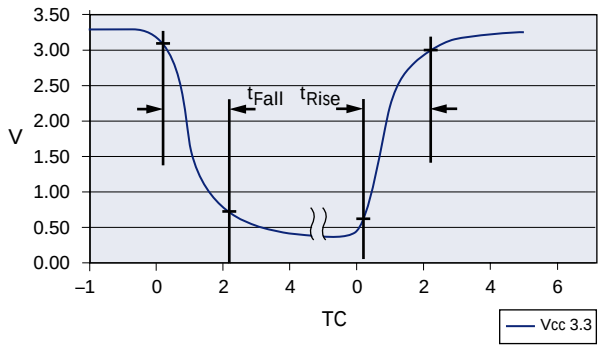


Figure 10. tRise and tFall



Notes:
1. tRise and tFall calculated at 10 percent–90 percent points.
2. tRise primarily dependent on external pull-up resistor and external capacitive loading.
3. tFall [a] 10ns at 3.3V.
4. See TC values in Figure 12, “TC vs. Rp” on page 18 for approximate Rp value and TC.

Figure 11. tIol vs. Rp

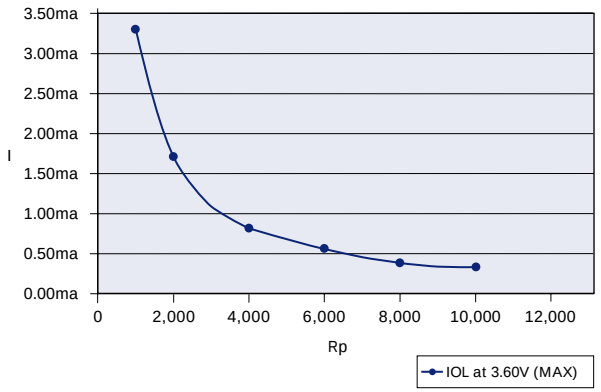


Figure 12. TC vs. Rp

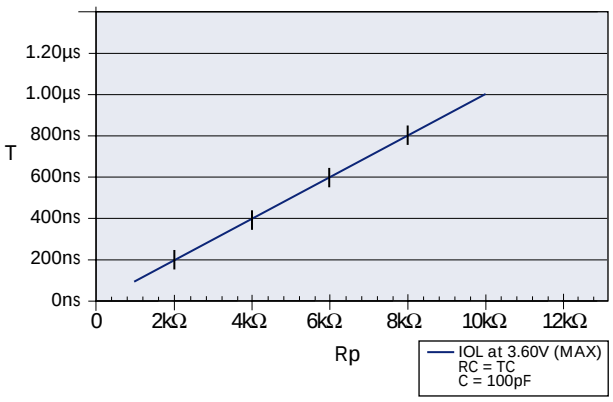


Table 5. Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#[1]	Mode	
H	L	L	↑	H	X	Read mode	Command input
L	H	L	↑	H	X		Address input
H	L	L	↑	H	H	Write mode	Command input
L	H	L	↑	H	H		Address input
L	L	L	↑	H	H	Data input	
L	L	L	H	↓	X	Sequential read and data output	
X	X	X	H	H	X	During read (busy)	
X	X	X	X	X	H	During program (busy)	
X	X	X	X	X	H	During erase (busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0V/Vcc[1]	Standby	

Notes:
1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

§ §

6.0 Electrical Characteristics

Table 6. Absolute Maximum Ratings by Device

Parameter / Condition		Symbol	Min	Max	Unit
Voltage input	JS29F04G08AANB1 JS29F08G08CANB2 JS29F16G08FANB1	VIN	–0.6	+4.6	V
VCC supply voltage	JS29F04G08AANB1 JS29F08G08CANB2 JS29F16G08FANB1	VCC	–0.6	+4.6	V
Storage temperature		TSTG	–65	+150	°C
Short circuit output current, I/Os			–	5	mA
Note: Voltage on any pin relative to VSS.					

Caution: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating ***only***, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7. Recommended Operating Conditions

Parameter / Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	TA	-25	–	+85	°C
VCC supply voltage	JS29F04G08AANB1 JS29F08G08CANB2 JS29F16G08FANB1	Vcc	2.7	3.3	3.6	V
Ground supply voltage		Vss	0	0	0	V

6.1 VCC Power Cycling

Intel® NAND Flash devices are designed to prevent data corruption during power transitions. VCC is internally monitored. When VCC goes below approximately 2.0V, PROGRAM and ERASE functions are disabled. WP# provides additional hardware protection. WP# should be kept at VIL during power cycling. When VCC reaches 2.5V, 10 ms should be allowed for the NAND Flash to initialize before executing any commands (see Figure 13 on page 20).

The RESET command must be issued to all CE#s after power-on. The device will be busy for a maximum of 1ms.

Figure 13. AC Waveforms During Power Transitions

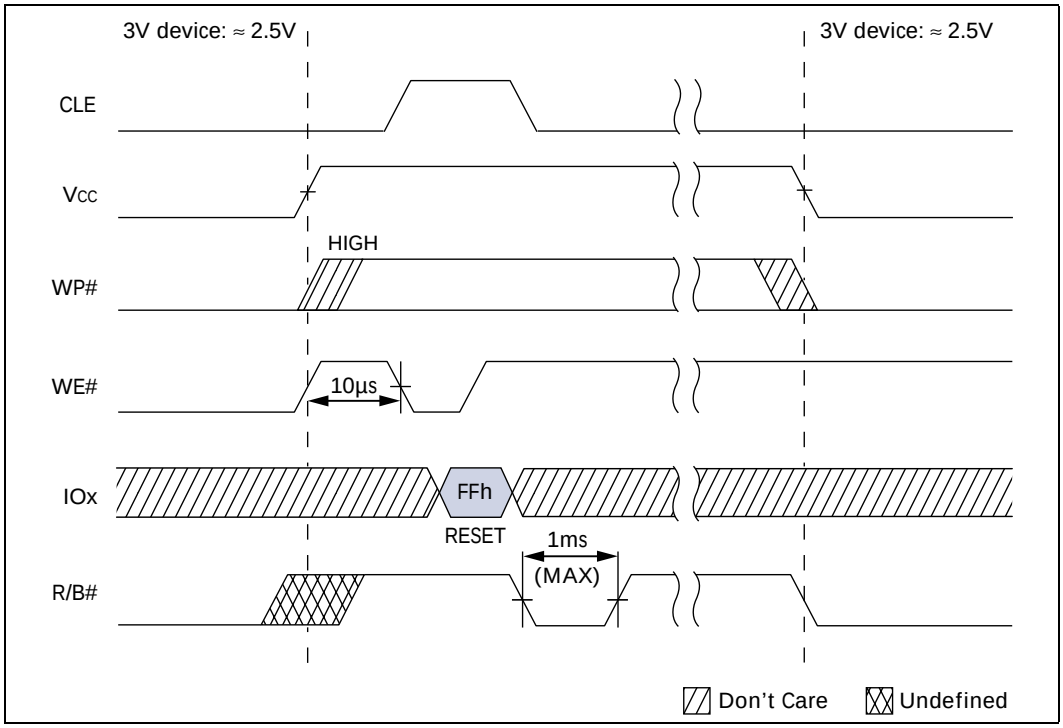


Table 8. 3V Device DC and Operating Characteristics (Sheet 1 of 2)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential read current	^{t}RC = 25ns, CE# = VIL, IOUT = 0mA	ICC1	—	25	35	mA	—
Program current	–	ICC2	—	25	35	mA	—
Erase current	–	ICC3	—	25	35	mA	—
Standby current (TTL)	CE# = VIH, WP# = 0V/VCC	ISB1	—	—	1	mA	— —
Standby current (CMOS)							
JS29F04G08AANB1 JS29F08G08CANB2 JS29F16G08FANB1	CE# = VCC – 0.2V, WP# = 0V/VCC	ISB2	— — —	10 20 40	50 100 200	µA µA µA	— — —
Input leakage current							
JS29F04G08AANB1 JS29F08G08CANB2 JS29F16G08FANB1	VIN = 0V to VCC	ILI	— — —	— — —	±10 ±20 ±40	µA µA µA	— — —
Output leakage current							
JS29F04G08AANB1 JS29F08G08CANB2 JS29F16G08FANB1	VOUT = 0V to VCC	ILO	— — —	— — —	±10 ±20 ±40	µA µA µA	— —

Table 8. 3V Device DC and Operating Characteristics (Sheet 2 of 2)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	I/O[7:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#	V_{IH}	0.8 x Vcc	–	V_{CC} + 0.3	V	—
Input low voltage (all inputs)	–	V_{IL}	–0.3	—	0.2 x Vcc	V	—
Output high voltage	I_{OH} = –400µA	V_{OH}	2.4	–	–	V	—
Output low voltage	I_{OL} = 2.1mA	V_{OL}	—	—	0.4	V	—
Output low current (R/B#)	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	—	mA	—

Table 9. Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Number of valid blocks	N_{VB}	JS29F04G08AANB1	4,016	4,096	Blocks	1, 2
		JS29F08G08CANB2	8,032	8,192		1, 2, 3
		JS29F16G08FANB1	16,064	16,384		1, 2, 4

Notes:
1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below Nvb during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid and does not require error correction up to 1,000 PROGRAM/ERASE cycles.
3. Each die will have a maximum of 80 invalid blocks.
4. Two die associated with each CE# will have a maximum of 160 invalid blocks. Each device has two CE# signals.

Table 10. Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input capacitance	C_{IN}	JS29F04G08AANB1	10	pF	1, 2
		JS29F08G08CANB2	20		
		JS29F16G08FANB1	40		
Input/output capacitance (I/O)	C_{IO}	JS29F04G08AANB1	10	pF	1, 2
		JS29F08G08CANB2	20		
		JS29F16G08FANB1	40		

Notes:
1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_c = 25°C; f = 1 MHz; VIN = 0V.

Table 11. Test Conditions

Parameter		Value	Notes
Input pulse levels	JS29F04G08AANB1 JS29F08G08CANB2 JS29F16G08FANB1	0.0V to Vcc	
Input rise and fall times		5ns	
Input and output timing levels		Vcc/2	
Output load		1 TTL GATE and CL = 50pF	1

Note:
1. Verified in device characterization; not 100 percent tested.

Table 12. AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	Cache Mode		Standard Mode		Unit	Notes
		Min	Max	Min	Max		
ALE to data start	^{t}ADL	70	–	70	–	ns	1
ALE hold time	^{t}ALH	10	–	5	–	ns	
ALE setup time	^{t}ALS	25	–	10	–	ns	
CE# hold time	^{t}CH	10	–	5	–	ns	
CLE hold time	^{t}CLH	10	–	5	–	ns	
CLE setup time	^{t}CLS	25	–	10	–	ns	
CE# setup time	^{t}CS	35	–	15	–	ns	
Data hold time	^{t}DH	10	–	5	–	ns	
Data setup time	^{t}DS	20	–	10	–	ns	
WRITE cycle time	^{t}WC	45	–	25	–	ns	
WE# pulse width HIGH	^{t}WH	15	–	10	–	ns	
WE# pulse width	^{t}WP	25	–	12	–	ns	
WP# setup time	^{t}WW	30	–	30	–	ns	

1. Timing for ^{t}ADL begins in the ADDRESS cycle on the final rising edge of WE# and ends with the first rising edge of WE# for data input.

Table 13. AC Characteristics: Normal Operation (Sheet 1 of 2)

Parameter	Symbol	Cache Mode		Standard Mode		Unit	Notes
		Min	Max	Min	Max		
ALE to RE# delay	^{t}AR	10	–	10	–	ns	—
CE# access time	^{t}CEA	–	45	–	25	ns	1
CE# HIGH to output High-Z	^{t}CHZ	–	45	–	30	ns	2
CLE to RE# delay	^{t}CLR	10	–	10	–	ns	—
CE# HIGH to output hold	^{t}COH	15	–	15	–	ns	—
Cache busy in page read cache mode (first 31h)	^{t}DCBSYR1	–	3	–	–	µs	—

Table 13. AC Characteristics: Normal Operation (Sheet 2 of 2)

Parameter	Symbol	Cache Mode		Standard Mode		Unit	Notes
		Min	Max	Min	Max		
Cache busy in page read cache mode (next 31h and 3Fh)	^{t}DCBSYR2	^{t}DCBSYR1	25	–	–	µs	—
Output High-Z to RE# LOW	^{t}IR	0	–	0	–	ns	1
Data transfer from Flash array to data register	^{t}R	–	25	–	25	µs	—
READ cycle time	^{t}RC	50	–	25	–	ns	1
RE# access time	^{t}REA	–	30	–	20	ns	1
RE# HIGH hold time	^{t}REH	15	–	10	–	ns	1
RE# HIGH to output hold	^{t}RHOH	22	–	22	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	100	–	ns	—
RE# HIGH to output High-Z	^{t}RHZ	–	100	–	100	ns	2
RE# LOW to output hold	^{t}RLOH	5	–	5	–	ns	
RE# pulse width	^{t}RP	25	–	12	–	ns	1
Ready to RE# LOW	^{t}RR	20	–	20	–	ns	—
Reset time (READ/PROGRAM/ ERASE/ Power-On)	^{t}RST	–	5/10/500	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	60	–	60	–	ns	—

Notes:
1. For PAGE READ CACHE MODE and PROGRAM PAGE CACHE MODE operations, the Cache Mode cache mode timing applies.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for maximum 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Table 14. PROGRAM / ERASE Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	—	4	Cycles	4
BLOCK ERASE operation time	tBERS	1.5	2	ms	
Busy time for PROGRAM CACHE operation	tCBSY	3	500	µs	1
Busy time for TWO-PLANE PROGRAM PAGE operation	tDBSY	0.5	1	µs	—
LAST PAGE PROGRAM operation time	tLPROG	—	—	–	2
Busy time for OTP DATA PROGRAM operation if OTP is protected	tOBSY	—	25	µs	—
PAGE PROGRAM operation time	tPROG	220	500	µs	3

Notes:
1. tCBSY MAX time depends on timing between internal program completion and data-in.
2. tLPROG = ^{t}PROG (last page) + tPROG (last – 1 page) – cmd load time (last page) – addr load time (last page) – data load time (last page).
3. Typical tPROG time may increase for two-plane operations.
4. Four total partial page programs to the same page.

7.0 Command Definitions

7.1 Command Definitions

Table 15. Command Set

Command	Command Cycle #1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle #2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	5
PAGE READ CACHE MODE	31h	–	No	–	No	2
PAGE READ CACHE MODE LAST	3Fh	–	No	–	No	2
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	3
RANDOM DATA READ	05h	2	No	E0h	No	4
READ ID	90h	1	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	5
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	3
RANDOM DATA INPUT	85h	2	Yes	–	No	6
BLOCK ERASE	60h	3	No	D0h	No	5
RESET	FFh	–	No	–	Yes	
OTP DATA PROGRAM	A0h	5	Yes	10h	No	
OTP DATA PROTECT	A5h	5	No	10h	No	
OTP DATA READ	AFh	5	No	30h	No	

Notes:
1. Indicates required data cycles between command cycle 1 and command cycle 2.
2. Do not cross block address boundaries when using PAGE READ CACHE MODE operations.
3. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE. See Table 2 and 3 on page 9 for plane address boundary definitions.
4. RANDOM DATA READ command limited to use within a single page.
5. These commands are valid during busy when performing an interleaved die operation. See Section 7.7, “Two-Plane Operations” on page 38 for additional details.
6. RANDOM DATA INPUT command limited to use within a single page.

Table 16. Two-Plane Command Set

Command	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Command Cycle 3	Valid During Busy	Notes
TWO-PLANE PAGE READ	00h	5	00h	5	30h	No	
TWO-PLANE READ for INTERNAL DATA MOVE	00h	5	00h	5	35h	No	1
TWO-PLANE RANDOM DATA READ	06h	5	E0h	–	–	No	2
TWO-PLANE/MULTIPLE-DIE READ STATUS	78h	3	–	–	–	Yes	3
TWO-PLANE PROGRAM PAGE	80h	5	11h-80h or 11h-81h	5	10h	No	4
TWO-PLANE PROGRAM PAGE CACHE MODE	80h	5	11h-80h or 11h-81h	5	15h	No	4
TWO-PLANE PROGRAM for INTERNAL DATA MOVE	85h	5	11h-80h or 11h-81h	5	10h	No	1
TWO-PLANE BLOCK ERASE	60h	3	60h	3	D0h	No	4

Notes:
1. Do not cross plane address boundaries when using TWO-PLANE READ for INTERNAL DATA MOVE and TWO-PLANE PROGRAM for INTERNAL DATA MOVE. See Table 2 on page 9, and Table 3 on page 10 for plane address boundary definitions.
2. TWO-PLANE/MULTIPLE-DIE RANDOM DATA READ command is limited to use within a single page.
3. The TWO-PLANE/MULTIPLE-DIE READ STATUS command can be used to check status with two-plane and multiple-die operations, excluding the TWO-PLANE PAGE READ (00h-00h- 30h) command.
4. These commands are valid during busy when performing interleaved die operations. See "Interleaved Die Operations" on page 48 for additional details.

7.2 READ Operations

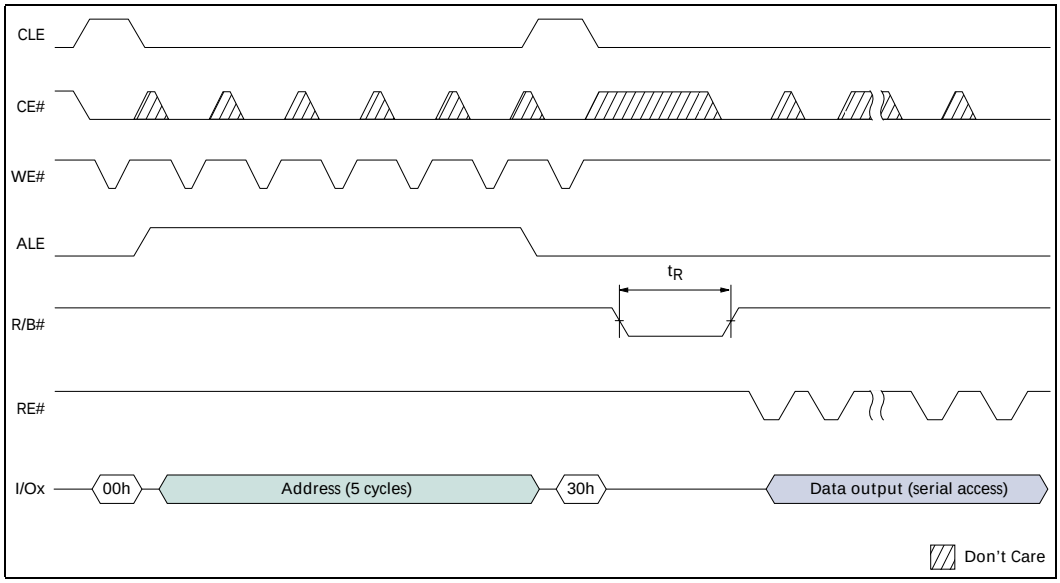
7.2.1 PAGE READ 00h–30h

On initial power up, each device defaults to read mode. To enter the read mode while in operation, write the 00h command to the command register then write five ADDRESS cycles, then conclude with the 30h command.

To determine the progress of the data transfer from the NAND Flash array to the data register (^{t}R), monitor the R/B# signal; or alternately, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must re-issue the READ (00h) command to receive data output from the data register. See Figure 64, "PAGE READ CACHE MODE Operation, Part 1 of 2" on page 63 and Figure 65, "PAGE READ CACHE MODE Operation, Part 2 of 2" on page 63 for examples. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate (see Figure 14).

Figure 14. PAGE READ Operation



7.2.2 RANDOM DATA READ 05h–E0h

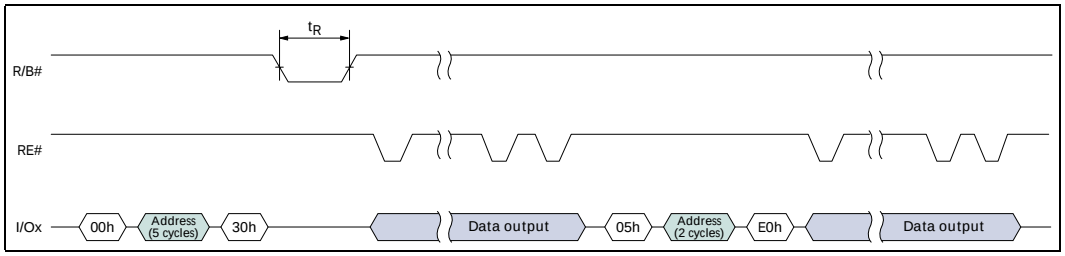
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h) sequence.

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (two cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially (see Figure 15 on page 26).

Figure 15. Random Data Read Operation



7.2.3 PAGE READ CACHE MODE START 31h; PAGE READ CACHE MODE START LAST 3Fh

Intel® NAND Flash devices have a cache register that can be used to increase READ operation speed when accessing sequential pages in a block.

First, issue a normal PAGE READ (00h–30h) command sequence. See Figure 16 on page 27 for operation details. The R/B# signal goes LOW for ^{t}R during the time it takes to transfer the first page of data from the memory to the data register. After R/B# returns to HIGH, the PAGE READ CACHE MODE START (31h) command is latched into

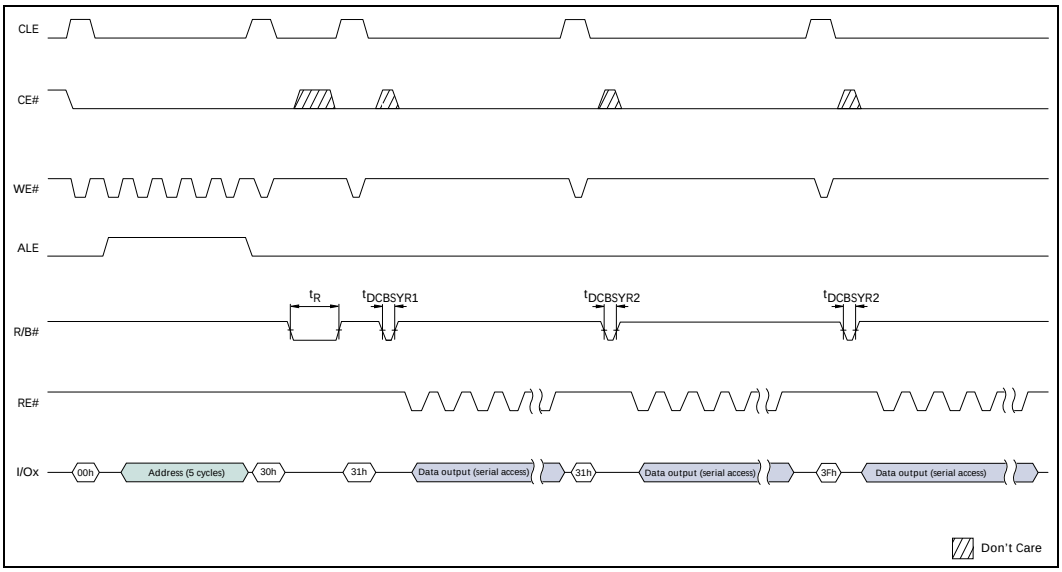
the command register. R/B# goes LOW for ^{t}DCBSYR1 while data is being transferred from the data register to the cache register. After the data register contents are transferred to the cache register, another PAGE READ is automatically started as part of the 31h command. Data is transferred from the next sequential page of the memory array to the data register during the same time data is being read serially (pulsing RE#) from the cache register. If the total time to output data exceeds ^{t}R, then the PAGE READ is hidden.

The second and subsequent pages of data are transferred to the cache register by issuing additional 31h commands. R/B# will stay LOW up to ^{t}DCBSYR2. This time can vary, depending on whether the previous memory-to-data-register transfer was completed prior to issuing the next 31h command. See Table 13 on page 22 for timing parameters. If the data transfer from memory to the data register is not completed before the 31h command is issued, R/B# stays LOW until the transfer is complete.

It is not necessary to output a whole page of data before issuing another 31h command. R/B# will stay LOW until the previous PAGE READ is complete and the data has been transferred to the cache register.

To read out the last page of data, the PAGE READ CACHE MODE START LAST (3Fh) command is issued. This command transfers data from the data register to the cache register without issuing another PAGE READ (see Figure 16 on page 27).

Figure 16. PAGE READ CACHE MODE

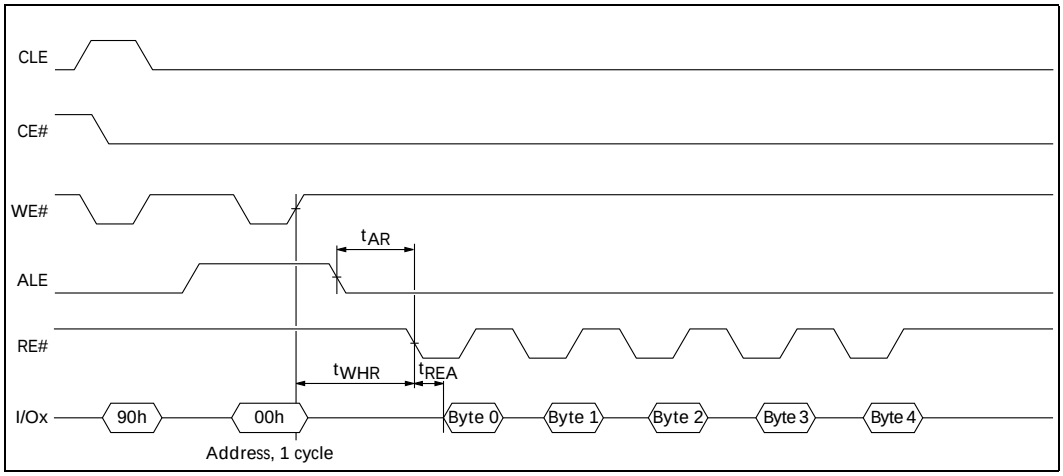


7.2.4 READ ID 90h

The READ ID command is used to read the 5 bytes of identifier code programmed into the Intel® SD74 NAND Flash Memory devices. The READ ID command reads a 5-byte table that includes manufacturer ID, device configuration, and part-specific Table 17, “Device ID and Configuration Codes” on page 29).

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued (see Figure 17).

Figure 17. READ ID Operation



Note: See Table 17 on page 29 for byte definitions.

Table 17. Device ID and Configuration Codes

	Options	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	Value[1]	Notes
Byte 0	Manufacturer ID										
	Intel	0	0	1	0	1	1	0	0	2Ch	
Byte 1	Device ID										
JS29F04G08AANB1	4Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	
JS29F08G08CANB2	8Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	2
JS29F16G08FANB1	16Gb, x8, 3V	1	1	0	1	0	0	1	1	D3h	
Byte 2											
Number of die per CE	1							0	0	00b	
	2							0	1	01b	
Cell type	SLC					0	0			00b	
Number of simultaneously programmed pages	2			0	1					01b	
Interleaved operations between multiple die	Not supported		0							0b	
	Supported		1							1b	
Cache programming	Supported	1								1b	
Byte value	JS29F04G08AANB1	1	0	0	1	0	0	0	0	90h	
	JS29F08G08CANB2	1	0	0	1	0	0	0	0	90h	2
	JS29F16G08FANB1	1	1	0	1	0	0	0	1	D1h	
Byte 3											
Page size	2KB							0	1	01b	
Spare area size (bytes)	64B						1			1b	
Block size (w/o spare)	128KB			0	1					01b	
Organization	x8		0							0b	
Serial access (MIN)	25ns	1				0				1xxx0b	
Byte value	8-bit bus width	1	0	0	1	0	1	0	1	95h	
Byte 4											
Reserved								0	0	00b	
Planes per CE#	2					0	1			01b	
	4					1	0			10b	
Plane size	2Gb		1	0	1					101b	
Reserved		0								0b	
Byte value	JS29F04G08AANB1	0	1	0	1	0	1	0	0	54h	
	JS29F08G08CANB2	0	1	0	1	0	1	0	0	54h	2
	JS29F16G08FANB1	0	1	0	1	1	0	0	0	58h	2

Notes:
1. b = binary; h = hex.
2. The JS29F08G08CANB2 device ID code reflects the configuration of each 4Gb section.

7.2.5 READ STATUS 70h

These NAND Flash devices have an 8-bit status register that the software can read during device operation. Table 18 describes the status register.

After a READ STATUS command, all READ cycles will be from the status register until a new command is issued. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ STATUS cycle to see these changes.

In devices that have more than one die sharing a common CE# pin, the READ STATUS (70h) command reports the status of the die that was last addressed. If interleaved operations are started on both die, then the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command must be used to select the die that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as both die will respond until the next operation is issued.

While monitoring the status register to determine when the ^{t}R (transfer from NAND Flash array to data register) is complete, the user must re-issue the READ (00h) command to make the change from status to read mode. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

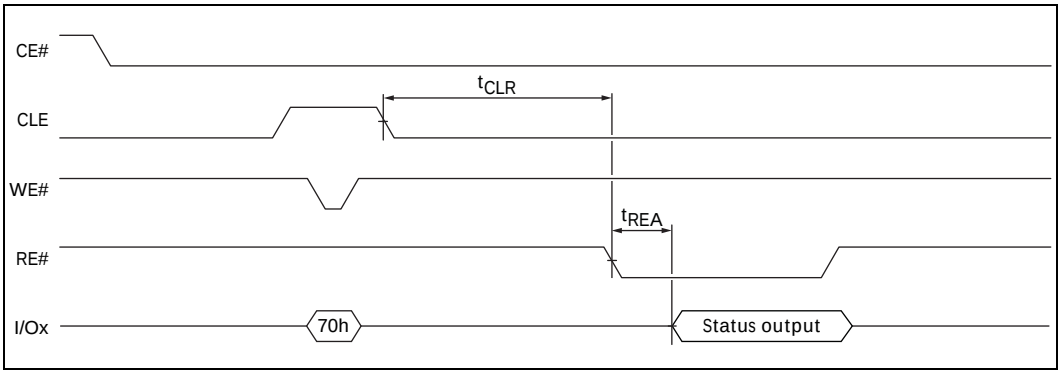
Table 18. Status Register Bit Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0[1]	Pass/fail	Pass/fail (N)	–	–	Pass/fail	"0" = Successful PROGRAM/ ERASE "1" = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	"0" = Successful PROGRAM "1" = Error in PROGRAM
2	–	–	–	–	–	"0"
3	–	–	–	–	–	"0"
4	–	–	–	–	–	"0"
5	Ready/busy	Ready/ busy[2]	Ready/busy	Ready/ busy[2]	Ready/busy	"0" = Busy "1" = Ready
6	Ready/busy	Ready/busy cache[3]	Ready/busy	Ready/busy cache[3]	Ready/busy	"0" = Busy "1" = Ready
7	Write protect	Write protect	Write protect	Write protect	Write protect	"0" = Protected "1" = Not protected

Notes:

1. Status register bit 0 reports a "1" if a TWO-PLANE PROGRAM operation fails on one or both planes. Status register bit 1 reports a "1" if a TWO-PLANE PROGRAM PAGE CACHE MODE operation fails on one or both planes. Use TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) to determine the plane to which the operation failed
2. Status register bit 5 is "0" during the actual programming operation. If cache mode is used, this bit will be "1" when all internal operations are complete.
3. Status register bit 6 is "1" when the cache is ready to accept new data. R/B# follows bit 6. See Figure 21, "PROGRAM PAGE CACHE MODE Example" on page 33 and Figure 74, "PROGRAM PAGE CACHE MODE Operation Ending on 15h" on page 67.

Figure 18. Status Register Operation



7.3 PROGRAM Operations

7.3.1 PROGRAM PAGE 80h–10h

Intel® NAND Flash devices are inherently page-programmed devices. Pages must be programmed consecutively within a block, from the least significant page address to most significant page address (i.e., 0, 1, 2, …, 63). Random page address programming is prohibited.

Intel® NAND Flash devices also support partial-page programming operations. This means that any single bit can be programmed only one time before an erase is required; however, the page can be partitioned such that a maximum of four programming operations are supported before an erase is required.

7.3.2 SERIAL DATA INPUT 80h

PROGRAM PAGE operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by five ADDRESS cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address. The PROGRAM (10h) command is written after the data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects “1s” that are not successfully written to “0s.”

R/B# goes LOW for the duration of array programming time, ^{t}PROG. The READ STATUS (70h) **command** and the RESET (FFh) command are the only commands valid during the programming operation. Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the program operation passed or failed (see Figure 19). The command register stays in read status register mode until another valid command is written to it.

7.3.3 RANDOM DATA INPUT 85h

After the initial data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command. See Figure 20 for the proper command sequence.

Figure 19. PROGRAM and READ STATUS Operation

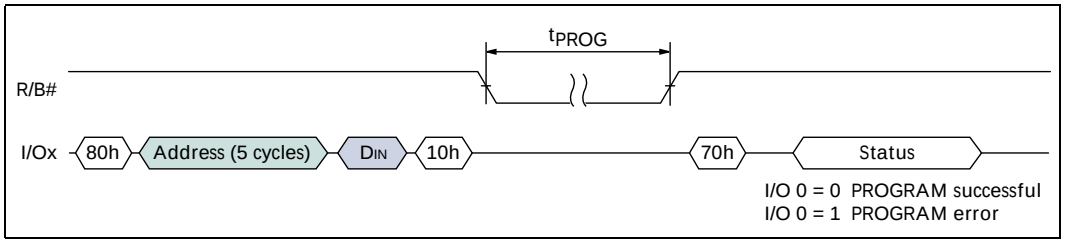
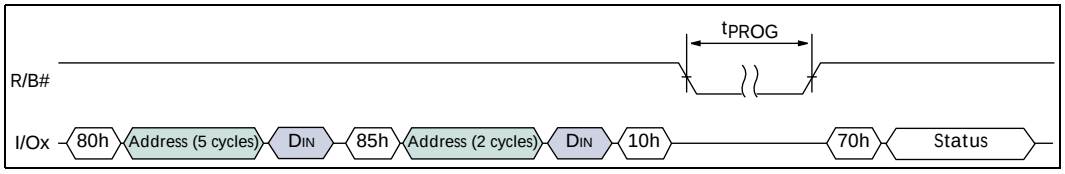


Figure 20. RANDOM DATA INPUT



7.3.4 PROGRAM PAGE CACHE MODE 80h–15h

Cache programming is actually a buffered programming mode of the standard PROGRAM PAGE command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by five cycles of address, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE PROGRAM (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array.

The PROGRAM PAGE CACHE MODE command can cross block address boundaries; it must not cross die address boundaries. RANDOM DATA INPUT (85h) commands are permitted with PROGRAM PAGE CACHE MODE operations.

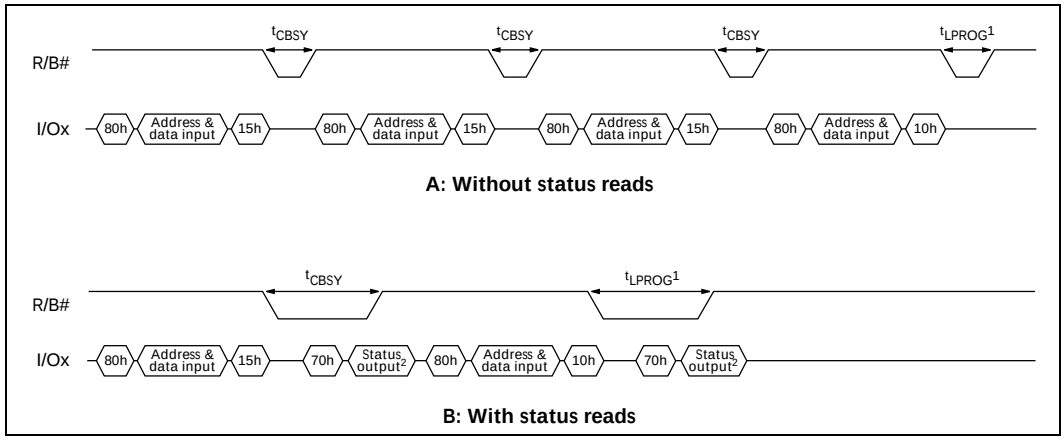
Bit 6 (Cache R/B#) of the status register can be read by issuing the READ STATUS (70h) command to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6.

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

If just the R/B# pin is used to determine programming completion, the last page of the program sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete (see Figure 21).

Bit 0 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a “1” (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a “1” (ready state) (as shown in Figure 21.)

Figure 21. PROGRAM PAGE CACHE MODE Example



Notes:
1. See Note 3, Table 14, "PROGRAM/ERASE Characteristics" on page 23.
2. Check I/O[6:5] for internal Ready/Busy. Check I/O[1:0] for pass/fail status. RE# can stay LOW or pulse multiple times after a 70h command.

7.4 Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. *Data moves are only supported within the plane from which data is read. Moving data from odd to even blocks, from even to odd blocks, and across die boundaries is prohibited.*

7.4.1 READ FOR INTERNAL DATA MOVE 00h–35h

The READ for INTERNAL DATA MOVE (00h-35h) command is used in conjunction with the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. First, 00h is written to the command register, then the internal source address is written (five cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

The written column addresses are ignored even though all five ADDRESS cycles are required.

The memory device is now ready to accept the PROGRAM for INTERNAL DATA MOVE command. Please refer to the description of this command in the following section.

7.4.2 PROGRAM for INTERNAL DATA MOVE 85h–10h

After the READ for INTERNAL DATA MOVE (00h-35h) command has been issued and R/B# goes HIGH, the PROGRAM for INTERNAL DATA MOVE (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register and programming of the new destination page begins. The sequence: 85h, destination address (five cycles), then 10h, is written to the device. After 10h is written, R/B# goes LOW while the control logic automatically programs the new page. The READ STATUS command can be used instead of the R/B# line to determine when the write is complete. Status register bit 6 = "1," bit 0 of the status register indicates if the operation was successful.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for INTERNAL DATA MOVE command sequence to modify one or more bytes of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data are transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h (see Figure 22 and Figure 23 starting on page 34).

Because INTERNAL DATA MOVE operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using INTERNAL DATA MOVE operations also use a robust ECC scheme that can correct two or more bits per sector.

Figure 22. INTERNAL DATA MOVE

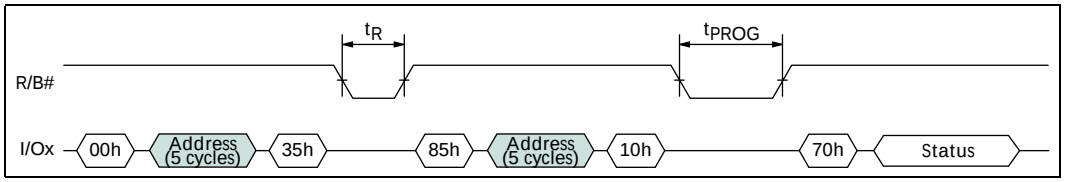
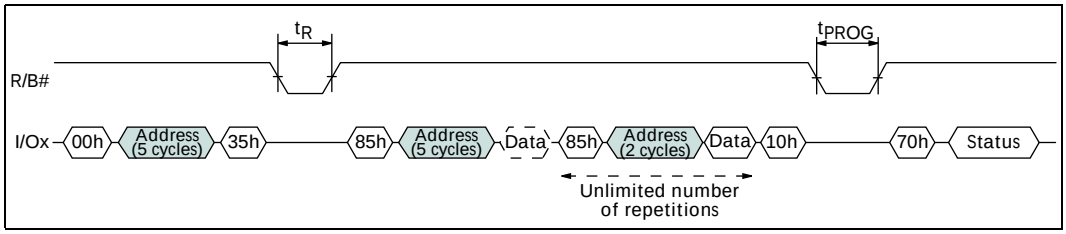


Figure 23. INTERNAL DATA MOVE with RANDOM DATA INPUT



7.5 BLOCK ERASE Operation

7.5.1 BLOCK ERASE 60h–D0h

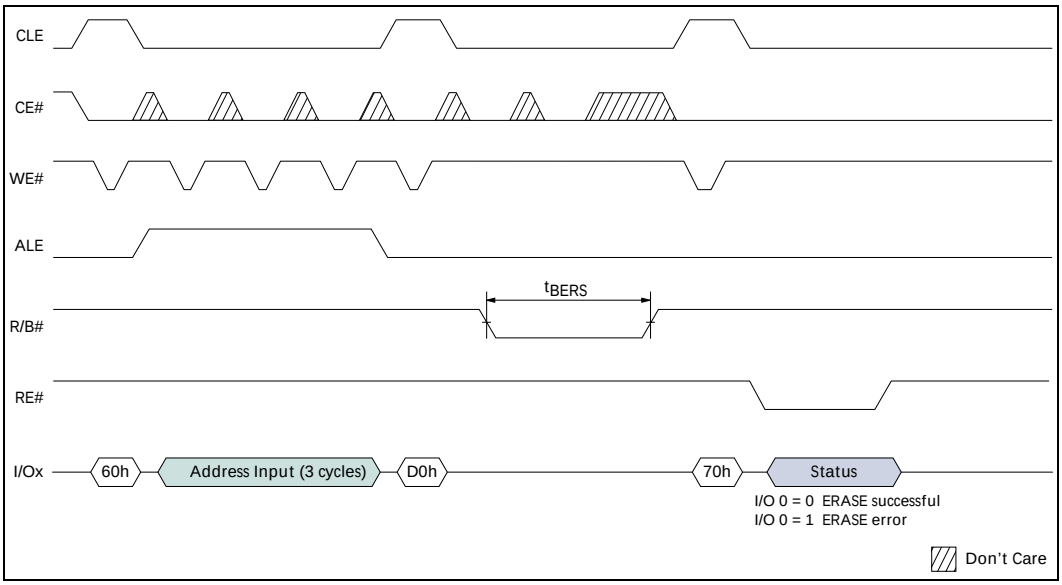
Erasing occurs at the block level. For example, the JS29F04G08AANB1 device has 4,096 erase blocks, organized into 64 pages per block, 2,112 bytes per page (2,048 + 64 bytes). Each block is 132K bytes (128K + 4K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 24 on page 35).

Three cycles of addresses BA[18:6] and PA[5:0]are required. Although page addresses PA[5:0] are loaded, they are a “Don’t Care” and are ignored for BLOCK ERASE operations. See Figure 2 on page 8 for addressing details.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then three cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS (70h) command can be used to check the status of the BLOCK ERASE operation. When bit 6 = “1” the ERASE operation is complete. Bit 0 indicates a pass/fail condition where “0” = pass (see Figure 24 on page 35, and Table 18 on page 30).

Figure 24.Block Erase Operation



7.6 One-Time Programmable (OTP) Area

This Intel® NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (2,112 bytes per page) of OTP data is available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Intel® NAND Flash devices, the OTP area leaves the factory in a non-written state (all bits are “1s”). Programming or partial-page programming enables the user to program only “0” bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as “one-time programmable,” Intel provides a unique way to program and verify data—before permanently protecting it and preventing future changes.

OTP programming and protection are accomplished in two discrete operations. First, using the OTP DATA PROGRAM (A0h-10h) command, an OTP page is programmed entirely in one operation, or in up to four partial-page programming sequences. Programming can occur on other pages within the OTP area in a similar manner. Second, the OTP area is permanently protected from further programming using the OTP DATA PROTECT (A5h-10h) command. The pages within the OTP area can always be read using the OTP DATA READ (AFh-30h) command, whether or not it is protected.

To determine whether or not the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited during and following OTP operations.

7.6.1 OTP DATA PROGRAM A0h-10h

The OTP DATA PROGRAM (A0h-10h) command is used to write data to the pages within the OTP area. An entire page can be programmed at one time, or a page can be partially programmed up to four times. There is no ERASE operation for the OTP pages.

The OTP DATA PROGRAM enables programming into an offset of an OTP page, using the two bytes of column address (CA[11:0]). The command is not compatible with the RANDOM DATA INPUT (85h) command. The OTP DATA PROGRAM command will not execute if the OTP area has been protected.

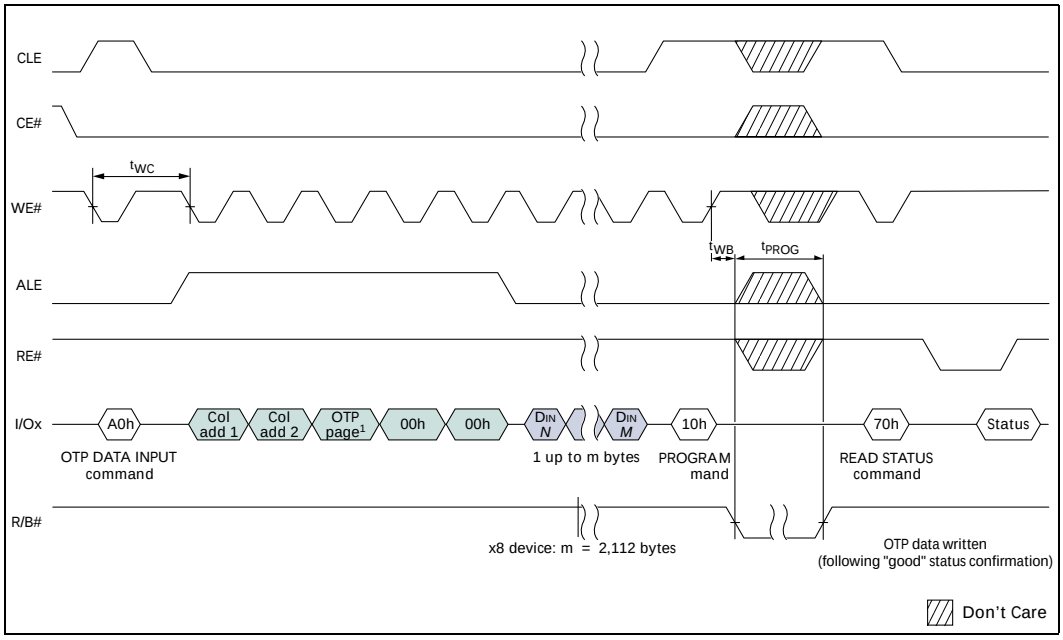
To use the OTP DATA PROGRAM command, issue the A0h command. Issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Next, write from 1 to 2,112 bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification. Program verification only detects “1s” that are not successfully written to “0s.”

R/B# goes LOW during the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only command valid during the OTP DATA PROGRAM operation. Bit 5 of the status register will reflect the state of R/B#. If bit 7 is “0,” then the OTP area has been protected; otherwise, it will be a “1.”

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 18 on page 30).

It is possible to program each OTP page a maximum of four times.

Figure 25. OTP DATA PROGRAM



Note: The OTP page must be within the 02h–0Bh range.

7.6.2 OTP DATA PROTECT A5h-10h

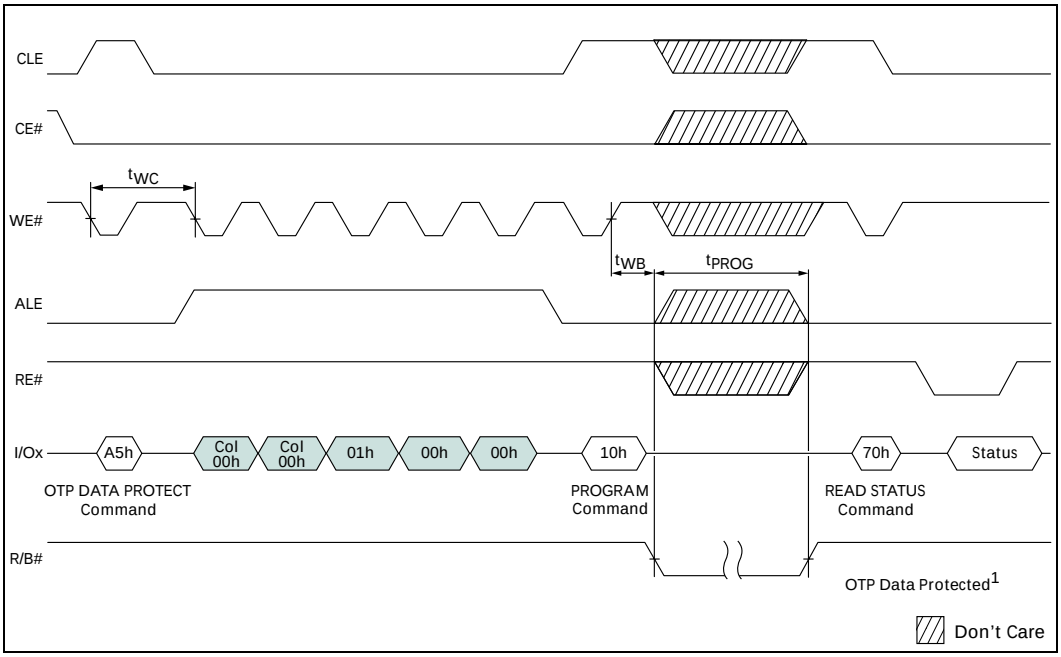
The OTP DATA PROTECT (A5h-10h) command is used to protect all the data in the OTP area. After the data is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the OTP DATA PROTECT command, issue the A5h command. Next, issue the following five ADDRESS cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

R/B# goes LOW while the OTP area is being protected. The protect command duration is similar to a normal page programming operation, ^{t}PROG. The READ STATUS (70h) command is the only command valid during the OTP DATA PROTECT operation. Bit 5 of the status register will reflect the state of R/B#.

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 18, “Status Register Bit Definition” on page 30).

Figure 26. OTP DATA PROTECT



Note: OTP data is protected following “good” status confirmation.

7.6.3 OTP DATA READ AFh-30h

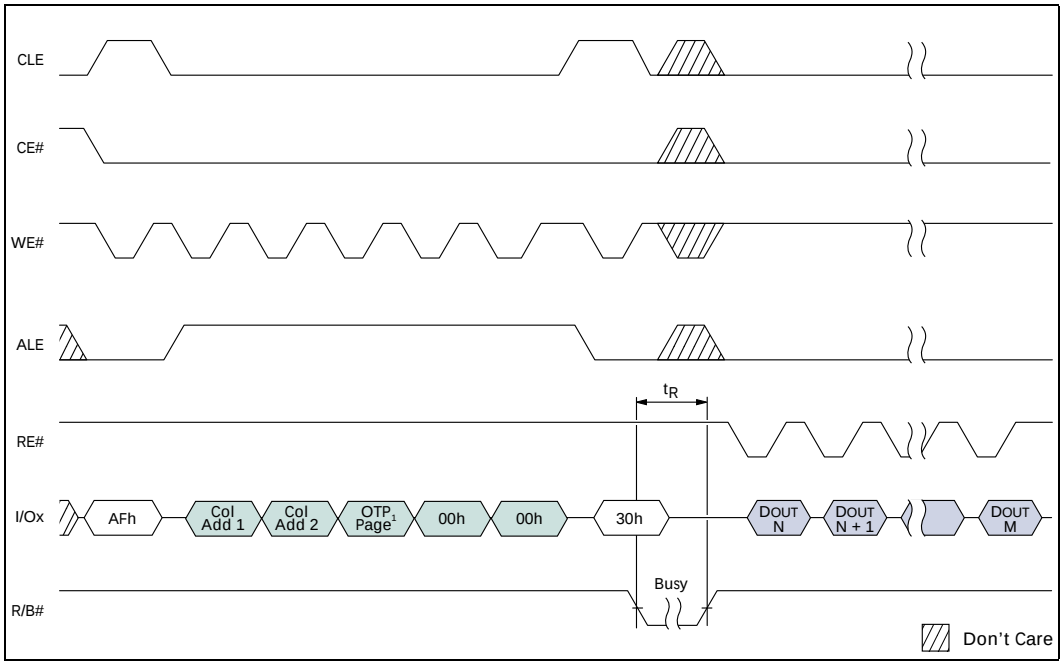
The OTP DATA READ (AFh-30h) command is used to read data from a page within the OTP area. An OTP page within the OTP area is available for reading data whether or not the area is protected.

To use the OTP DATA READ command, issue the AFh command. Next, issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Finally, issue the 30h command.

R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the OTP DATA READ operation. Bit 5 of the status register will reflect the state of R/B#. For details, refer to Table 18 on page 30.

Normal READ operation timings apply to OTP read accesses (see Figure). Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

Figure 27. OTP DATA READ Operation



Note: The OTP page must be within the 02h–0Bh range.

7.7 Two-Plane Operations

This NAND Flash device is divided into two physical planes. Each plane contains a 2,112-byte data register, a 2,112-byte cache register, and a 2,048-block NAND Flash array. Two-plane commands make better use of the Flash arrays on these physical planes by performing PROGRAM, READ, or ERASE operations simultaneously, significantly improving system performance.

7.7.1 TWO-PLANE Addressing

Two-plane commands require two addresses, one address per plane. These two addresses are subject to the following requirements:

- The least significant block address bit, BA6, must be different for the two addresses.
- The most significant block address bit, BA18 for 16Gb devices, must be identical for both addresses.
- The page address bits, PA[5:0], must be identical for both addresses.

7.7.2 TWO-PLANE PAGE READ 00h-00h-30h

The TWO-PLANE PAGE READ (00h-00h-30h) operation is similar to the PAGE READ (00h-30h) operation. It transfers two pages of data from the NAND Flash array to the data registers. Each page must be from a different plane on the same die.

To enter the TWO-PLANE PAGE READ mode, write the 00h command to the command register, then write five ADDRESS cycles for plane 0 (BA6 = “0”). Next, write the 00h command to the command register, then write five ADDRESS cycles for plane 1 (BA6 = “1”). Finally, issue the 30h command. The first-plane and second-plane addresses must meet the two-plane addressing requirements, and in addition, they must have identical column addresses.

After the 30h command is written, page data is transferred from both planes to their respective data registers in ^{t}R. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# goes HIGH. To read out the data from the plane 0 data register, pulse RE# repeatedly. After the data cycle from the plane 0 address completes, issue a TWO-PLANE/MULTIPLE-DIE RANDOM DATA READ (06h-E0h) command to select the plane 1 address, then repeatedly pulse RE# to read out the data from the plane 1 data register.

Alternately, the READ STATUS (70h) command can monitor the data transfers. When the transfers are complete, status register bit 6 is set to “1.” To read data from the first of the two planes, the user must first issue the TWO-PLANE RANDOM DATA READ (06h-E0h) command and pulse RE# repeatedly. When the data cycle is complete, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the other plane. To output the data beginning at the specified column address, pulse RE# repeatedly.

Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited during and following a TWO-PLANE PAGE READ operation.

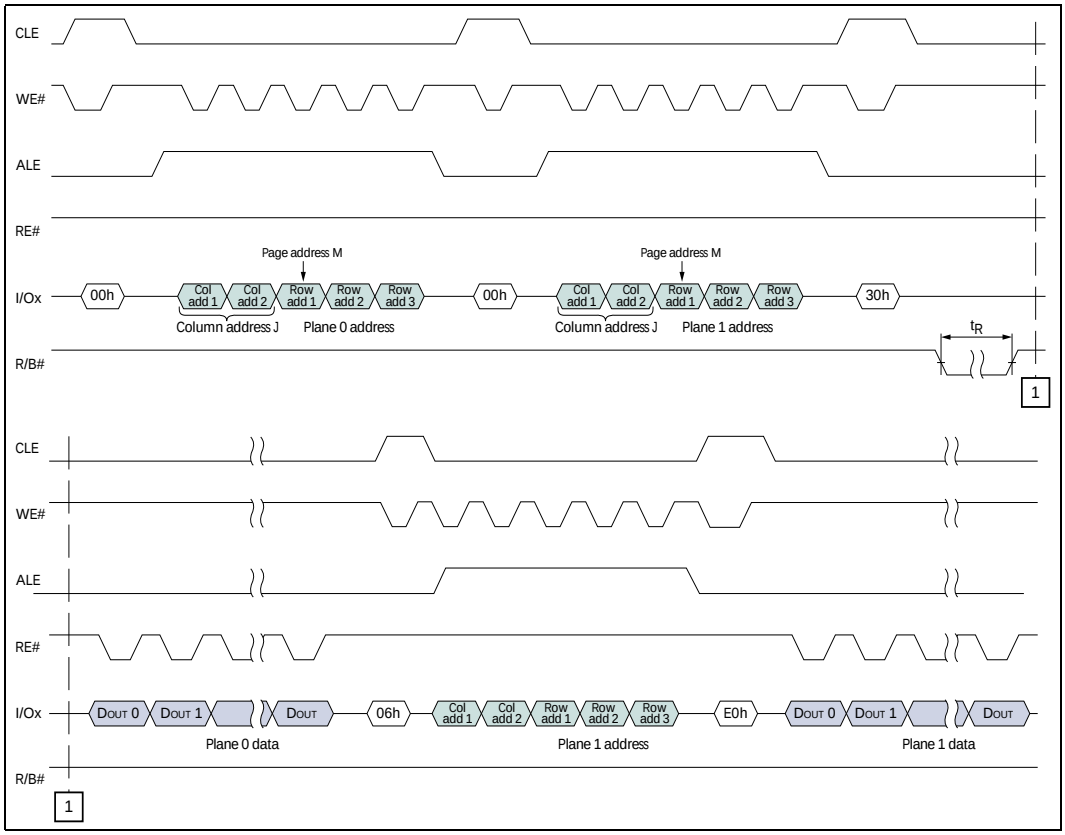
7.7.3 TWO-PLANE/MULTIPLE-DIE RANDOM DATA READ 06h-E0h

The TWO-PLANE RANDOM DATA READ (06h-E0h) command is similar to the RANDOM DATA READ (05h-E0h) command, except that it requires five ADDRESS cycles rather than two. The command selects a die and plane and a column address from which to read data after a TWO-PLANE PAGE READ (00h-00h-30h) command, and during or after an interleaved PAGE READ operation (see Section 7.8, “Interleaved Die Operations” on page 48

To issue a TWO-PLANE RANDOM DATA READ command, issue the 06h command, then five ADDRESS cycles, and follow with the E0h command. Pulse RE# repeatedly to read data from the new plane, beginning at the specified column address.

The primary purpose of the TWO-PLANE RANDOM DATA READ command is to select a new die and plane and a column address within that die and plane. If a new die and plane do not need to be selected, then it is possible to use the RANDOM DATA READ (05h-E0h) command instead (see Table 7.2.2, “RANDOM DATA READ 05h–E0h” on page 26).

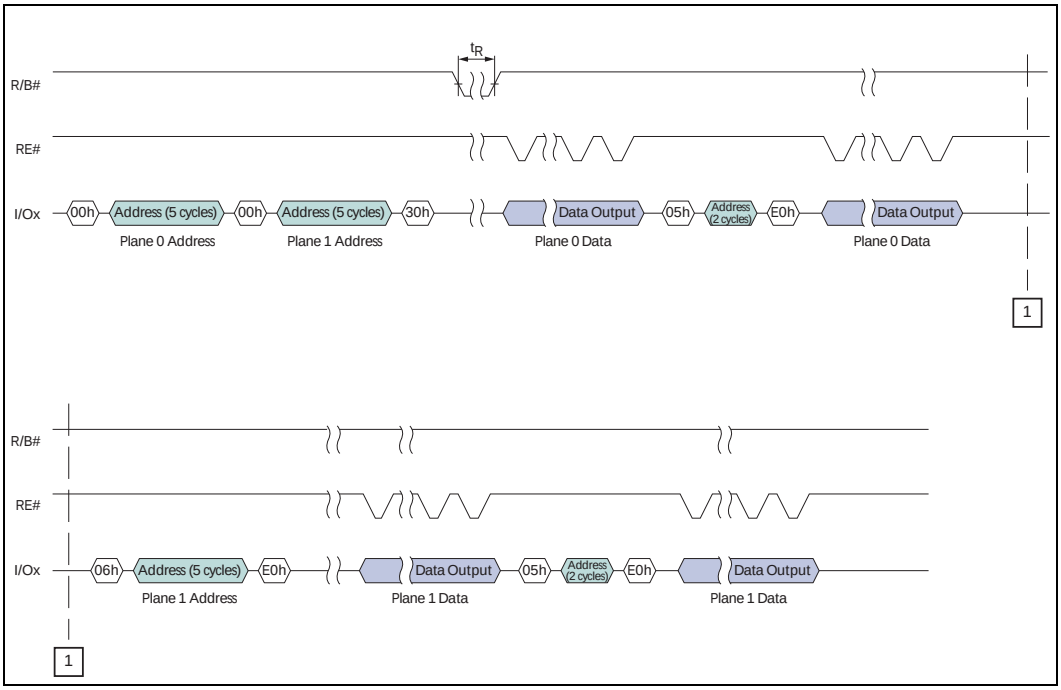
Figure 28. TWO-PLANE PAGE READ



Notes:

1. Column and page addresses must be the same.
2. The least significant block address bit, BA6, must not be the same for the first and second plane addresses.

Figure 29. TWO-PLANE PAGE READ with RANDOM DATA READ



7.7.4 TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h or 80h-11h-81h-10h

The TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h or 80h-11h-81h-10h) operation is similar to the PROGRAM PAGE (80h-10h) operation. It programs two pages of data from the data registers to the Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to most significant page address. Random page programming within a block is prohibited. The first plane address and the second plane address must meet the two-plane addressing requirements (see "TWO-PLANE Addressing" on page 38).

To begin the TWO-PLANE PROGRAM PAGE operation, write the 80h command to the command register; write five ADDRESS cycles for the first plane; then write the data. Serial data is loaded on consecutive WE# cycles starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h) and RESET (FFh).

After ^{t}DBSY, write the 80h (or 81h) command to the command register; write five ADDRESS cycles for the second plane; then write the data. The PROGRAM (10h) command is written after the second-plane data input is complete.

After the 10h command is written, the control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operations to both planes. WRITE verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of the array programming time (t_{PROG}). When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during t_{PROG} are READ STATUS (70h), TWO-PLANE/ MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

When the device is ready, if the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = "1"), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

During serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane. For details on this command, see Section 7.3.3, "RANDOM DATA INPUT 85h" on page 31. Figure 30 shows TWO-PLANE PROGRAM PAGE operation.

Figure 30. TWO-PLANE PROGRAM PAGE

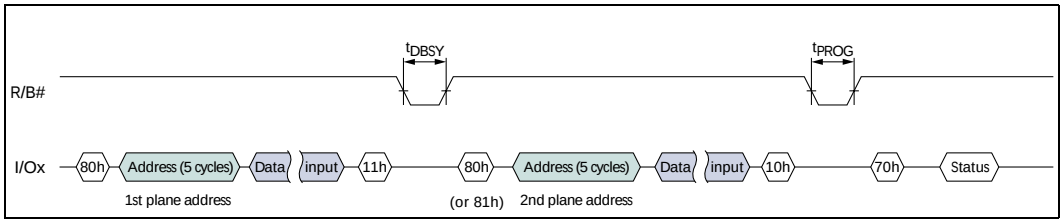
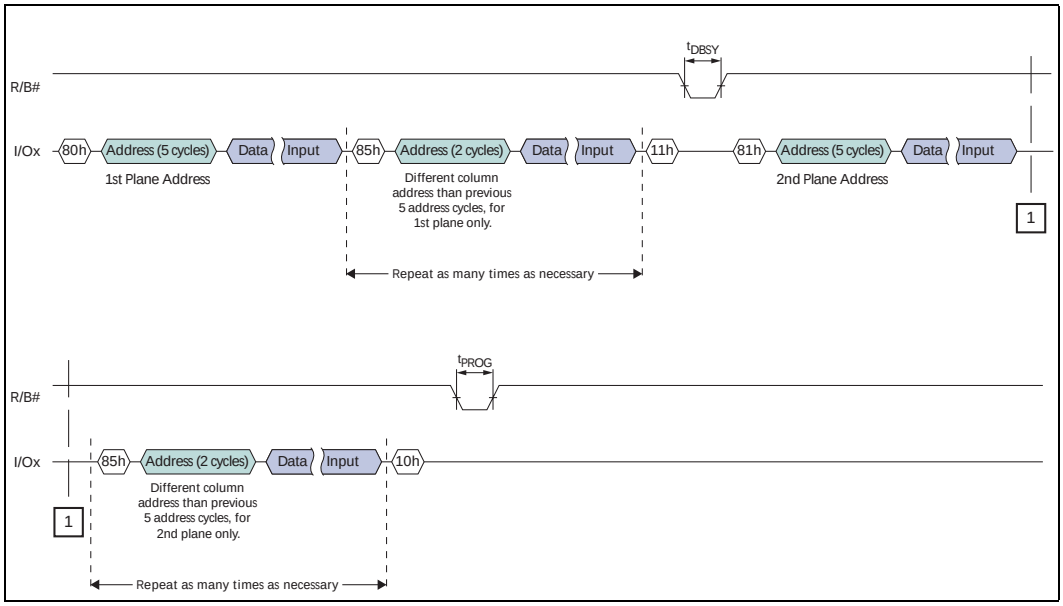


Figure 31. TWO-PLANE PROGRAM PAGE with RANDOM DATA INPUT



7.7.5 TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h or 80h-11h-81h-15h

The TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h or 80h-11h-81h-15h) operation is similar to the PROGRAM PAGE CACHE MODE (80h-15h) operation. It programs two pages of data from the data registers to the NAND Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to the most significant page address. Random page programming within a block is prohibited. The first plane and second plane addresses must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 38).

To enter the two-plane program page cache mode, write the 80h command to the command register, write five ADDRESS cycles for the first plane, then write the data. Serial data is loaded on consecutive WE# cycles starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for tDBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during tDBSY are READ STATUS (70h) and RESET (FFh).

After tDBSY, write the 80h (or 81h) command to the command register, write five ADDRESS cycles for the second plane, then write the data. The CACHE WRITE (15h) command is written after the second-plane data input is complete. Data is transferred from the cache registers to the data registers on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data registers and R/B# returns HIGH, memory array programming to both planes begins.

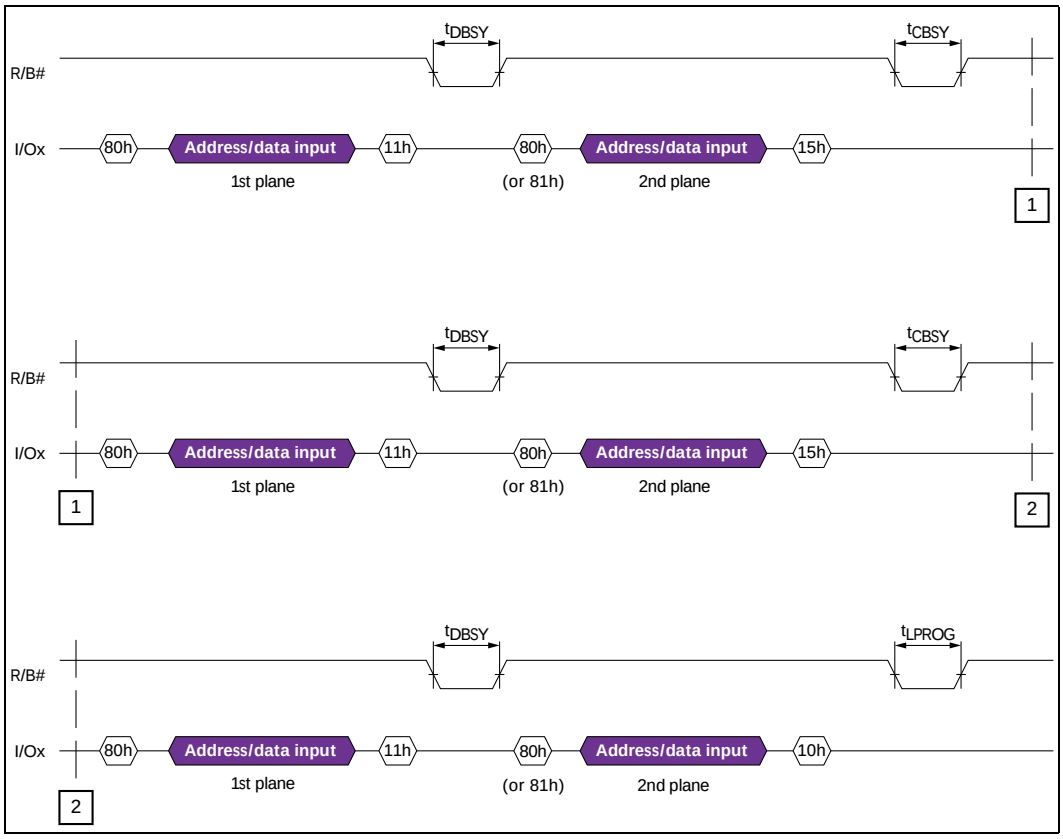
When R/B# returns HIGH, new data can be written to the cache registers by issuing another TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h or 80h-11h-81h-15h) sequence. The time that R/B# stays LOW (tCBSY) is determined by the actual programming time of the previous operation. For the first cache operation, the duration of tCBSY is the time it takes for the data to be copied from the cache registers to the data registers. On the second and subsequent TWO-PLANE PROGRAM PAGE CACHE MODE operations, transfer from the cache registers to the data registers is delayed until the current data register contents have been programmed into the arrays.

If the R/B# pin is used to determine programming completion, the last operation of the program sequence must use the TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h or 80h-11h-81h-10h) command instead of the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h or 80h-11h-81h-15h) command. If the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h or 80h-11h-81h-15h) command is used for the last operation, then use READ STATUS (70h) to monitor the operation progress; status register bit 5 indicates when programming is complete. See Table 13 on page 36 for details of the status register.

To determine when the current TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-10h or 80h-11h-81h-10h) operation has completed, issue the READ STATUS (70h) command and check status register bits 5 and 6. When the device is ready, use status register bit 0 to determine if the current operation passed and status register bit 1 to determine if the previous operation passed. If either bit 0 or bit 1 = "1," indicating a failed operation, then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which current or previous plane operation failed. For more information on status register bit definitions, see Table 18 on page 30.

During the serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane. For details on this command, see Section 7.3.3, “RANDOM DATA INPUT 85h” on page 31. See Figure 32 on page 44 for an example.

Figure 32. TWO-PLANE PROGRAM PAGE CACHE MODE



7.7.6 TWO-PLANE INTERNAL DATA MOVE 00h-00h-35h/85h-11h-80h-10h

A TWO-PLANE INTERNAL DATA MOVE operation is similar to an INTERNAL DATA MOVE operation, and requires two sequences. Issue a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command first, then the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command. Data moves are only supported within the planes from which data is read. The first plane and second plane addresses must meet the two-plane addressing requirements for both the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) and TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) commands (see “Two-Plane Addressing” on page 38).

7.7.7 TWO-PLANE READ for INTERNAL DATA MOVE 00h-00h-35h

The TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is used in conjunction with the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command. First, write 00h to the command register, then write the first plane internal source address (five cycles). Again, write 00h to the command register, followed by the second-plane internal source address (five cycles). Finally, write 35h to the command register. After the 35h command, R/B# goes LOW for ^{t}R while two pages are read into their respective cache registers.

The memory device is now ready to accept the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command.

7.7.8 TWO-PLANE PROGRAM for INTERNAL DATA MOVE 85h-11h-80h-10h or 85h-11h-81h-10h

After the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command has been issued and R/B# goes HIGH (or the status register bit 6 is “1”), the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h or 85h-11h-81h-10h) command is used. Pages must be read from and programmed to the same plane.

First, write 85h to the command register, then write the first plane destination address (five cycles), then write 11h to the command register. The 11h command is a “dummy” command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to “1.” The only valid commands during ^{t}DBSY are READ STATUS (70h) and RESET (FFh).

After ^{t}DBSY, write the 80h (or 81h) command to the command register, then write the second plane destination address (five cycles), then write 10h to the command register. Data is transferred from the cache registers to the data registers on the rising edge of WE#, and programming begins on both planes.

R/B# goes LOW for the duration of array programming time, ^{t}PROG. When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to “1.” The only valid commands during ^{t}PROG are READ STATUS (70h), TWO-PLANE/ MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = “1”), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

During the serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane. For details on this command, see Section 7.3.3, “RANDOM DATA INPUT 85h” on page 31. See Figure 33 on page 45 for an example.

Figure 33. TWO-PLANE INTERNAL DATA MOVE

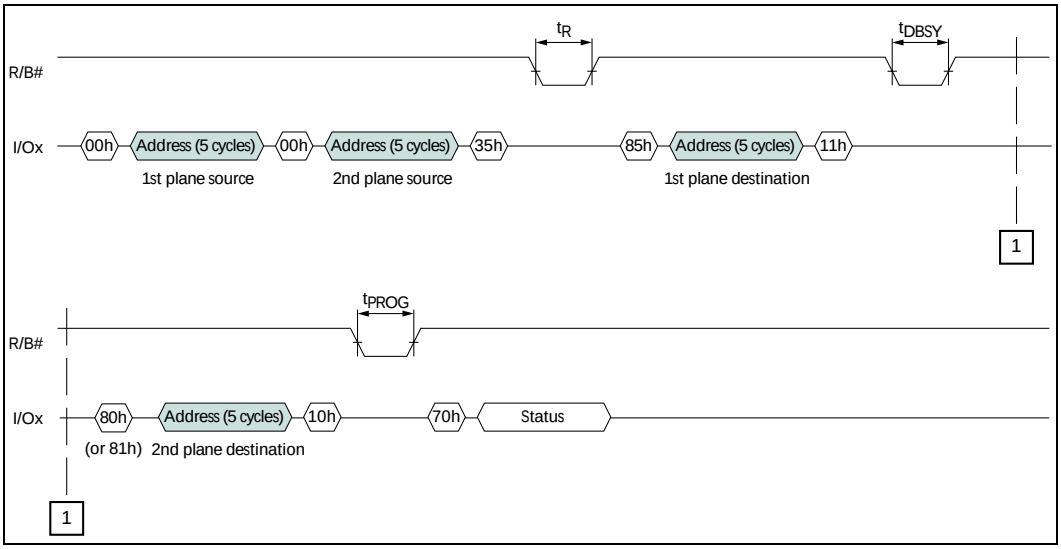
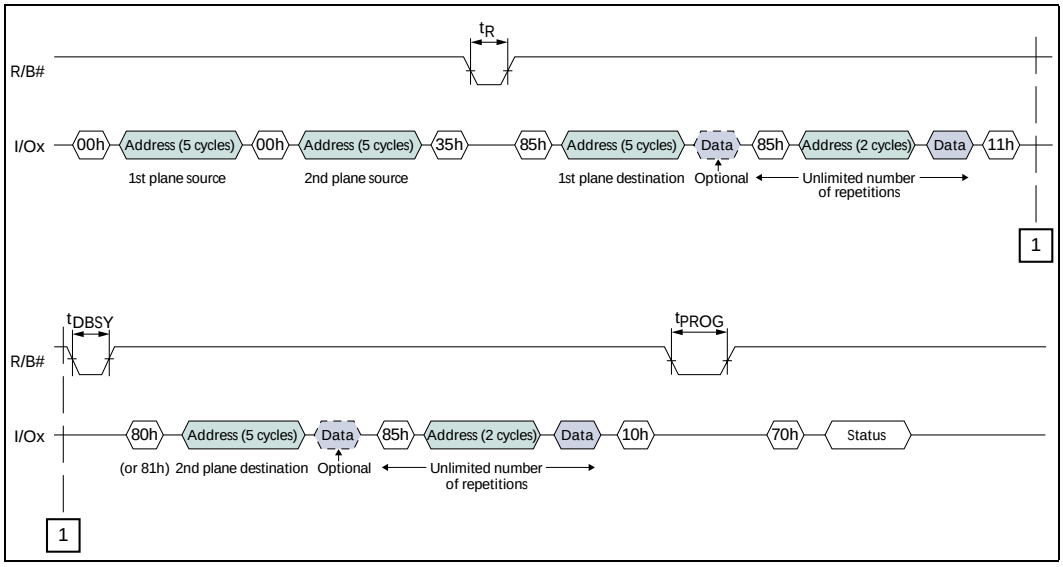


Figure 34. TWO-PLANE INTERNAL DATA MOVE with RANDOM DATA INPUT



7.7.9 TWO-PLANE BLOCK ERASE 60h-60h-D0h

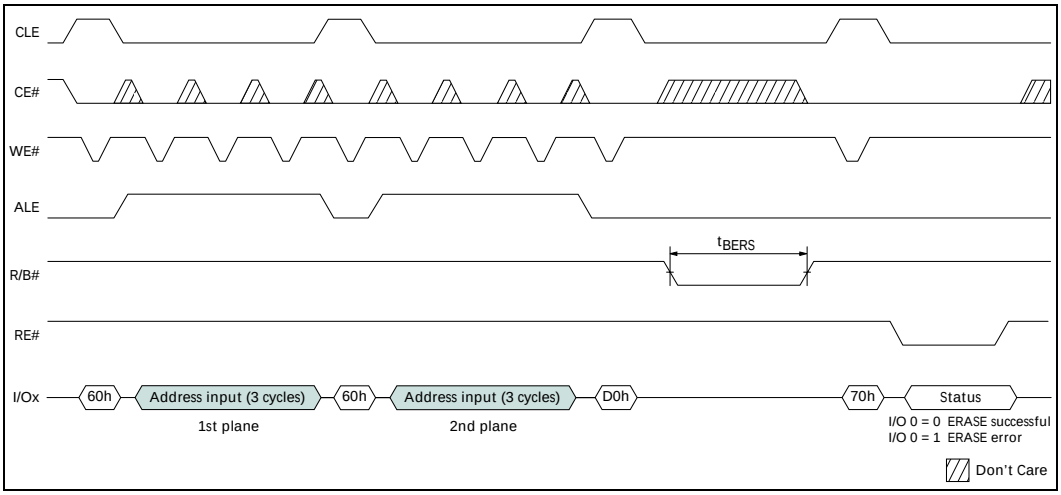
The TWO-PLANE BLOCK ERASE (60h-60h-D0h) operation is similar to the BLOCK ERASE (60h-D0h) operation. It erases two blocks instead of one. The blocks to be erased must be on different planes on the same die. The first plane and second plane addresses must meet the two-plane addressing requirements (see "TWO-PLANE Addressing" on page 38). Additionally, the page addresses, PA[5:0], for both planes must be LOW.

Begin a TWO-PLANE BLOCK ERASE operation by writing 60h to the command register, followed by three ADDRESS cycles of the first plane block address. Then write 60h again to the command register, followed by three ADDRESS cycles of the second-plane block address. Finally, issue the D0h command.

R/B# goes LOW for the duration of block erase time, ^{t}BERS. When block erase is complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}BERS are READ STATUS (70h), TWO-PLANE/MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = "1"), then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

Figure 35. TWO-PLANE BLOCK ERASE Operation



7.7.10 TWO-PLANE/MULTIPLE-DIE READ STATUS 78h

In Intel® NAND Flash devices that have two planes, and possibly more than one die in a package that share the same CE# pin, it is possible to independently poll the status register of a particular plane and die using the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command. This command can be used to check the status register during and after two-plane operations (with the exception of TWO-PLANE PAGE READ), and to check the status of interleaved die operations.

After the 78h command is issued, the device requires three ADDRESS cycles containing the block and page addresses, BA[18:6] and PA[5:0]. The most significant block address bit in the third ADDRESS cycle, BA18, selects the proper die, and the least significant block address bit in the first ADDRESS cycle, BA6, selects the proper plane within that die.

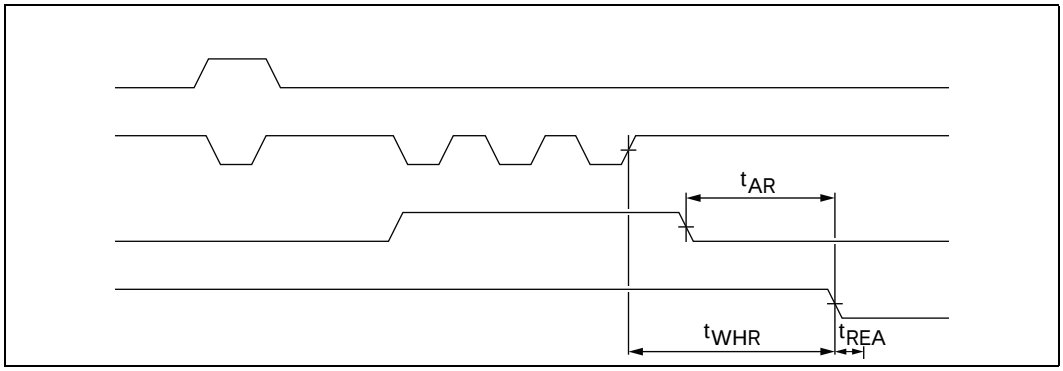
After the 78h command and the three ADDRESS cycles, the status register is output on I/O[7:0] when RE# is LOW. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to issue a new TWO-PLANE/MULTIPLE-DIE READ STATUS command to see these changes. The status register bit definitions are identical to those reported by the READ STATUS (70h) command (see Table 18, "Status Register Bit Definition" on page 30).

In devices that have more than one die sharing a common CE# pin, when one die is not busy (status register bit 5 is "1"), it is possible to initiate a new operation to that die even if the other die is busy (see Section 7.8, "Interleaved Die Operations" on page 48).

If both die are busy during or following an interleaved die operation, the READ STATUS (70h) command must not be used to check status, as both die will respond, causing bus contention on I/O[7:0]. The TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is required to check status during and after interleaved die operations.

Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited during and following power-on RESET and OTP commands.

Figure 36. TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle



7.8 Interleaved Die Operations

In devices that have more than one die sharing a common CE# pin, it is possible to significantly improve performance by interleaving operations between the die. When both die are idle (R/B# is HIGH or status register bit 5 is “1”), issue a command to the first die (BA18 = “0”). Then, while the first die is busy (R/B# is LOW), issue a command to the other die (BA18 = “1”).

There are two ways to verify operation completion in each die: using the R/B# signal, or monitoring the status register. R/B# remains LOW while either die is busy. When R/B# goes HIGH, then both die are idle and the operations are complete. Alternatively, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command can report the status of each die individually. If a die is performing a cache operation, like PROGRAM PAGE CACHE MODE (80h-15h) or TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h), then the die is able to accept the data for another cache operation when status register bit 6 is “1.” All operations, including cache operations, are complete on a die when status register bit 5 is “1.”

During and following interleaved die operations, the READ STATUS (70h) command is prohibited. Instead, use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command. This command selects which die will report status. Interleaved two-plane commands must also meet the requirements in “TWO-PLANE Addressing” on page 38.

PROGRAM PAGE, PROGRAM PAGE CACHE MODE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, BLOCK ERASE, and TWO-PLANE BLOCK ERASE can be used as interleaved operations on separate die that share a common CE#.

7.8.1 Interleaved PROGRAM PAGE Operations

Figure 37 on page 49 and Figure 38 on page 49 show how to perform two types of interleaved PROGRAM PAGE operations. In Figure 37, the R/B# signal is monitored for operation completion. In Figure 38, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE operations.

Figure 37. Interleaved PROGRAM PAGE with R/B# Monitoring

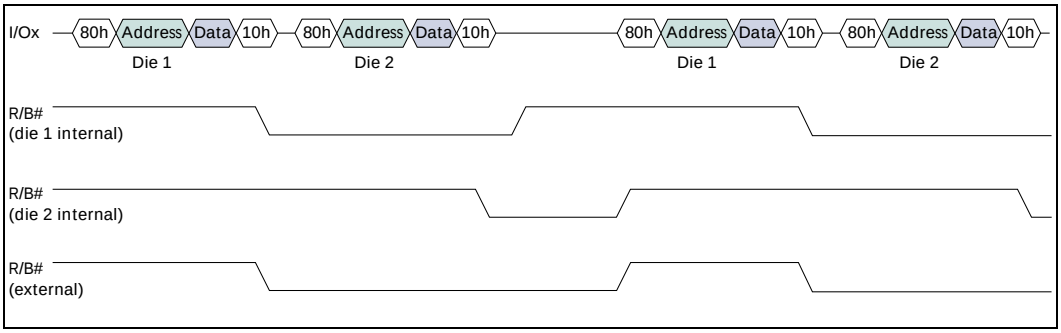
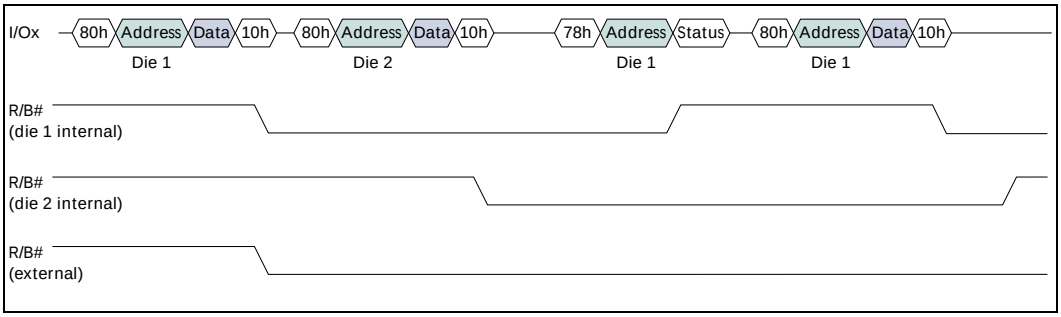


Figure 38. Interleaved PROGRAM PAGE with Status Register Monitoring



7.8.2 Interleaved PROGRAM PAGE CACHE MODE Operations

Figure 37 and Figure 38 show how to perform two types of interleaved PROGRAM PAGE CACHE MODE operations. In Figure 37, the R/B# signal is monitored. In Figure 38, the status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE CACHE MODE operations.

Figure 39. Interleaved PROGRAM PAGE CACHE MODE with R/B# Monitoring

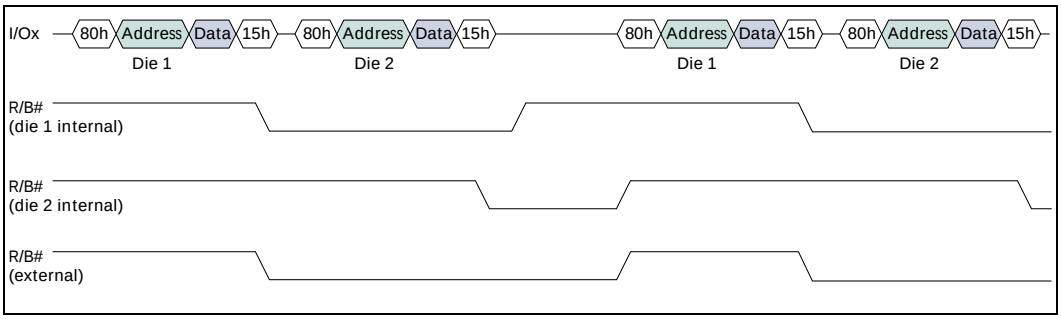
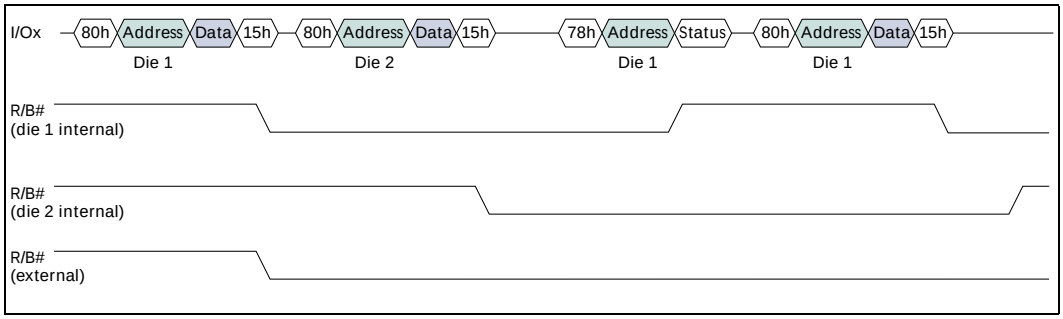


Figure 40. Interleaved PROGRAM PAGE CACHE MODE with Status Register Monitoring



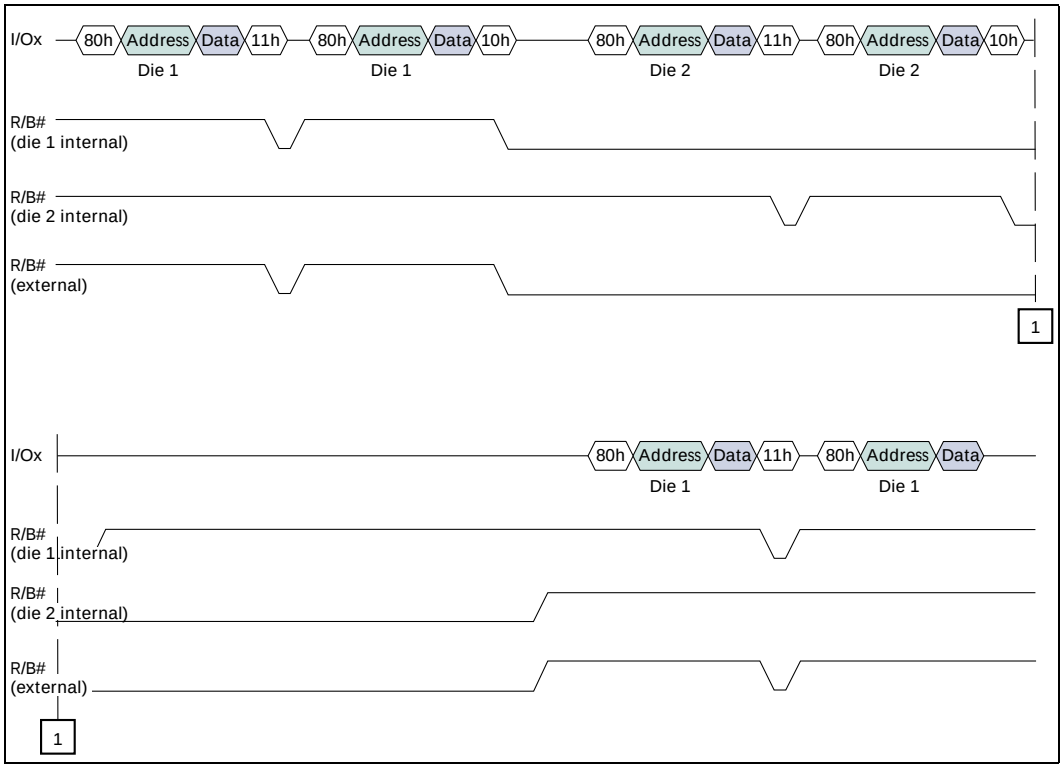
7.8.3 Interleaved TWO-PLANE PROGRAM PAGE Operations

Figure 41 and Figure 42 show how to perform two types of interleaved TWO-PLANE PROGRAM PAGE operations. In Figure 41, the R/B# signal is monitored for operation completion. In Figure 42, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE PROGRAM PAGE operation must meet two-plane addressing requirements. See Section 7.7.1, “TWO-PLANE Addressing” on page 38 for details.

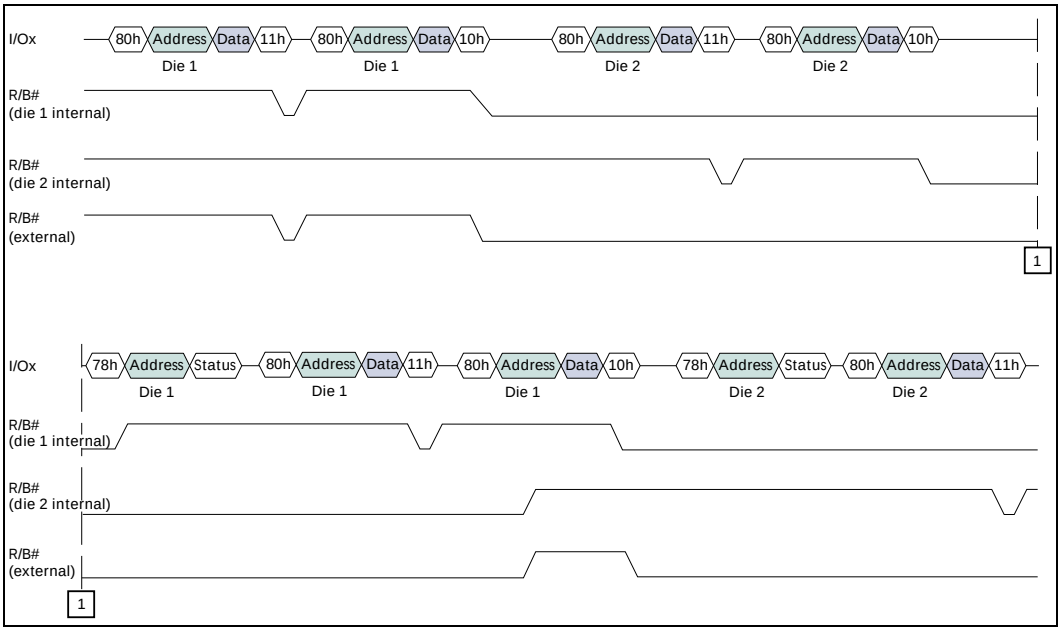
RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE operations.

Figure 41. Interleaved TWO-PLANE PROGRAM PAGE with R/B# Monitoring



Note: Two-plane addressing requirements apply.

Figure 42. Interleaved TWO-PLANE PROGRAM PAGE with Status Register Monitoring



Note: Two-plane addressing requirements apply.

7.8.4 Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE Operations

Figure 43 and Figure 44 show how to perform two types of interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations. In Figure 43, the R/B# signal is monitored. In Figure 44, the status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

The interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operation must meet two-plane addressing requirements. See Section 7.7.1, “TWO-PLANE Addressing” on page 38 for details.

RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations.

Figure 43. Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE with R/B# Monitoring

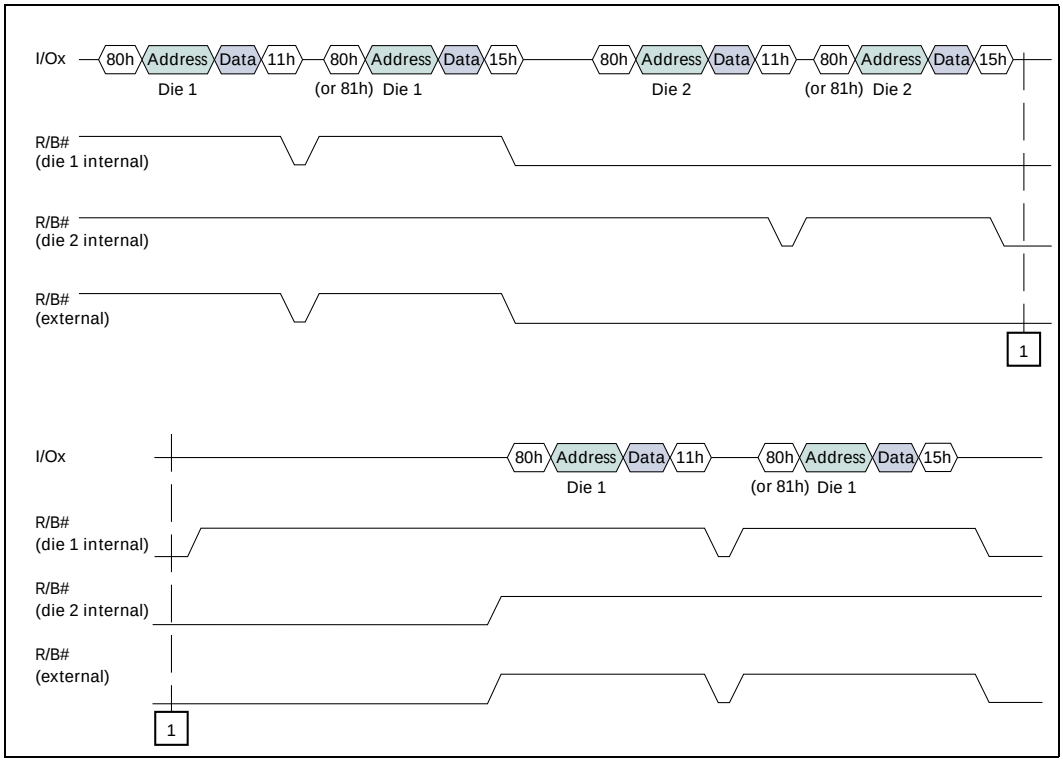
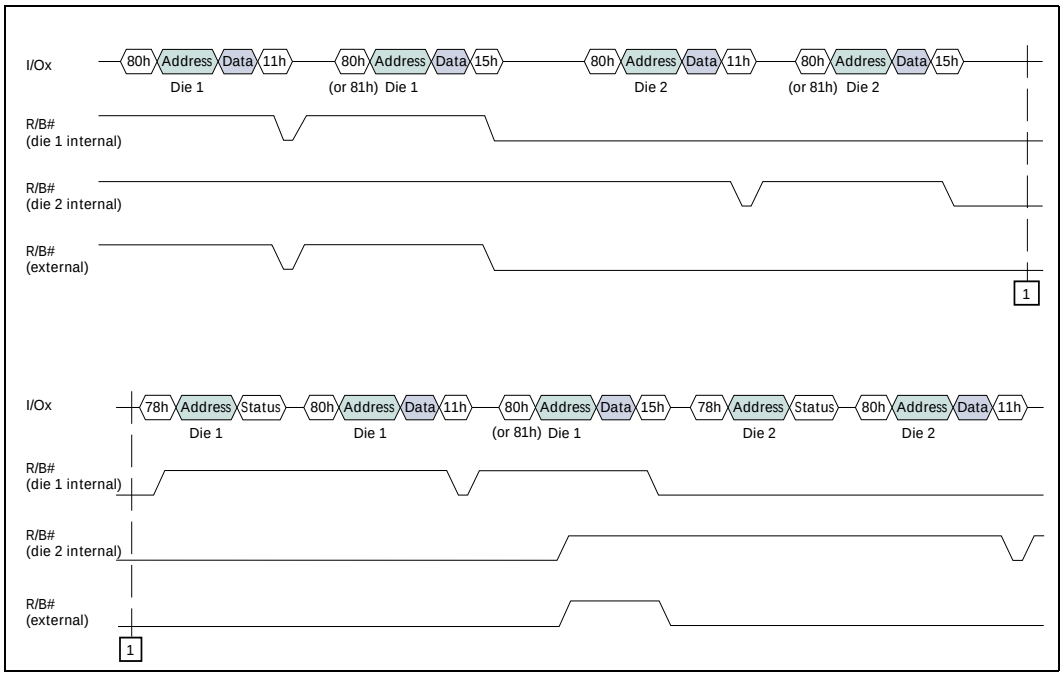


Figure 44. Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE with Status Register Monitoring



Note: Two-plane addressing requirements apply.

7.8.5 Interleaved BLOCK ERASE Operations

Figure 45 and Figure 46 show how to perform two types of interleaved BLOCK ERASE operations. In Figure 45, the R/B# signal is monitored for operation completion. In Figure 46, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

Figure 45. Interleaved BLOCK ERASE with R/B# Monitoring

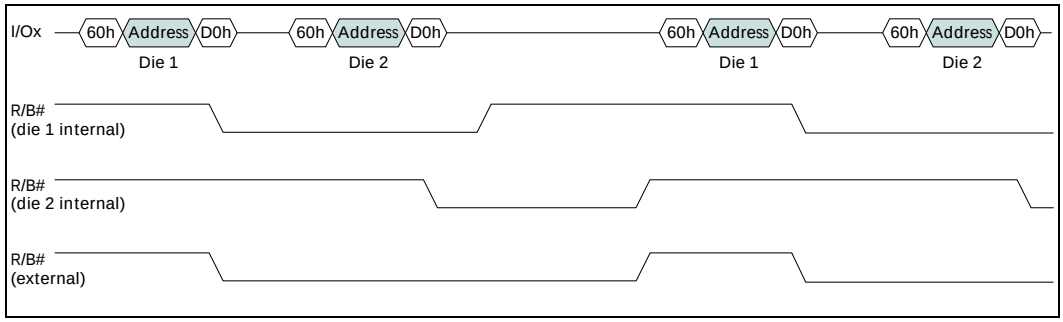
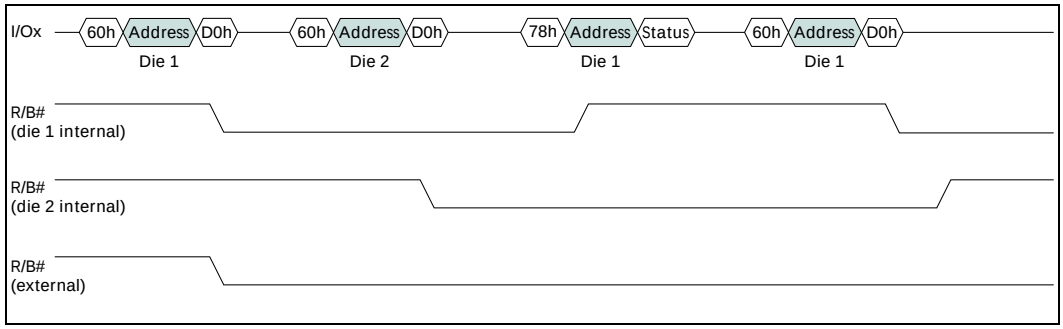


Figure 46. Interleaved BLOCK ERASE with Status Register Monitoring

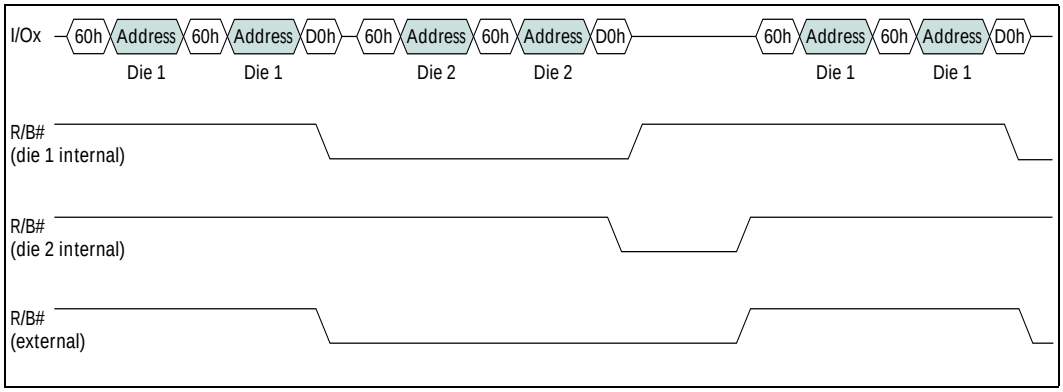


7.8.6 Interleaved TWO-PLANE BLOCK ERASE Operations

Figure 47 and Figure 48 show how to perform two types of interleaved BLOCK ERASE operations. In Figure 47, the R/B# signal is monitored for operation completion. In Figure 48, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

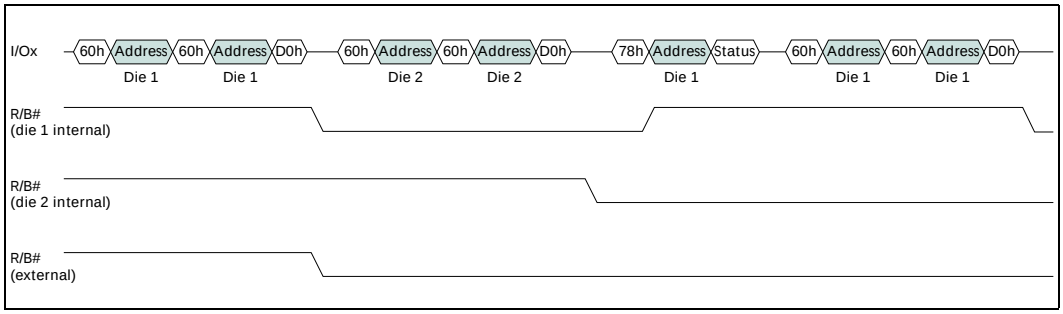
The interleaved TWO-PLANE BLOCK ERASE operation must meet two-plane addressing requirements. See Table 7.7.1, “TWO-PLANE Addressing” on page 38 for details.

Figure 47. Interleaved TWO-PLANE BLOCK ERASE with R/B# Monitoring



Note: Two-plane addressing requirements apply.

Figure 48. Interleaved TWO-PLANE BLOCK ERASE with Status Register Monitoring



Note: Two-plane addressing requirements apply.

7.9 RESET Operation

7.9.1 RESET FFh

The RESET command is used to put the memory device into a known condition and to abort a command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes LOW for ^{t}RST after the RESET command is written to the command register (see Figure 49 and Table 19).

The RESET command must be issued to all CE#s after power-on. The device will be busy for a maximum of 1ms. Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited during and following the initial RESET command and OTP operations.

Figure 49.RESET Operation

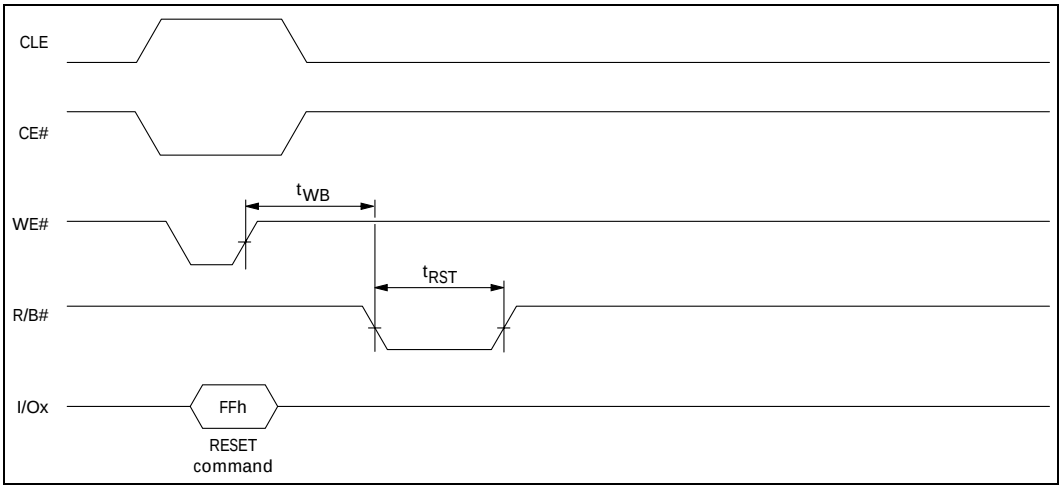


Table 19. Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

7.10 WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using the WP# pin. Figure 50 on page 55 through Figure 53 on page 56 illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, the WP# pin must not be toggled until the command is complete and the device is ready (status register bit 5 is “1”).

Figure 50. ERASE Enable

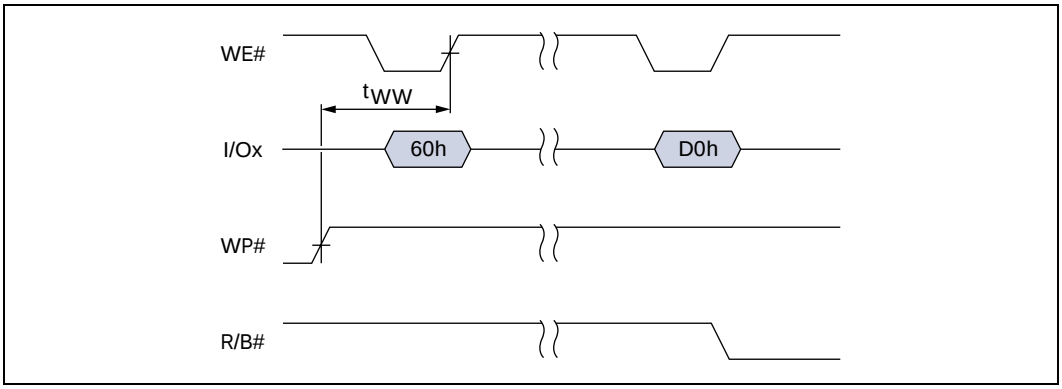


Figure 51. ERASE Disable

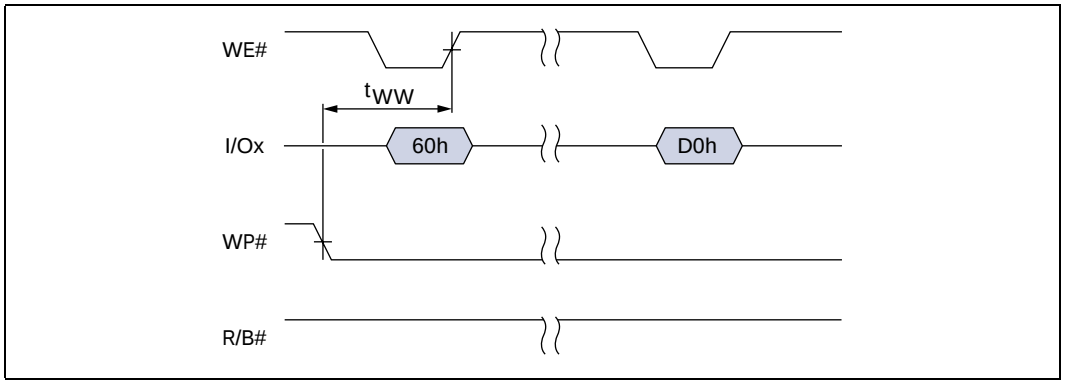


Figure 52. PROGRAM Enable

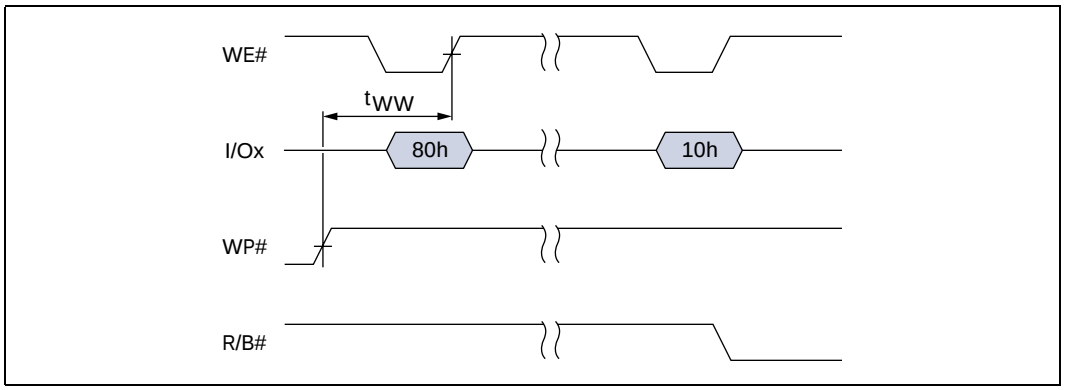
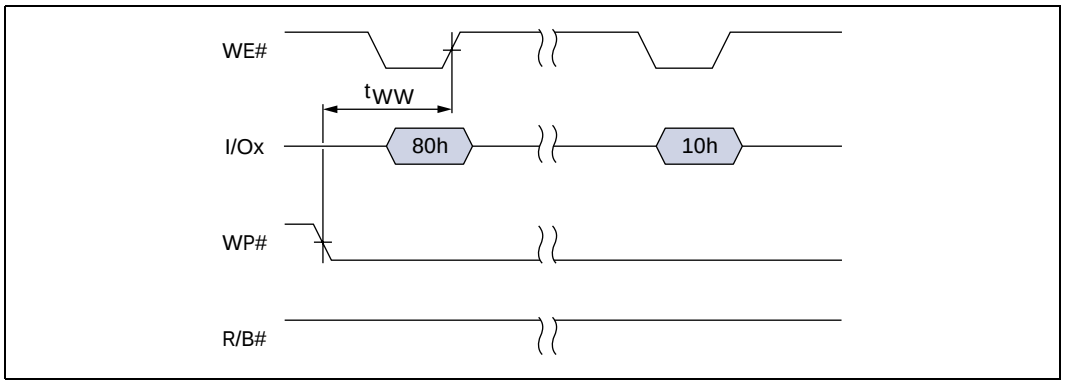


Figure 53. PROGRAM Disable



§ §

8.0 Error Management

Intel® SD74 NAND Flash Memory devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains one or more bad bits. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC (up to 1,000 PROGRAM/ERASE cycles) when shipped from the factory. This provides a reliable location for storing boot code and critical boot information.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming data other than FFh into the first spare location (column address 2,048) of the first or second page of each bad block.

System software should check the first spare address on the first and second page of each block prior to performing any program or erase operations on the NAND Flash device. A bad block table can then be created, allowing system software to map around these areas. Factory testing is performed under worst-case conditions. Because blocks marked “bad” may be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Check status after a PROGRAM, ERASE, or INTERNAL DATA MOVE operation.
- Under typical-use conditions, a minimum of 1-bit ECC per 528 bytes of data is required.
- Use bad block management and a wear-leveling algorithm.

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9.0 Timing Diagrams

Figure 54. COMMAND LATCH Cycle

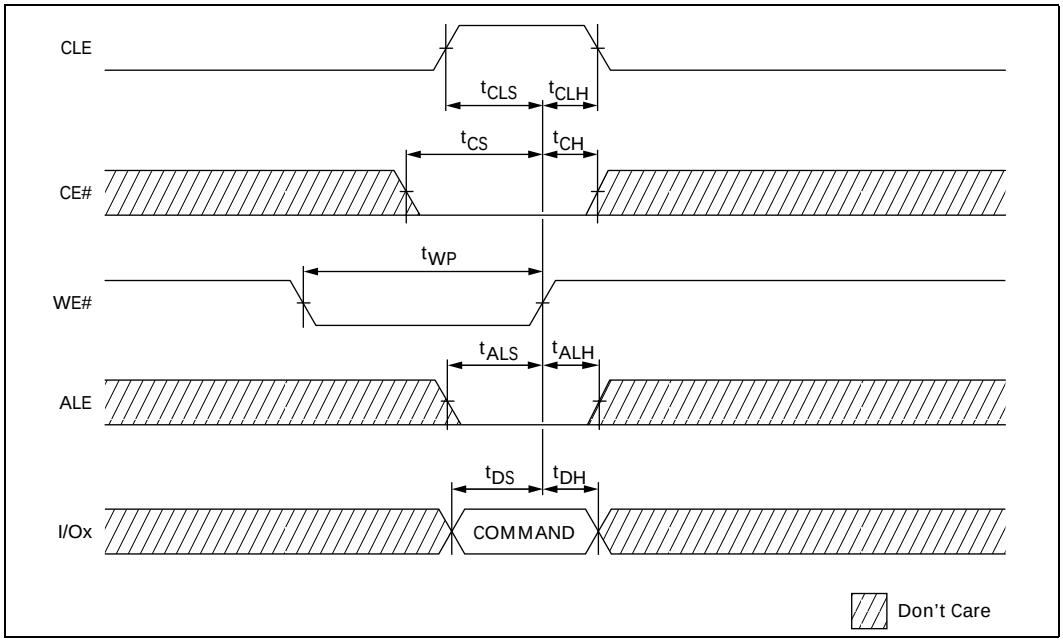


Figure 55. ADDRESS LATCH Cycle

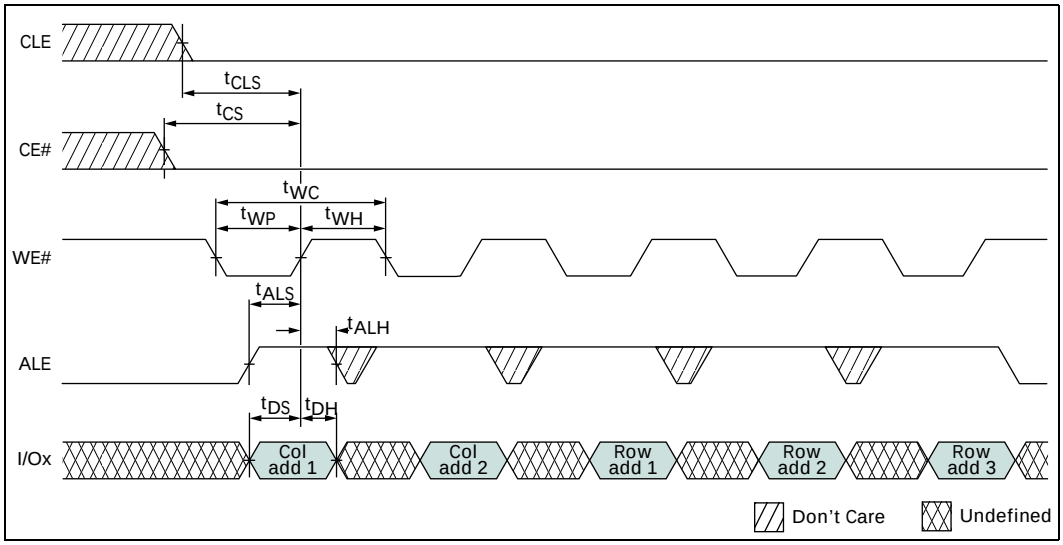
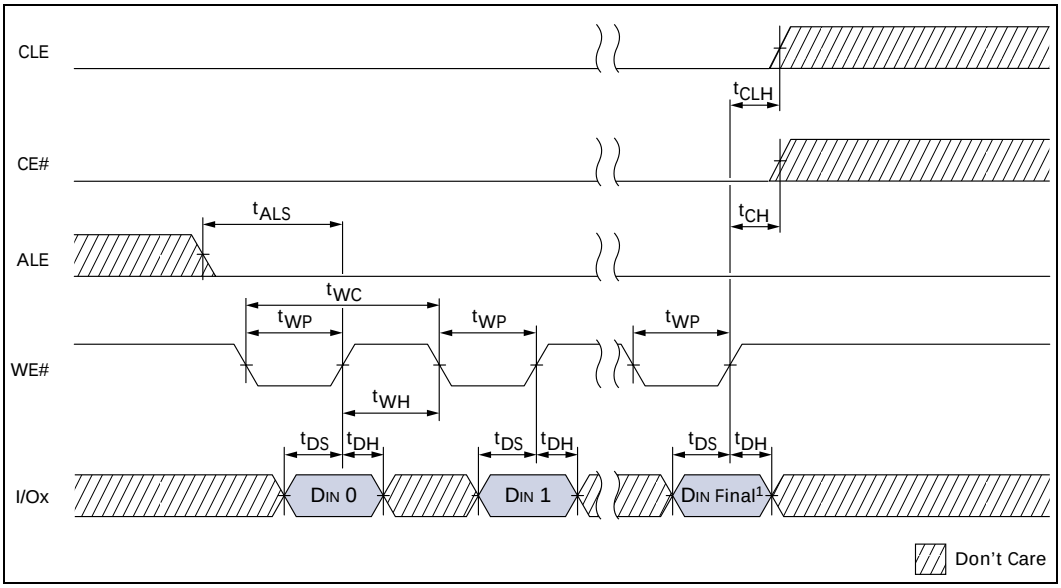
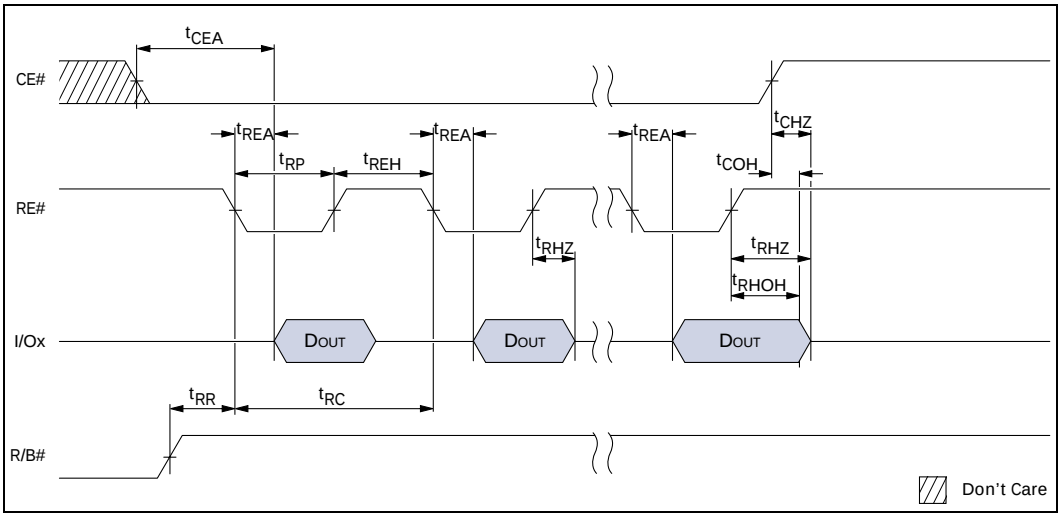


Figure 56. INPUT DATA LATCH Cycle



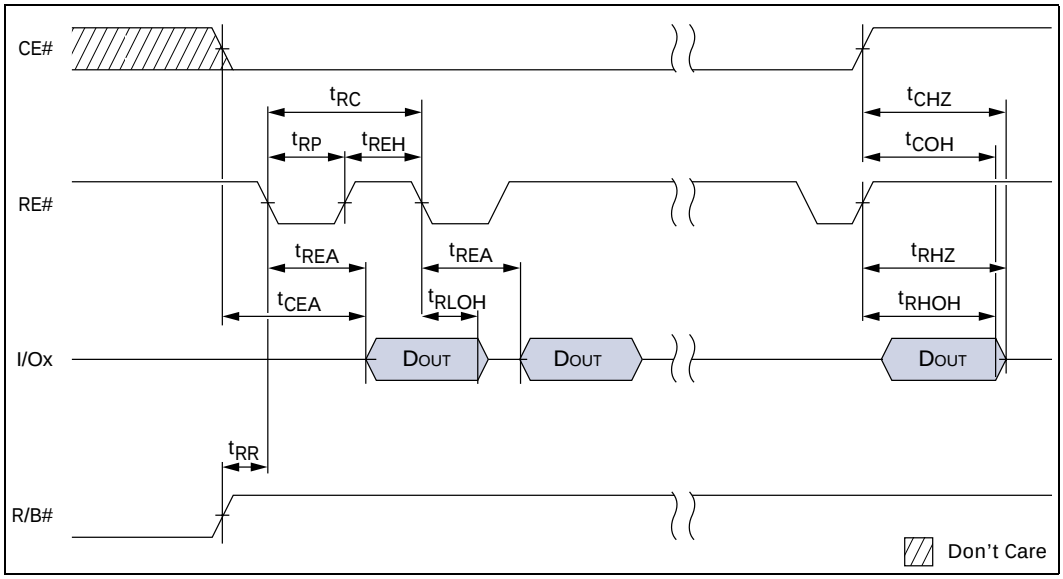
1. DIN Final = 2,111 (x8).

Figure 57. SERIAL ACCESS Cycle After READ



Note: Use this timing diagram for $^{t}RC \geq 30ns$.

Figure 58. SERIAL ACCESS Cycle After READ (EDO Mode)



Note: Use this timing diagram for $^{t}RC < 30ns$.

Figure 59. READ STATUS Operation

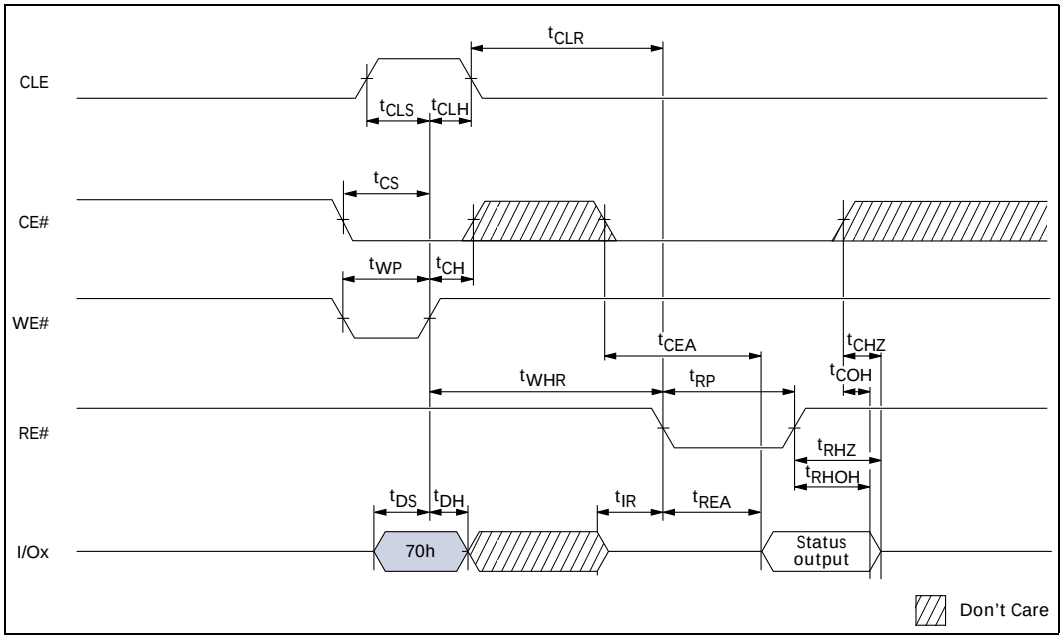


Figure 60. TWO-PLANE/MULTIPLE-DIE READ STATUS Operation

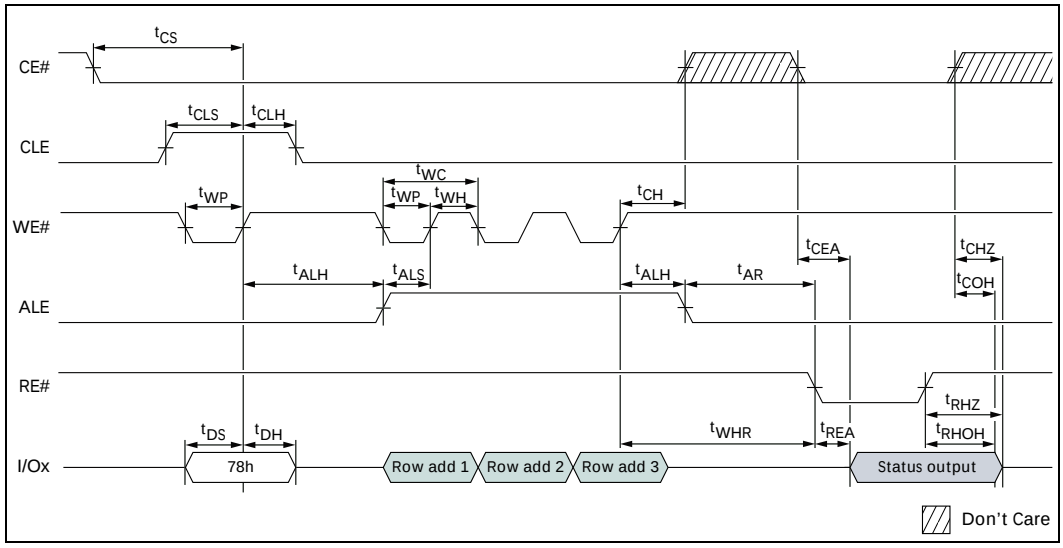


Figure 61. PAGE READ Operation

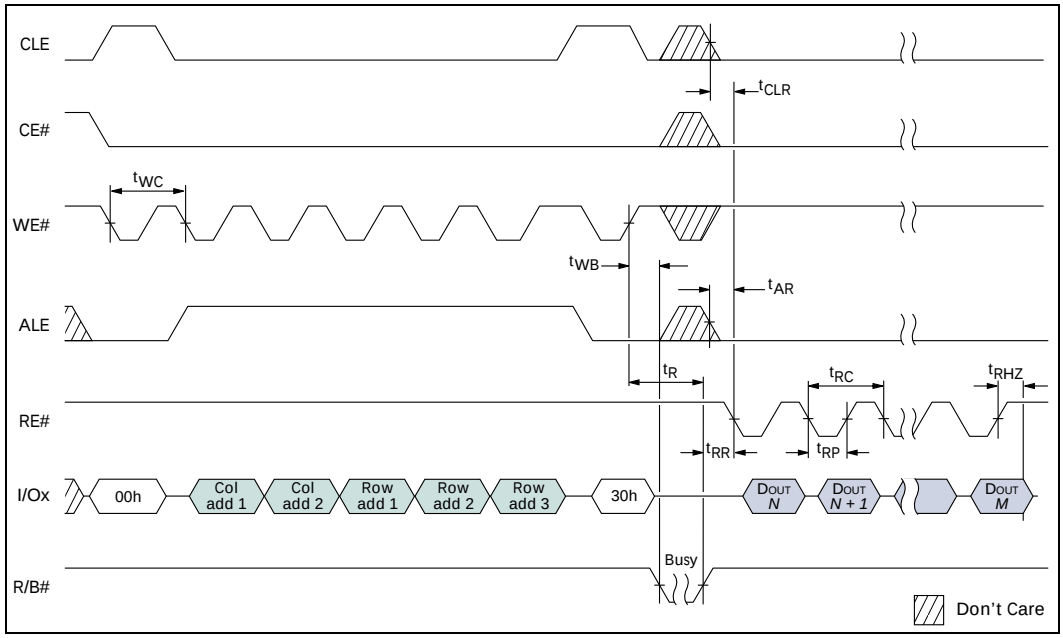


Figure 62. READ Operation with CE# "Don't Care"

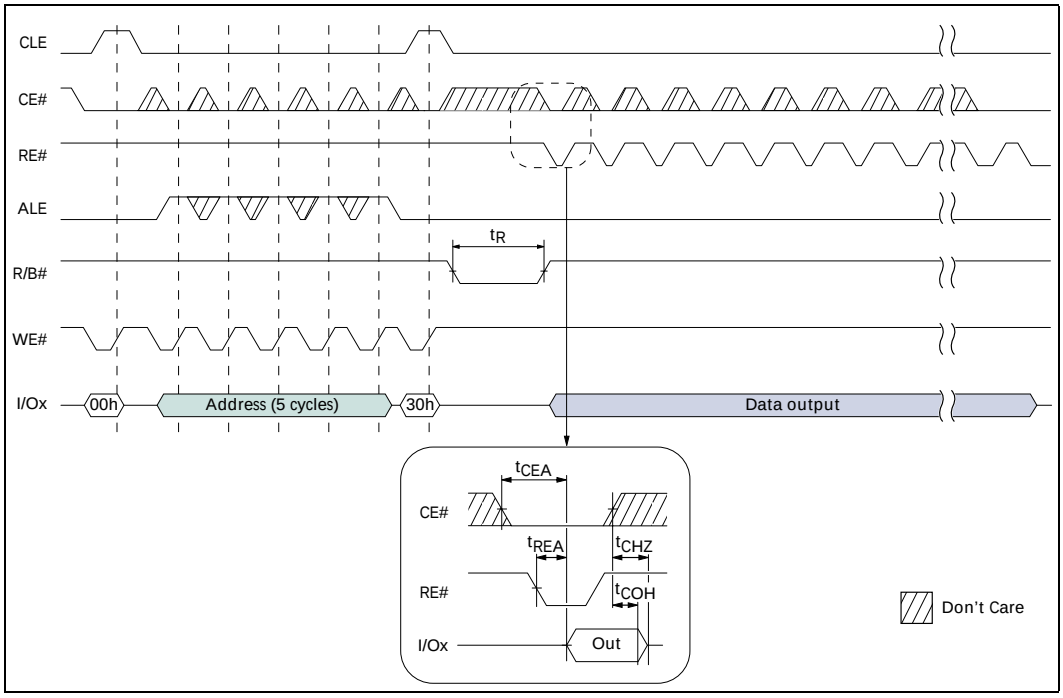


Figure 63. RANDOM DATA READ Operation

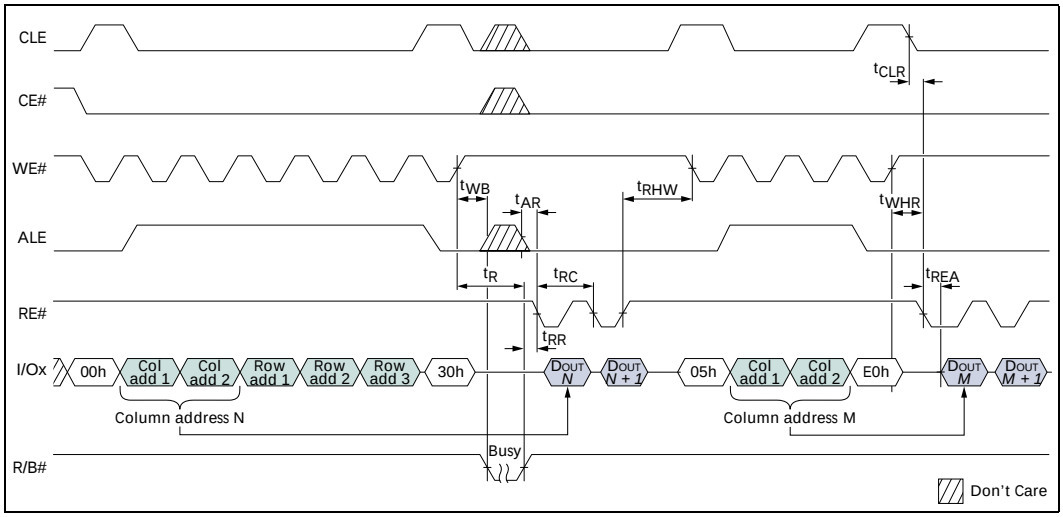


Figure 64. PAGE READ CACHE MODE Operation, Part 1 of 2

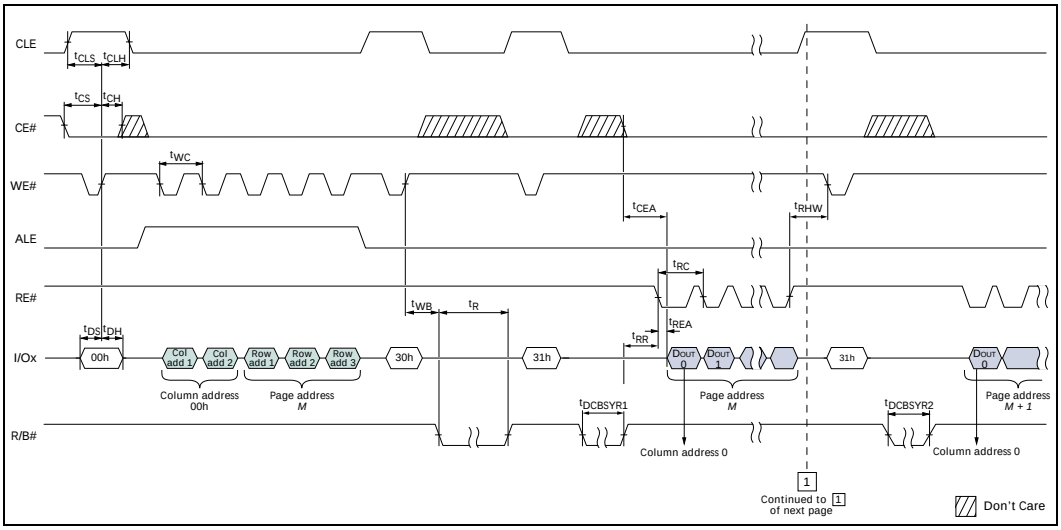


Figure 65. PAGE READ CACHE MODE Operation, Part 2 of 2

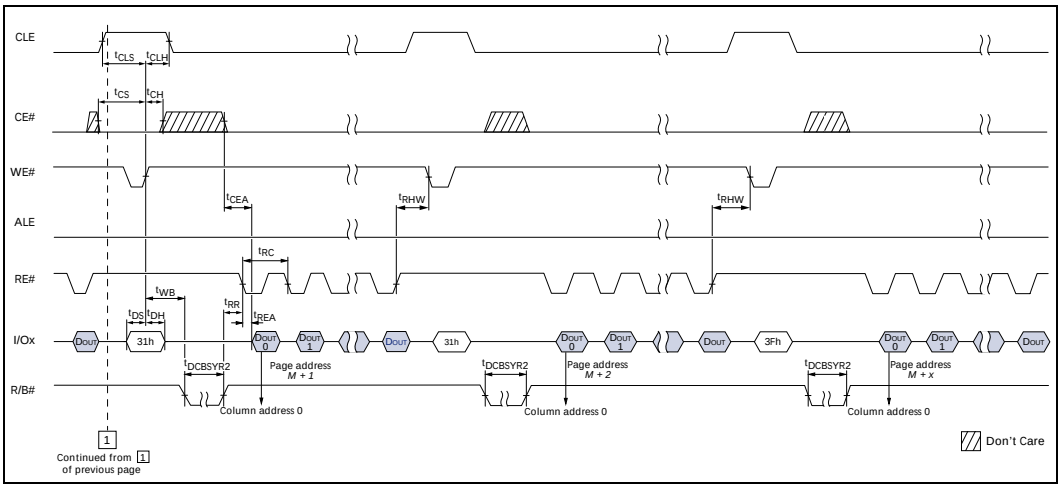


Figure 66. PAGE READ CACHE MODE Operation without R/B#, Part 1 of 2

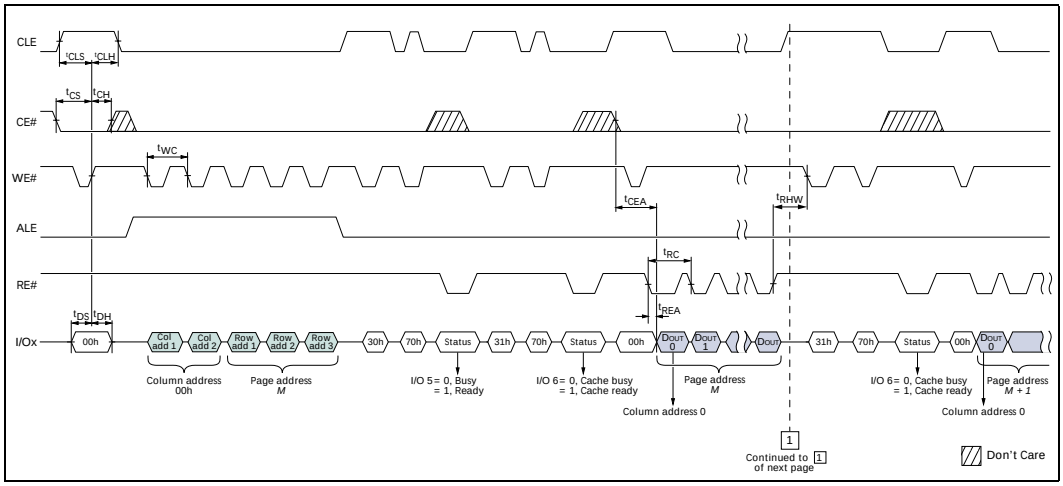


Figure 67. PAGE READ CACHE MODE Operation without R/B#, Part 2 of 2

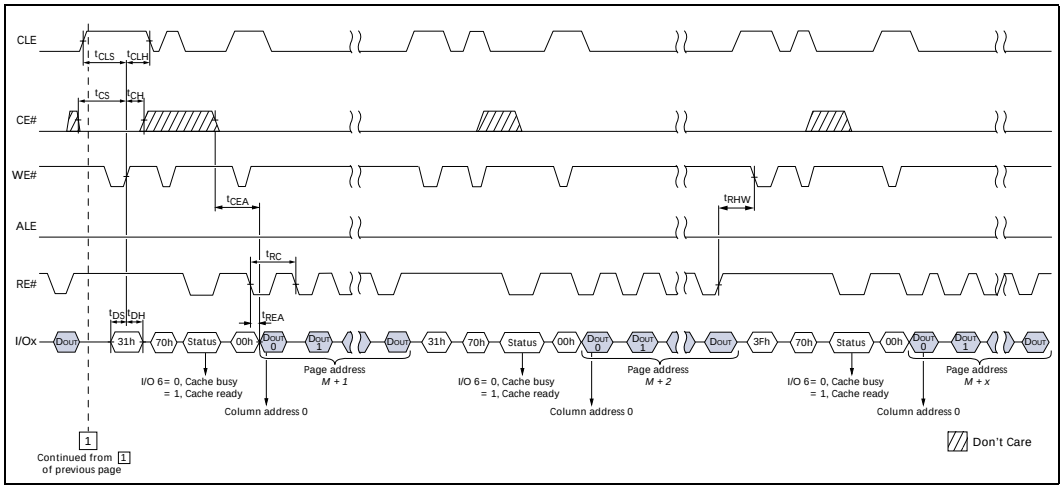
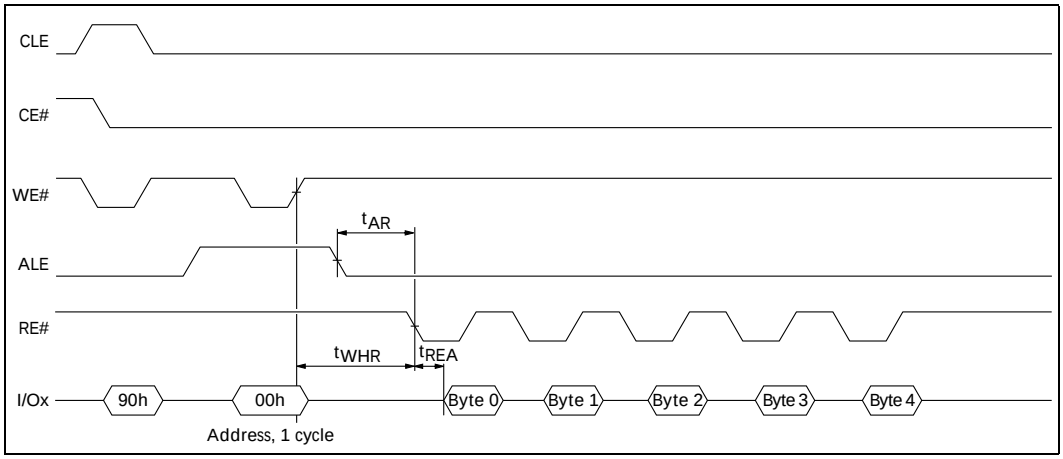


Figure 68. READ ID Operation



Note: See Table 17, "Device ID and Configuration Codes" on page 29 for actual values.

Figure 69. PROGRAM PAGE Operation

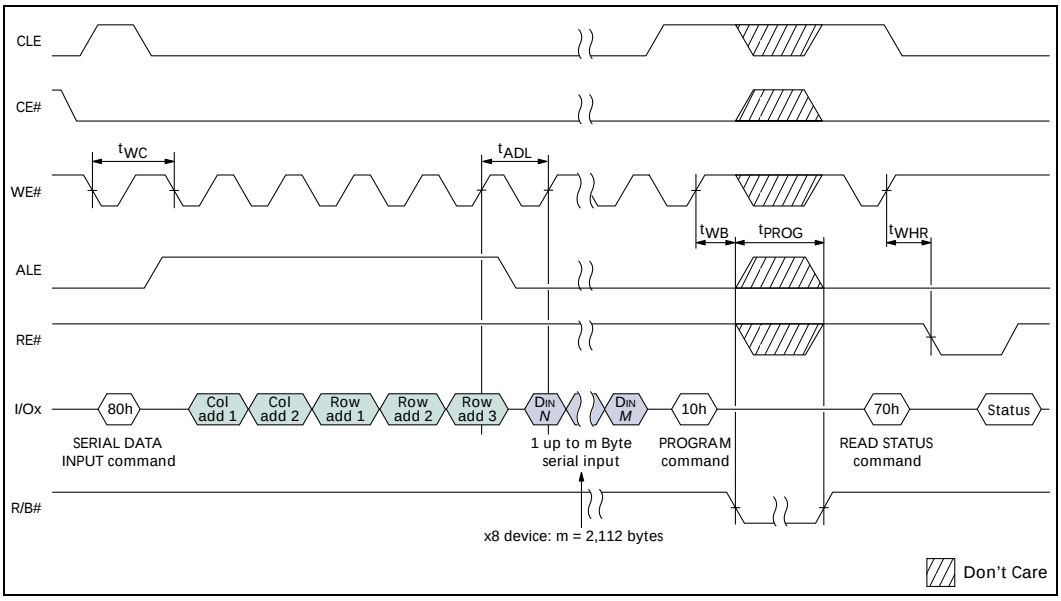


Figure 70. Program Operation with CE# "Don't Care"

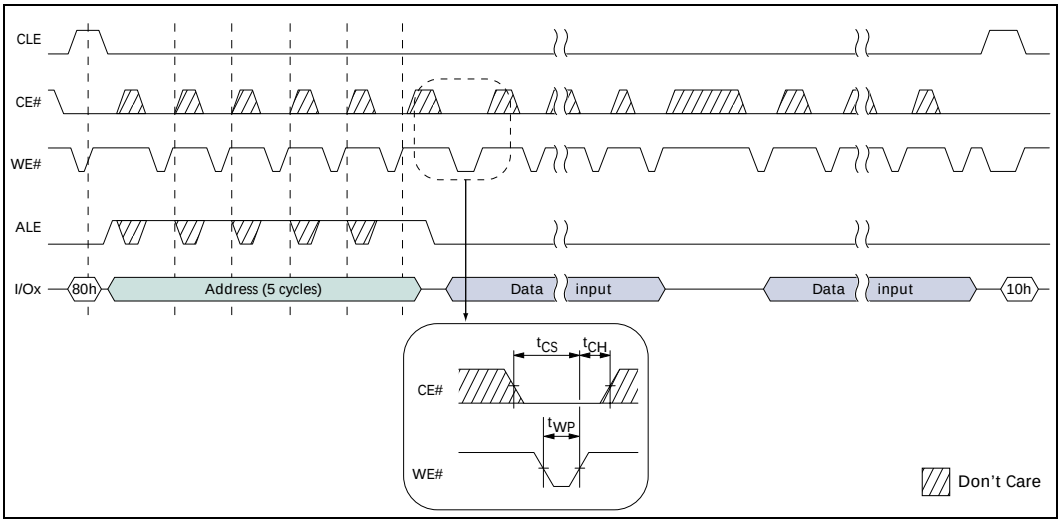


Figure 71. PROGRAM PAGE Operation with RANDOM DATA INPUT

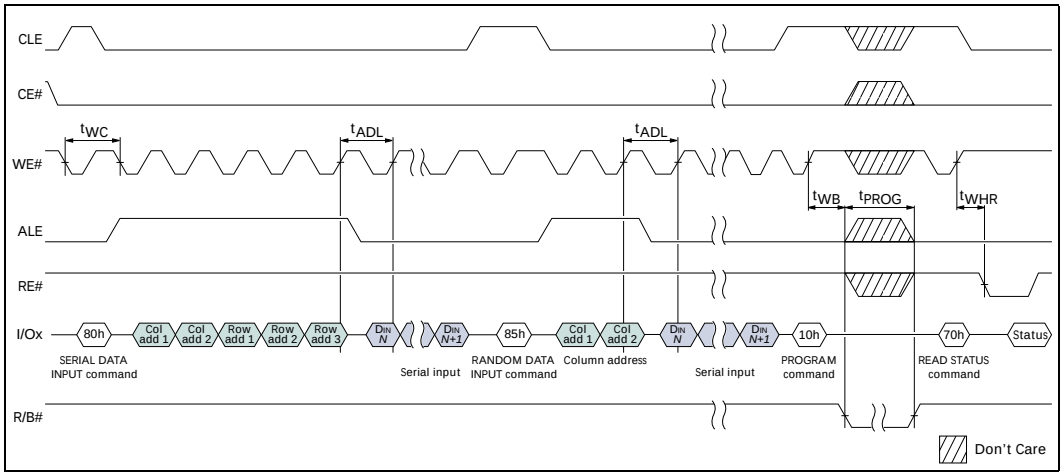
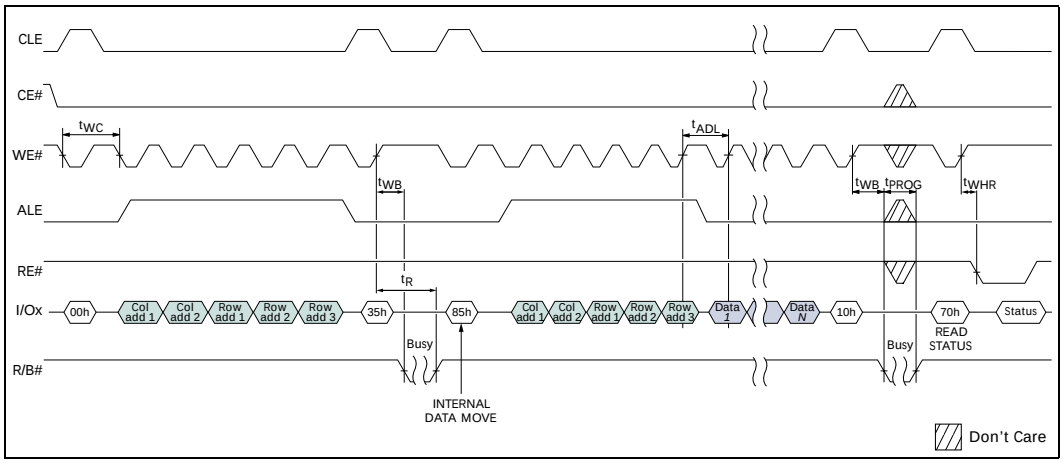


Figure 72. INTERNAL DATA MOVE Operation



Note: INTERNAL DATA MOVE operations are only supported within the plane from which data is read.

Figure 73. PROGRAM PAGE CACHE MODE Operation

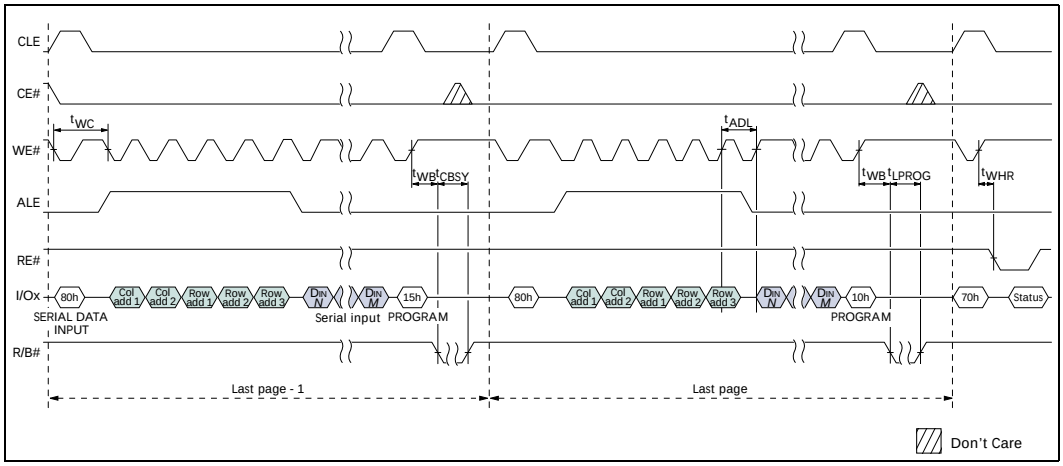


Figure 74. PROGRAM PAGE CACHE MODE Operation Ending on 15h

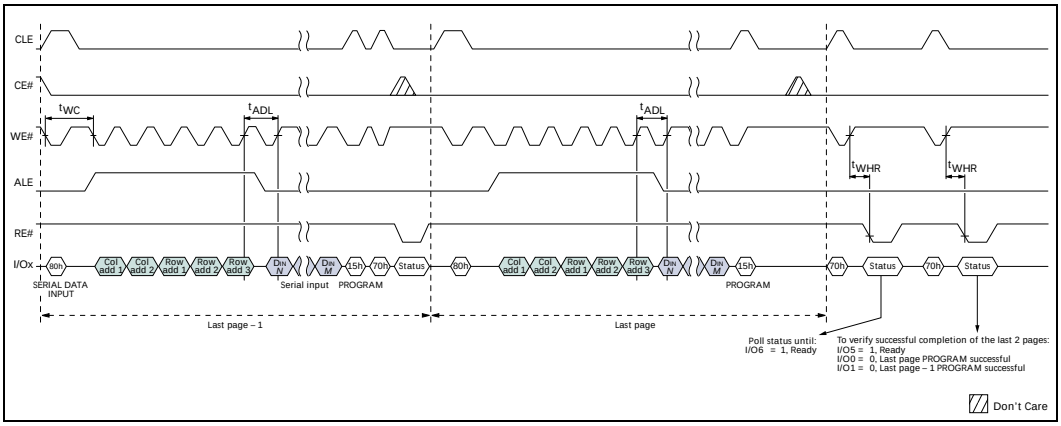


Figure 75. BLOCK ERASE Operation

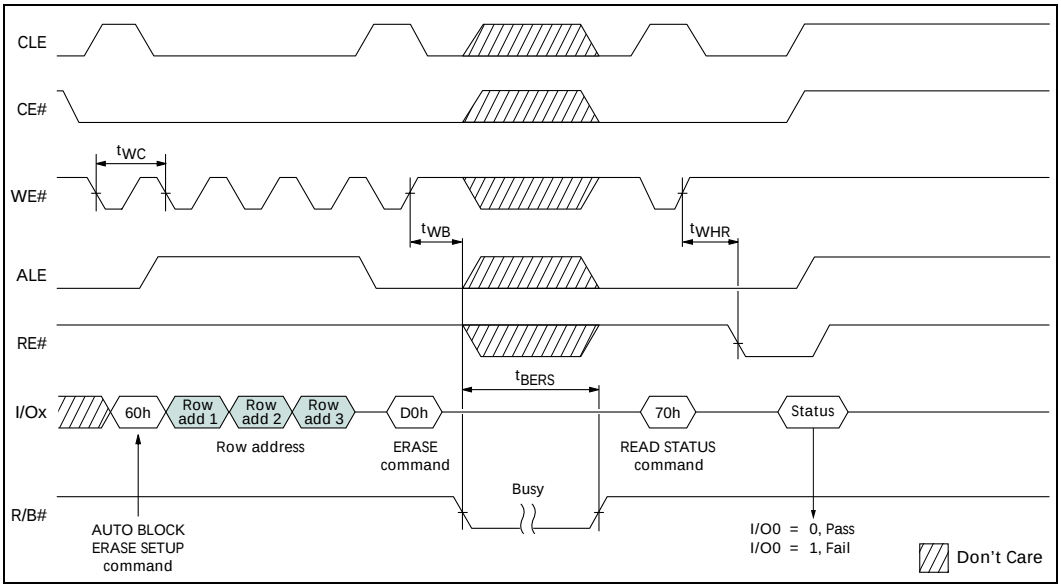
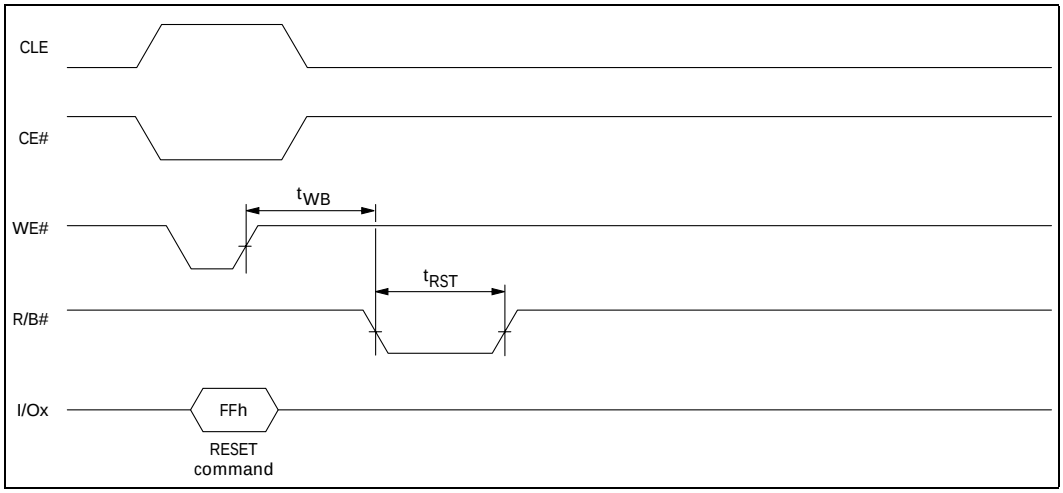


Figure 76. RESET Operation



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10.0 Ordering Information

Figure 77, “Decoder” on page 69 provides the device part number decoder and Table 20, “Intel® NAND Flash Memory Ordering Information” on page 69 provides the available combinations. For combinations not listed, please contact your local Intel sales office.

Figure 77. Decoder

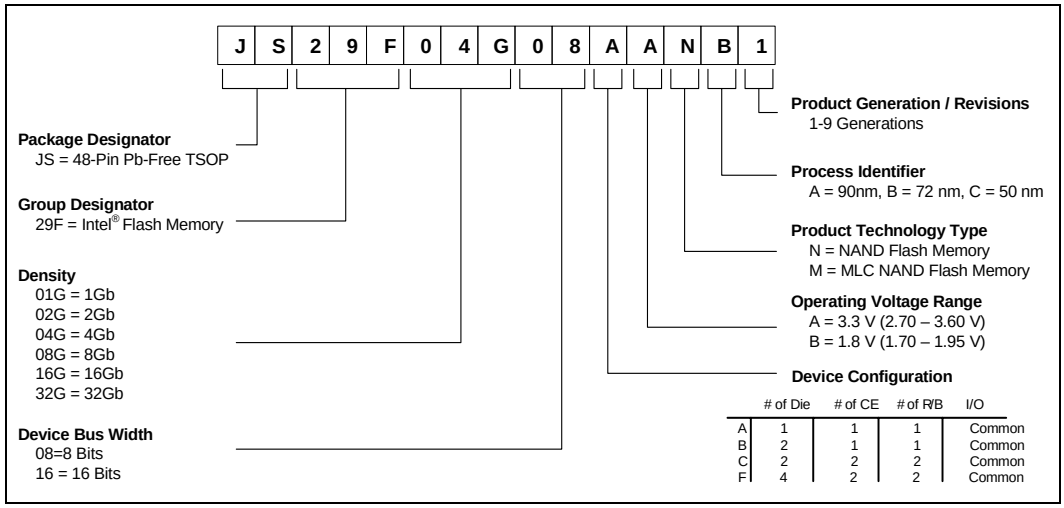

Table 20. Intel® NAND Flash Memory Ordering Information

IM L1 Part Number	Marking Device # (1st Mark Line)	MM # (2nd Mark Line)	Device Nomenclature
JS29F04G08AANB1	29F04G08AANB1	880199	4Gb, x8, 1 die, 3 V, NAND, 72 nm, 1st Gen Intel Si (1000pc T&R), Pb-Free
		880200	4Gb, x8, 1 die, 3 V, NAND, 72 nm, 1st Gen Intel Si (1000pc Tray Pack), Pb-Free
JS29F08G08CANB2	29F08G08CANB2	887759	8Gb, x8, 2 die, 3 V, 2 CE, NAND, 72 nm, 1st Gen Intel Si (1000pc T&R), Pb-Free
		887753	8Gb, x8, 2 die, 3 V, 2 CE, NAND, 72 nm, 1st Gen Intel Si (1000pc Tray Pack), Pb-Free
JS29F16G08FANB1	29F16G08FANB1	881167	16Gb, x8, 4 die, 3 V, 2 CE, NAND, 72 nm, 1st Gen Intel Si (1000pc Tray Pack), Pb-Free
		881166	16Gb, x8, 4 die, 3 V, 2 CE, NAND, 72 nm, 1st Gen Intel Si (1000pc T&R), Pb-Free

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