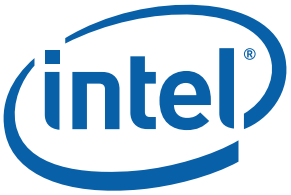


Intel® MD516 NAND Flash Memory

JS29F16G08AAMC1, JS29F32G08CAMC1, JS29F64G08FAMC1

Advance Datasheet

Product Features

- Open NAND Flash Interface (ONFI) 1.0 Compliant
- Multilevel cell (MLC) technology
- Organization:
  - — Page size: 4,314 bytes (4,096 + 218 bytes)
  - — Block size: 128 pages (512K + 27K bytes)
  - — Plane size: 2,048 blocks
  - — Device size: 16Gb: 4,096 blocks; 32Gb: 8,192 blocks; 64Gb: 16,384 blocks
- Read performance
  - — Random read: 50µs
  - — Sequential read: 20ns
- Write performance
  - — Page program: 900µs (TYP)
  - — Block erase: 2ms (TYP)
- Endurance:
  - — 5,000 PROGRAM/ERASE cycles
  - — Data Retention: JEDEC compliant
- Operating Temperature
  - — Commercial: 0 to +70 °C
  - — Extended: -40 to +85 °C
- Core Voltage (VCC): 2.7V - 3.6V
- First block (block address 00h) guaranteed to be valid when shipped from factory
- Industry-standard basic NAND Flash command set
- Advanced command set:
  - — PROGRAM PAGE CACHE MODE
  - — PAGE READ CACHE MODE
  - — One-time programmable (OTP) commands
  - — Two-plane commands
  - — Interleaved die operations
  - — READ UNIQUE ID (contact factory)
  - — READ ID2 (contact factory)
- Operation status byte provides a software method of detecting:
  - — Operation completion
  - — Pass/fail condition
  - — Write-protect status
- Ready/busy# (R/B#) signal provides a hardware method of detecting PROGRAM or ERASE cycle completion
- WP# signal: Entire device hardware write protect
- Staggered Power-up Sequence: Issue RESET command (FFH)
- INTERNAL DATA MOVE operations supported within the plane from which data is read
- Package: 48 TSOP, Type I (Lead-Free Plating)

Contents

Revision History

Date	Revision	Description
March 2007	001	Initial release Changed Endurance to 5K cycles and Retention to JEDEC Compliant

1.0 Introduction

NAND Flash technology provides a cost-effective solution for applications requiring high-density solid-state storage for:

- 16Gb NAND Flash memory device.
- 16Gb two-die stack that operate as a single 32Gb device.
- 16Gb four-die stack that operates as a single 64Gb device.

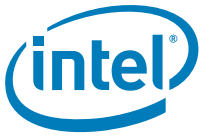
Intel® NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

Intel® NAND Flash devices use a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Two additional pins control hardware write protection (WP#) and monitor device status (R/B#).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

The 16-Mibt and 32-Mbit devices contain two planes per die, for a total of two or four planes respectively. Each plane consists of 2,048 blocks. Each block is subdivided into 128 programmable pages. Each page consists of 4,314 bytes. The pages are further divided into a 4,096-byte data storage region with a separate 218-byte area. The 218-byte area is typically used for error management functions.

The contents of each 4,314-byte page can be programmed in 900µs, and an entire block can be erased in 2ms. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/PROGRAM endurance is specified at 5,000 cycles when using appropriate error correcting code (ECC) and error management.



2.0 Functional Overview

This section provides an overview of the device in the following sections:

- Section 2.1, “Architecture”
- Section 2.2, “Memory Map and Addressing”

2.1 Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

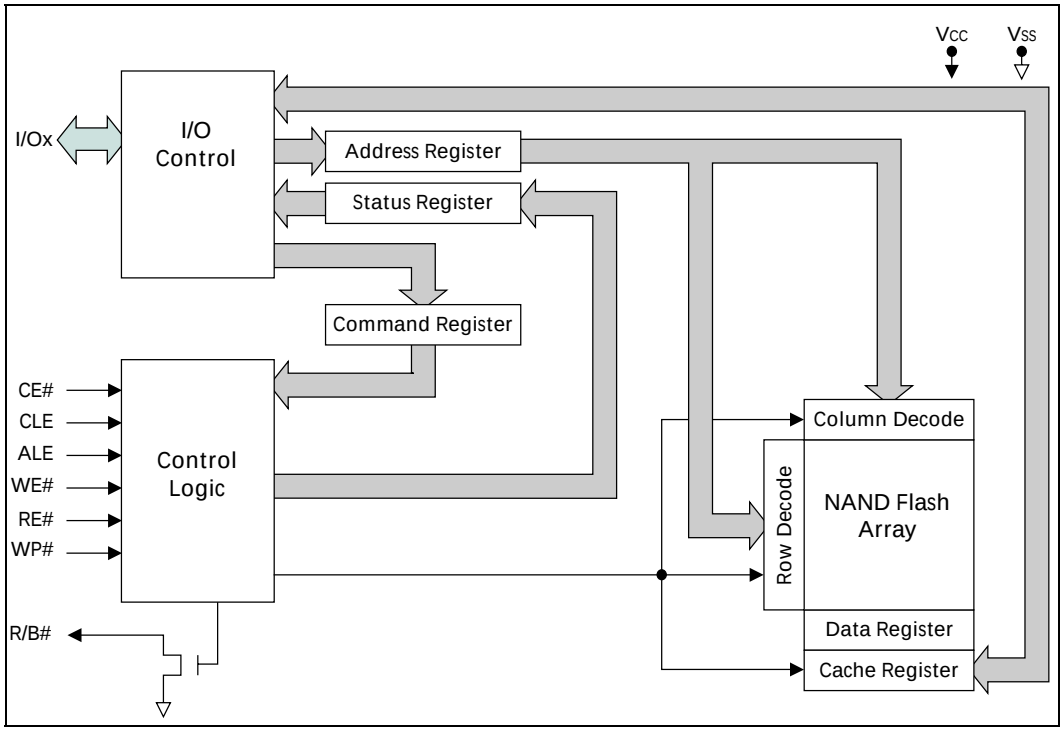
The data are transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data, whereas the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations and is erased in block-based operations. During normal page operations, the data and cache registers are tied together and act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

These devices also have a status register that reports the status of device operation.

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a five-cycle sequence as shown in Section 2.2, “Memory Map and Addressing” on page 8.

Figure 1. NAND Flash Functional Block Diagram



2.2 Memory Map and Addressing

2.2.1 Memory Map

Figure 2. Memory Map

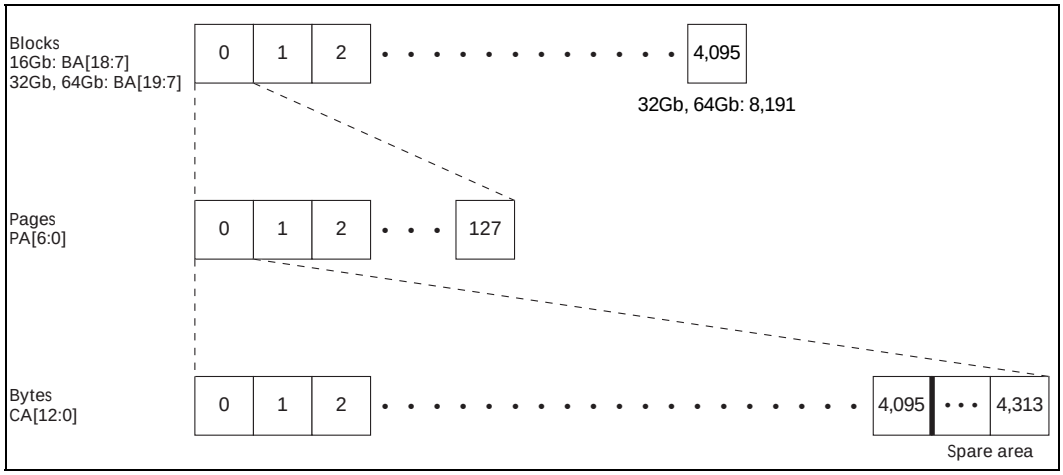


Table 1. Operational Example

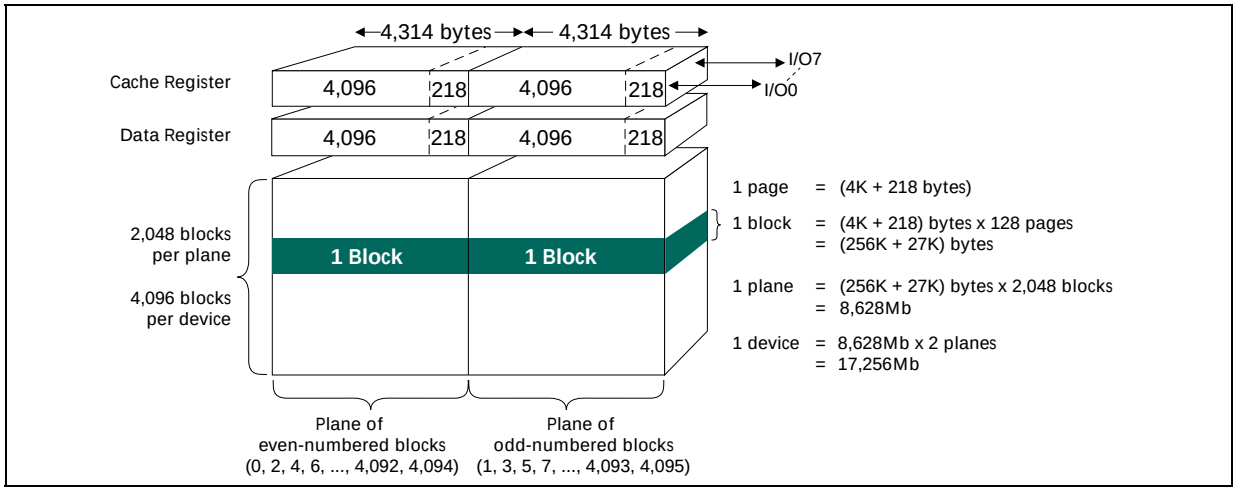
Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x00000010D9	0x00000010DA–0x0000001FFF
0	1	0x0000010000	0x00000110D9	0x00000110DA–0x0000011FFF
0	2	0x0000020000	0x00000210D9	0x00000210DA–0x0000021FFF
...	...	...	...	
4,095	126	0x07FFFE0000	0x07FFFE10D9	0x07FFFE10DA–0x03FFFE1FFF
4,095	127	0x07FFFF0000	0x07FFFF10D9	0x07FFFF10DA–0x03FFFF1FFF

Note: The three most significant bits in the high nibble of ADDRESS cycle 2 are not assigned; however, these 3 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.

The 13-bit column address is capable of addressing from 0 to 8,191 bytes on a x8 device; however, only bytes 0 through 4,313 are valid. Bytes 4,314 through 8,191 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

2.2.2 Array Organization

Figure 3. Array Organization, 16Gb or 32Gb



1. For the 32Gb device, the 16Gb array organization shown here applies to each chip enable (CE# and CE2#).

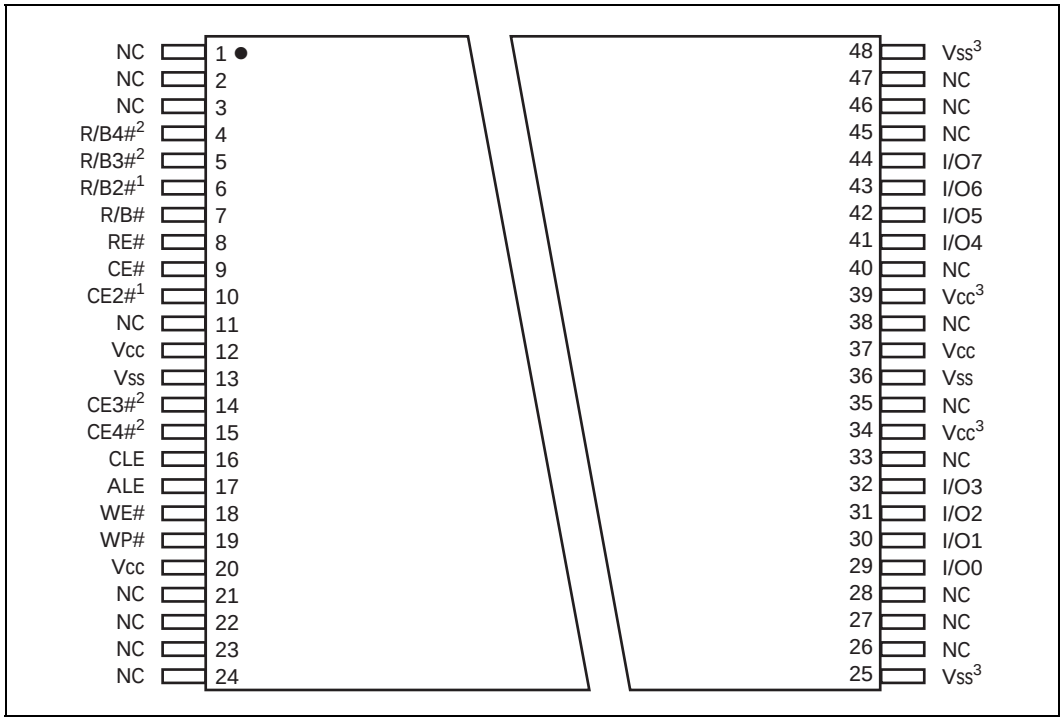
Table 2. Array Addressing, 16Gb or 32Gb

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7[3]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW		BA18	BA17	BA16

1. Block address concatenated with page address = actual page address. CAx, PAx, and BAx = column, page and block address, respectively.
2. Column adress 4,313 (10D9h) is the maximum valid column address.
3. Plane select bit: 0 = plane of even-numbered blocks 1 = plane of odd-numbered blocks.

3.0 Signal Assignments and Descriptions

Figure 4. Pin Assignment (Top View) 48-Pin TSOP Type 1



1. CE2# and R/B2# on 64Gb device only. These pins are NC for other configurations.
2. CE3#, CE4#, R/B3#, and R/B4# are for reference. Bond pads must be added for these pins to be used.
3. These Vcc and Vss pins are for compatibility with the ONFI TSOP x16 pinout, but are not internally connected.

Table 3. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Pin Function
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#, CE2#	Input	Chip enable: Gates transfers between the host system and the NAND Flash device. Once the device starts a PROGRAM or ERASE operation, CE# can be deasserted.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#	Input	Read enable: Gates transfers from the NAND Flash device to the host system.
WE#	Input	Write enable: Gates transfers from the host system to the NAND Flash device.
WP#	Input	Write protect: Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
I/O[7:0] (x8)	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#, R/B2#	Output	Ready/Busy: An open-drain, active-LOW output, that uses an external pull-up resistor. The pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during a READ operation to indicate when data is being transferred from the array into the serial data register. Once these operations have completed, R/B# returns to the high-impedance state.

Table 3. Signal Descriptions (Sheet 2 of 2)

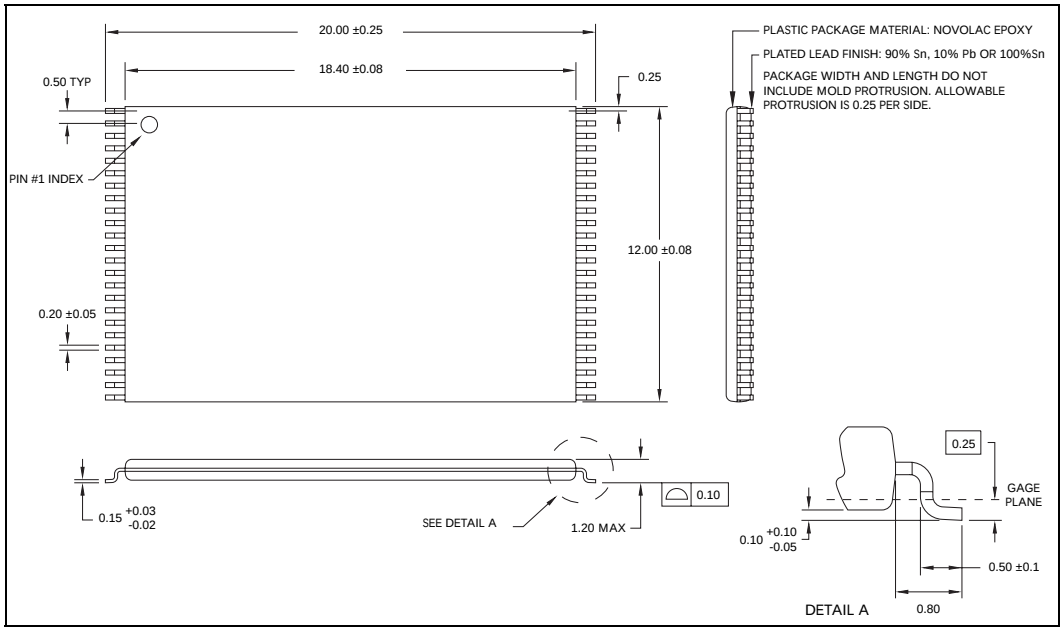
Symbol	Type	Pin Function
VCC	Supply	VCC: Power supply pin.
VSS	Supply	VSS: Ground connection.
NC	–	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	–	Do not use: DNUs must be left disconnected.

Note: The 32Gb device and 64Gb device packages incorporate two and four separate 16Gb devices, respectively. For the 32Gb device, all pins for the first and second devices are denoted "–1" and "–2," respectively. For the 64Gb device, all pins for the first 32Gb devices and second 32Gb devices are denoted "-1" and "-2" respectively.

4.0 Package Information

4.1 TSOP Package Information

Figure 5. TSOP Type 1 Package Dimensions



Note: All dimensions in millimeters; MIN/MAX, or typical, as noted.

5.0 NAND Flash Bus Operations

The bus on the MD516 family of devices is multiplexed. Data I/O, addresses, and commands all share the same pins, I/O[7:0].

The command sequence normally consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and one or more DATA cycles—either READ or WRITE.

5.1 Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control Flash device READ and WRITE operations. On a 32Gb multi-level cell device, CE# and CE2# each control independent 16Gb arrays, and on a 64Gb multi-level cell device, CE# and CE2# each control independent 32Gb arrays. CE# and CE2# function the same, each controlling its own array; that is, all operations described for CE# also apply to CE2#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the Flash memory will accept command, address, and data information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption.

The CE# “Don’t Care” operation allows the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus. One device can be programmed while another is being read.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

5.2 Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- the device is not busy.

As exceptions, the device accepts the READ STATUS, TWO-PLANE/MULTIPLE-DIE READ STATUS, and RESET commands when busy. Commands are transferred to the command register on the rising edge of WE#. Commands are input on I/O[7:0] only.

5.3 Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are low, and
- ALE is high.

Addresses are input on I/O[7:0] only. Bits not part of the address space must be LOW.

The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

5.4 Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy.

Data is input on I/O[7:0]. See Figure 70 on page 73 for additional data input details.

5.5 READs

After a READ command is issued, data is transferred from the memory array to the data register from the rising edge of WE#. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. R/B# returns to HIGH at this time. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 74 on page 75 for detailed timing information.

The READ STATUS (70h) command, TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command, or the R/B# signal can be used to determine when the device is ready.

If a controller is using a timing of 30ns or longer for ^{t}RC, use Figure 71 on page 73 for proper timing. If ^{t}RC is less than 30ns, use Figure 72 on page 74 for extended data output (EDO) timing.

5.6 Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically R/B# would be connected to an interrupt pin on the system controller (see Figure 8 on page 15).

On the 64Gb device, R/B# provides a status indication for the 32Gb section enabled by CE#, and R/B2# does the same for the 32Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 32Gb section. On the 32Gb and 64Gb devices, R/B#-1 and R/B#-2 can be tied together, or they can be used separately to provide independent indications for each 16Gb and 32Gb section, respectively.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC; see Figure 9, "^{t}Fall and ^{t}Rise" on page 15).

Figure 6. Time Constants

$$TC = R \times C$$

Where R = Rp and C = total capacitive load

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figure 9 on page 15, and Figure 10 on page 16, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and Vcc.

Figure 7. Minimum Rp

$$Rp\ (MIN, 3.3V\ part) = \frac{V_{CC}\ (MAX) - V_{OL}\ (MAX)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where ΣI_L is the sum of the input currents of all devices tied to the R/B# pin.

Figure 8. READY/BUSY# Open Drain

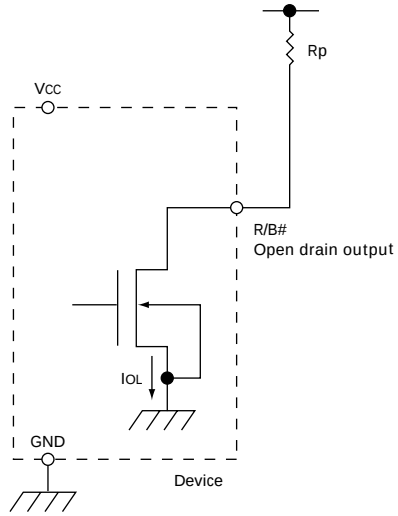
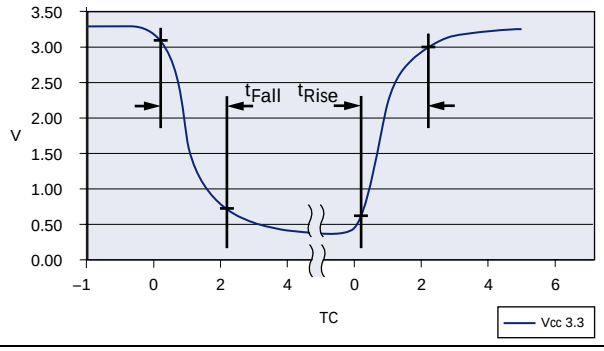


Figure 9. ^{t}Fall and ^{t}Rise



1. tFall and tRise calculated at 10 percent–90 percent points.
2. tRise dependent on external capacitance and resistive loading and output transistor impedance.
3. tRise primarily dependent on external pull-up resistor and external capacitive loading.
4. tFall ª 10ns at 3.3V; tFall ª 7ns at 1.8V.
5. See TC values in Figure 11 on page 16 for approximate Rp value and TC.

Figure 10. IOL vs. Rp

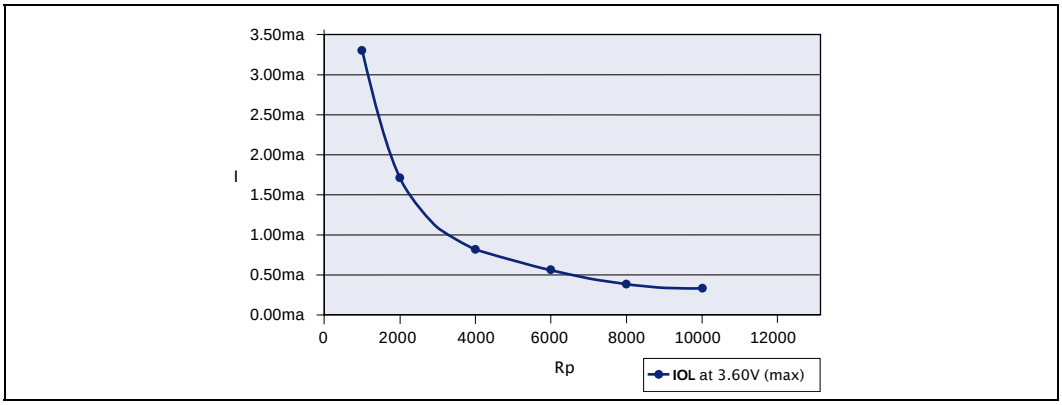


Figure 11. TC vs. Rp

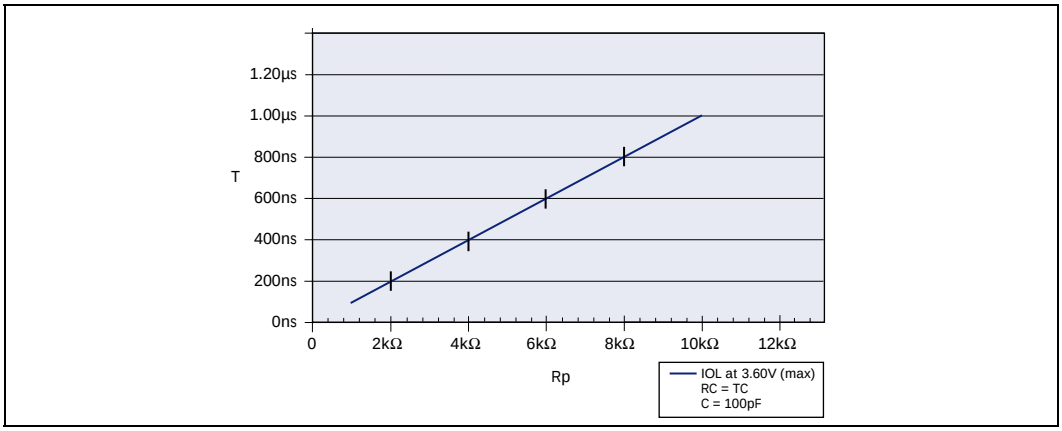


Table 4. Mode Selection (Sheet 1 of 2)

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L		H	X	Read mode	Command input
L	H	L		H	X		Address input
H	L	L		H	H	Write mode	Command input
L	H	L		H	H		Address input
L	L	L		H	H	Data input	
L	L	L	H		X	Sequential read and data output	
X	X	X	H	H	X	During read (busy)	
X	X	X	X	X	H	During program (busy)	

Table 4. Mode Selection (Sheet 2 of 2)

CLE	ALE	CE#	WE#	RE#	WP#	Mode
X	X	X	X	X	H	During erase (busy)
X	X	X	X	X	L	Write protect
X	X	H	X	X	0V/Vcc[1]	Standby

1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = Vih or Vil.

6.0 Electrical Characteristics

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation of the device at or above those indicated in the operational sections of this specification is not guaranteed.

Table 5. Absolute Maximum Ratings by Device

Parameter/Condition	Symbol	Min	Max	Unit
Voltage input	VIN	–0.6	+4.6	V
Vcc supply voltage	Vcc	–0.6	+4.6	V
Storage temperature	Tstg	–65	+150	°C
Short circuit output current, I/Os		–	5	mA

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 6. Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	Ta	0	–	+70	°C
	Extended		–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Ground supply voltage		Vss	0	0	0	V

6.1 Vcc Power Cycling

Intel® NAND Flash devices are designed to prevent data corruption during power transitions. Vcc is internally monitored. (The WP# signal permits additional hardware protection during power transitions.) When VCC reaches 2.5V for a 3V device, a minimum of 100µs should be allowed for the flash device to initialize before any commands are executed. (see Figure 12, “AC Waveforms During Power Transitions” on page 19).

The RESET command must be issued to all CE#s after the NAND flash device is powered on. Each CE# will be busy for a maximum of 1ms after a RESET command is issued.

Figure 12. AC Waveforms During Power Transitions

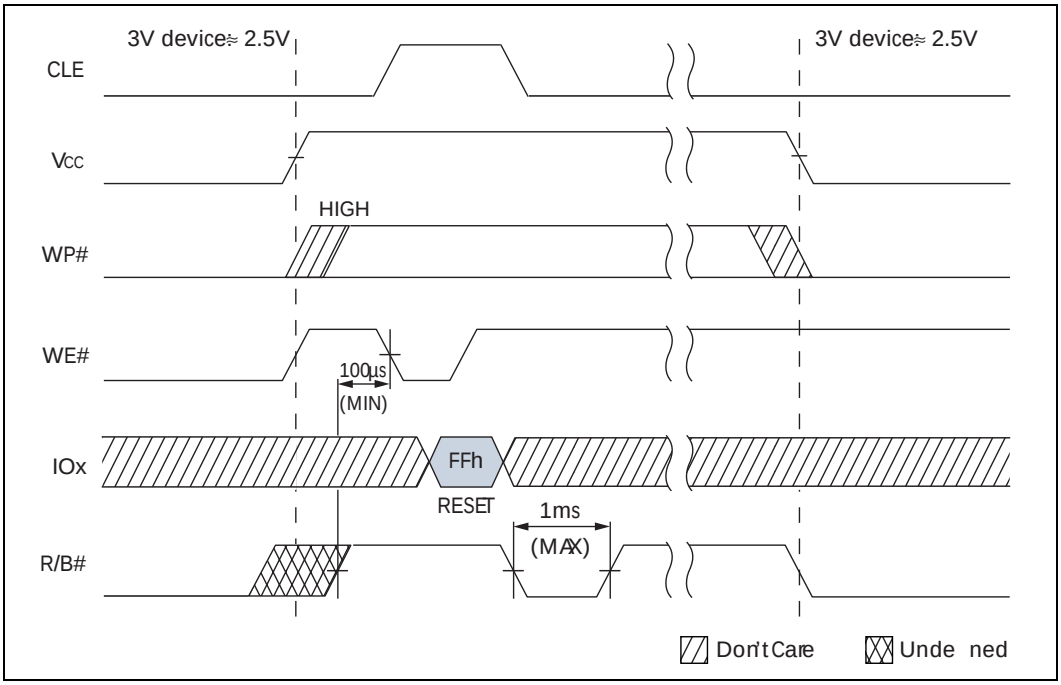


Table 7. Device DC and Operating Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Sequential read current	$^{t}RC = {}^{t}RC(MIN)$, CE# = V_{IL}, I_{OUT} = 0mA	I_{CC1}	–	20	40	mA
Program current	–	I_{CC2}	–	20	40	mA
Erase current	–	I_{CC3}	–	20	40	mA
Standby current (TTL)	CE# = V_{IH}, LOCKPRE = WP# = 0V/Vcc	I_{SB1}	–	–	1	mA
Standby current (CMOS)	CE# = Vcc – 0.2V, LOCKPRE = WP# = 0V/Vcc	I_{SB2}	–	10	50	µA
Input leakage current	V_{IN} = 0V to Vcc	I_{LI}	–	–	±10	µA
Output leakage current	V_{OUT} = 0V to Vcc	I_{LO}	–	–	±10	µA
Input high voltage	I/Ox, CE#, CLE, ALE, WE#, RE#, WP#, R/B#	V_{IH}	0.8 x Vcc	–	Vcc + 0.3	V
Input low voltage (all inputs)	–	V_{IL}	–0.3	–	0.2 x Vcc	V
Output high voltage	I_{OH} = –400µA	V_{OH}	0.67 x Vcc	–	–	V
Output low voltage	I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V
Output low current (R/B#)	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA

Table 8. Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	16 Gbit Device, single die	3,936	4,096	Blocks	1, 2
		32 Gbit Device, dual die	7,872	8,192		3
		64 Gbit Device, quad die	15,744	16,384		4

1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below Nvb during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid and does not require error correction up to 1K PROGRAM/ERASE cycles.
3. Each 16Gb section has a maximum of 160 invalid blocks.
4. Each 32Gb section has a maximum of 320 invalid blocks.

Table 9. Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input capacitance	Cin	SDP	10	pF	1, 2
		DDP	20		
		QDP	40		
Input/output capacitance (I/O)	Cout	SDP	10	pF	1, 2
		DDP	20		
		QDP	40		

1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_c = 25°C; f = 1 MHz; Vin = 0V.

Table 10. Test Conditions

Parameter		Value	Notes
Input pulse levels		0.0V to 3.3V	
Input rise and fall times		5ns	
Input and output timing levels		Vcc/2	
Output load	Vcc = 3.0V ± 10%	1 TTL GATE and CL = 50pF	1
	Vcc = 3.3V ± 10%	1 TTL GATE and CL = 100pF	1

1. Verified in device characterization; not 100 percent tested.

Table 11. AC Characteristics: Command, Data, and Address Input (Sheet 1 of 2)

Parameter	Symbol	PROGRAM PAGE CACHE MODE Operation		Standard Operating Modes		Unit	Notes
		Min	Max	Min	Max		
ALE to data start	tADL	100	–	70	–	ns	1
ALE hold time	tALH	10	–	5	–	ns	2
ALE setup time	tALS	15	–	10	–	ns	2
CE# hold time	tCH	10	–	5	–	ns	2
CLE hold time	tCLH	10	–	5	–	ns	2
CLE setup time	tCLS	15	–	10	–	ns	2

Table 11. AC Characteristics: Command, Data, and Address Input (Sheet 2 of 2)

Parameter	Symbol	PROGRAM PAGE CACHE MODE Operation		Standard Operating Modes		Unit	Notes
		Min	Max	Min	Max		
CE# setup time	^{t}CS	25	–	15	–	ns	2
Data hold time	^{t}DH	5	–	5	–	ns	2
Data setup time	^{t}DS	15	–	7	–	ns	2
WRITE cycle time	^{t}WC	35	–	20	–	ns	2
WE# pulse width HIGH	^{t}WH	15	–	7	–	ns	2
WE# pulse width	^{t}WP	17	–	10	–	ns	2
WP# setup time	^{t}WW	30	–	30	–	ns	

1. Timing for ^{t}ADL begins in the ADDRESS cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.
2. For PROGRAM PAGE CACHE MODE operations, the PROGRAM PAGE CACHE MODE operation AC characteristics apply.

Table 12. AC Characteristics: Normal Operation

Parameter	Symbol	PROGRAM PAGE CACHE MODE Operation		Standard Operating Modes		Unit	Notes
		Min	Max	Min	Max		
ALE to RE# delay	tAR	10	–	10	–	ns	
CE# access time	tCEA	–	30	–	25	ns	1
CE# HIGH to output High-Z	tCHZ	–	50	–	30	ns	2
CLE to RE# delay	tCLR	10	–	10	–	ns	
CE# HIGH to output hold	tCOH	15		15		ns	
Cache busy in page read cache mode (first 31h)	tDCBSYR1	–	10	–	10	µs	
Cache busy in page read cache mode (next 31h and 3Fh)	tDCBSYR2	tDCBSYR1	50	tDCBSYR1	50	µs	
Output High-Z to RE# LOW	tIR	0	–	0	–	ns	1
Data transfer from Flash array to data register	tR	–	50	–	50	µs	
READ cycle time	tRC	35	–	20	–	ns	1
RE# access time	tREA	–	25	–	16	ns	1, 3
RE# HIGH hold time	tREH	15	–	7	–	ns	1, 3
RE# HIGH to output hold	tRHOH	15	–	15	–	ns	3
RE# HIGH to WE# LOW	tRHW	100	–	100	–		
RE# HIGH to output High-Z	tRHZ	–	100	–	100	ns	2, 3
RE# LOW to output hold	tRLOH	0		5		ns	3
RE# pulse width	tRP	17	–	10	–	ns	1
Ready to RE# LOW	tRR	20	–	20	–	ns	
Reset time (READ/PROGRAM/ ERASE)	tRST	–	1	–	1	ms	4, 6
WE# HIGH to busy	tWB	–	100	–	100	ns	5
WE# HIGH to RE# LOW	tWHR	80	–	60	–	ns	

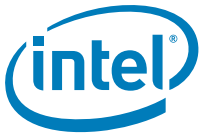
1. For PROGRAM PAGE CACHE MODE operations, the PROGRAM PAGE CACHE MODE operation AC characteristics apply.

2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if I/O drive strength is not set to “full.”
4. If RESET (FFh) command is loaded at ready state, the device goes busy for maximum 5µs.
5. Do not issue a new command during tWB, even if R/B# is ready.
6. After power-on, the device goes busy for a maximum of 1 ms.

Table 13. PROGRAM / ERASE Characteristics

Symbol	Parameter	Typ	Max	Unit	Notes
NOP	Number of partial page programs	–	1	Cycle	1
^{t}BERS	BLOCK ERASE operation time	2	10	ms	
^{t}CBSY	Busy time for PROGRAM CACHE operation	3	2,200	µs	2
^{t}DBSY	Busy time for TWO-PLANE PROGRAM PAGE operation	0.5	1	µs	
^{t}LPROG	LAST PAGE PROGRAM operation time	–	–	–	3
^{t}OBSY	Busy time for OTP DATA PROGRAM operation if OTP is protected	–	50	µs	
^{t}PROG	PAGE PROGRAM operation time	900	2,200	µs	

1. One total to the same page.
2. ^{t}CBSY MAX time depends on timing between internal program completion and data in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last – 1 page) – command load time (last page) – address load time (last page) – data load time (last page).



7.0 Command Definitions

Figure 13. Command Set

Command	Command Cycle 1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle 2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	2
PAGE READ CACHE MODE SEQUENTIAL	31h	–	No	–	No	3
PAGE READ CACHE MODE RANDOM	00h	5	No	31h	No	4
PAGE READ CACHE MODE LAST	3Fh	–	No	–	No	
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	2, 5
RANDOM DATA READ	05h	2	No	E0h	No	2
READ ID	90h	1	No	–	No	
READ PARAMETER PAGE	ECh	–	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	2
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	2
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	2, 5
RANDOM DATA INPUT	85h	2	Yes	–	No	2
BLOCK ERASE	60h	3	No	D0h	No	2
RESET	FFh	–	No	–	Yes	2
OTP DATA PROGRAM	A0h	5	Yes	10h	No	
OTP DATA PROTECT	A5h	5	No	10h	No	
OTP DATA READ	AFh	5	No	30h	No	
SET FEATURES	EFh	1	4	–	No	
GET FEATURES	EEh	1	No	–	No	

Notes:
1. Indicates required DATA cycles between COMMAND cycle 1 and COMMAND cycle 2.
2. These commands are valid during busy when an interleaved die operation is being performed.
3. The sequential PAGE READ CACHE MODE command should not be issued prior to reading the last page of a block.
4. When using the random PAGE READ CACHE MODE command, the plane select bit must be the same as the page last read.
5. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE. See plane address boundary definitions for more detail.

Table 14. Two-Plane Command Set (Sheet 1 of 2)

Command	Command Cycle 1	# of Addr Cycles	Command Cycle 2	# of Addr Cycles	Command Cycle 3	Valid During Busy	Notes
TWO-PLANE PAGE READ	00h	5	00h	5	30h	No	—
TWO-PLANE READ for INTERNAL DATA MOVE	00h	5	00h	5	35h	No	1
TWO-PLANE RANDOM DATA READ	06h	5	E0h	–	–	No	2,3
TWO-PLANE/MULTIPLE-DIE READ STATUS	78h	3	–	–	–	Yes	3

Table 14. Two-Plane Command Set (Sheet 2 of 2)

Command	Command Cycle 1	# of Addr Cycles	Command Cycle 2	# of Addr Cycles	Command Cycle 3	Valid During Busy	Notes
TWO-PLANE PROGRAM PAGE	80h	5	11h-80h	5	10h	No	3
TWO-PLANE PROGRAM PAGE CACHE MODE	80h	5	11h-80h	5	15h	No	—
TWO-PLANE PROGRAM for INTERNAL DATA MOVE	85h	5	11h-80h	5	10h	No	—
TWO-PLANE BLOCK ERASE	60h	3	D1h-60h	3	D0h	No	—

Notes:
1. Do not cross plane address boundaries when using TWO-PLANE READ for INTERNAL DATA MOVE and TWO-PLANE PROGRAM for INTERNAL DATA MOVE. See Figure 3 on page 9 for plane address boundary definitions.
2. The TWO-PLANE/MULTIPLE-DIE READ STATUS command must be used to check status during and following interleaved die operations.
3. The commands are valid during busy when interleaved die operations are being performed.

7.1 READ Operations

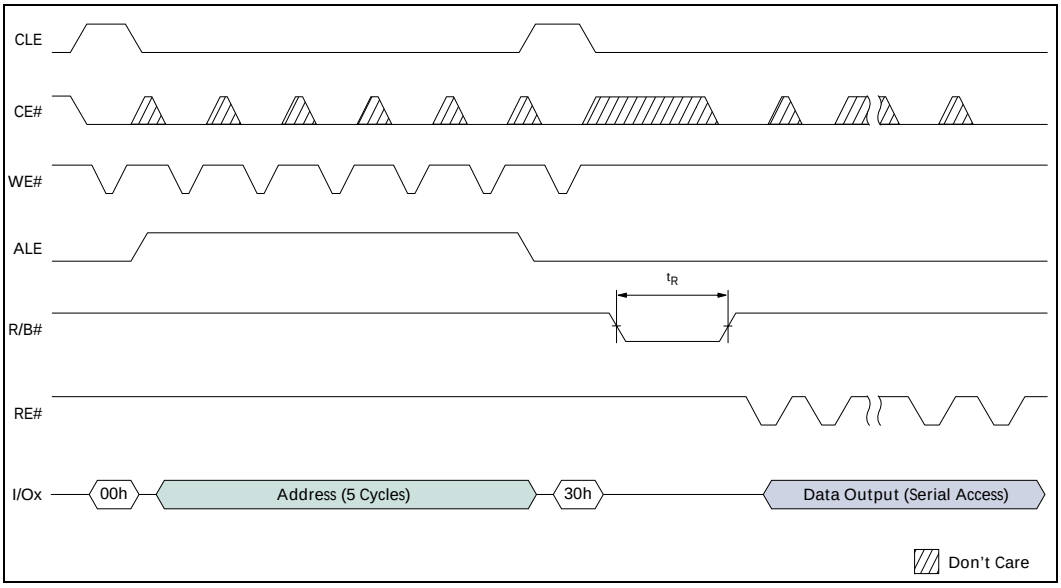
7.1.1 PAGE READ 00h–30h

On power-on the device defaults to READ mode. To enter READ mode while in operation, write the 00h command to the command register, then write five ADDRESS cycles, and conclude with the 30h command.

To determine the progress of the data transfer from the Flash array to the data register (^{t}R), monitor the R/B# signal; or alternately, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must re-issue the READ (00h) command to receive data output from the data register. See Figure 79 on page 77 and Figure 80 on page 78 for examples. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate.

Figure 14. Page Read Operation



7.1.2 RANDOM DATA READ 05h–E0h

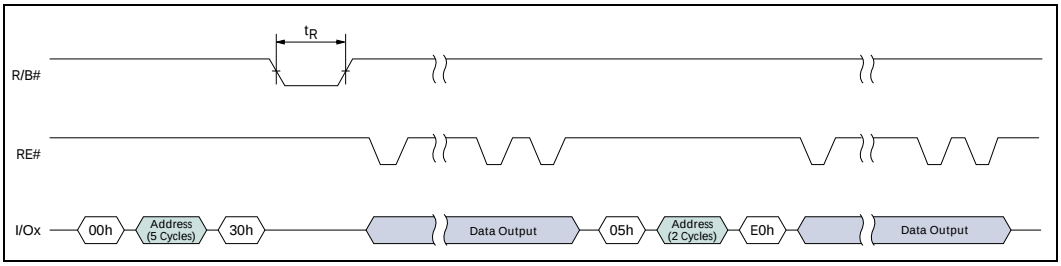
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h sequence).

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (two cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially.

Figure 15. RANDOM DATA READ Operation



7.1.3 PAGE READ CACHE MODE Operations

Intel® NAND Flash devices have a cache register that can be used to increase READ operation speed. Data can be output from the device's cache register while concurrently moving a page from the NAND Flash array to the data register.

To begin a PAGE READ CACHE MODE sequence, begin by reading a page from the NAND Flash array to the cache register using the PAGE READ (00h-30h) command. R/B# goes LOW during ^{t}R (status register bits 6 and 5 = 00). After ^{t}R (R/B# is HIGH and status register bits 6 and 5 = 11), issue either of these commands:

- PAGE READ CACHE MODE SEQUENTIAL (31h) command to begin copying the next sequential page from the NAND Flash array to the data register
- PAGE READ CACHE MODE RANDOM (00h-31h) command to begin copying the page specified in this command from the NAND Flash array to the data register.

After the PAGE READ CACHE MODE SEQUENTIAL or PAGE READ CACHE MODE RANDOM command has been issued, R/B# goes LOW (status register bits 6 and 5 = 00) for tRCBSYR1 while the next page begins copying into the data register. After tRCBSYR1, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that a page is being copied from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

After outputting the desired number of bytes from the cache register, it is possible to either begin an additional PAGE READ CACHE MODE (31h or 00h-31h) operation or issue the PAGE READ CACHE MODE LAST (3Fh) command.

If an additional PAGE READ CACHE MODE (31h or 00h-31h) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for tRCBSYR2 while the data register is copied to the cache register, then the next page begins copying into the data register. After tRCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

If the PAGE READ CACHE MODE LAST (3Fh) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSYR2 while the data register is copied into the cache register. After ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11, indicating that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

During device busy times, ^{t}RCBSYR1 and ^{t}RCBSYR2, the only valid commands are READ STATUS (70h,78h) and RESET (FFh). Until status register bit 5 = 1, the only valid commands during PAGE READ CACHE MODE operations are READ STATUS (70h,78h), READ (00h), PAGE READ CACHE MODE (31h and 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

7.1.3.1 PAGE READ CACHE MODE SEQUENTIAL 31h

The PAGE READ CACHE MODE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. To issue this command, write 31h to the command register.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}RCBSYR1 or ^{t}RCBSYR2. After ^{t}RCBSYR1 or ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

Do not issue the 31h command after reading the last page of the block into the data register. Instead, issue the 3Fh command. Crossing block boundaries with the PAGE READ CACHE MODE SEQUENTIAL (31h) command is prohibited.

7.1.3.2 PAGE READ CACHE MODE RANDOM 00h-31h

The PAGE READ CACHE MODE RANDOM (00h-31h) command reads the specified page into the data register while the previous page is output from the cache register. To issue this command, write 00h to the command register, then write five address cycles to the address register. Conclude the sequence by writing 31h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}RCBSYR1 or ^{t}RCBSYR2. After tRCBSYR1 or ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

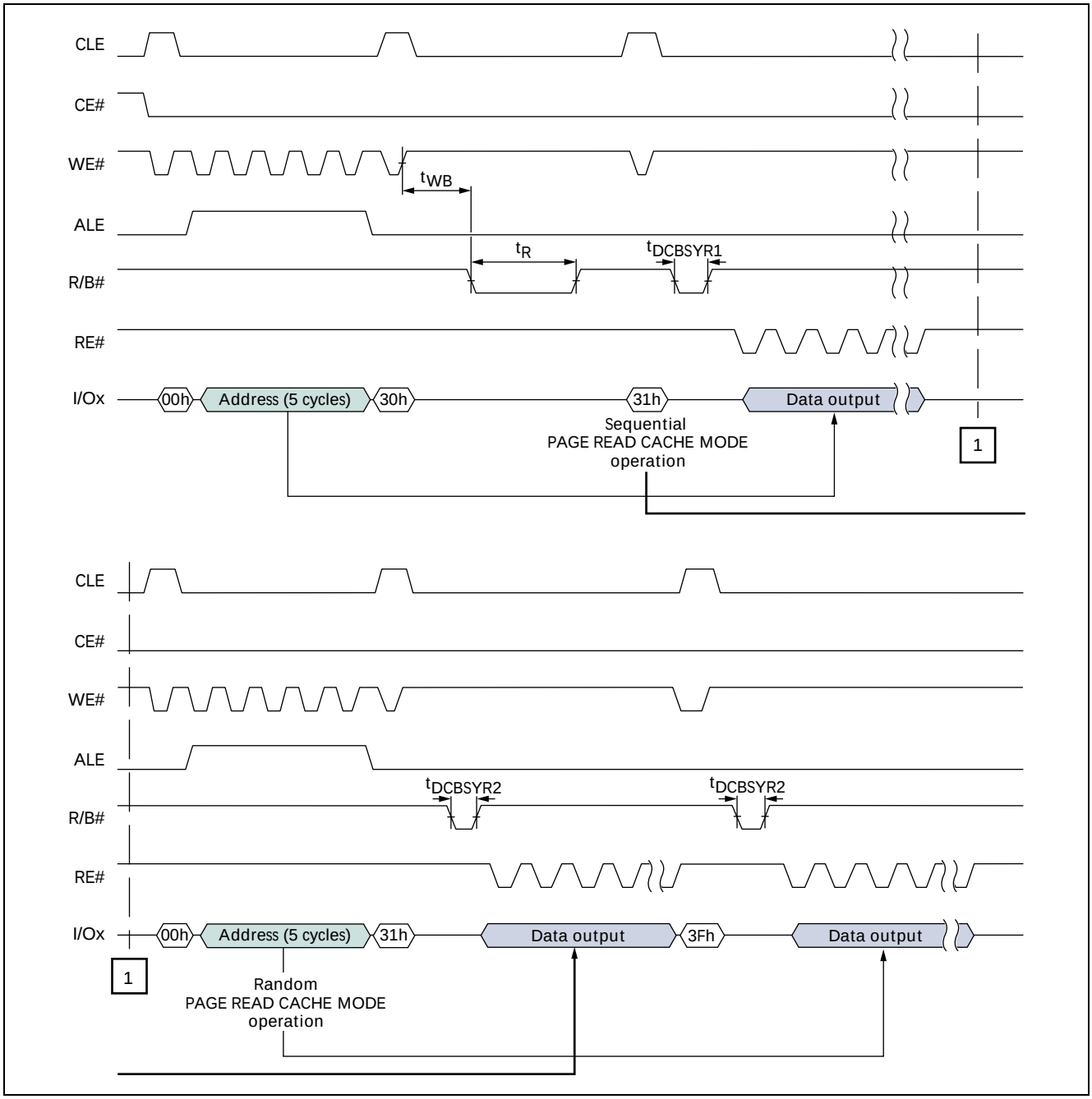
Do not issue the 00h-31h command to a different plane than the previously read page—the plane-select bit must be set to the same value. If crossing plane boundaries is required, complete the PAGE READ CACHE MODE operation using the 3Fh command, then start a PAGE READ (00h-30h) operation to the new plane.

7.1.3.3 PAGE READ CACHE MODE LAST 3Fh

The PAGE READ CACHE MODE LAST (3Fh) command copies a page from the data register to the cache register without beginning a new PAGE READ CACHE MODE operation. To issue the PAGE READ CACHE MODE LAST command, write 3Fh to the command register.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSYR2. After ^{t}RCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11 to indicate that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

Figure 16. Page Read Cache Mode Operation

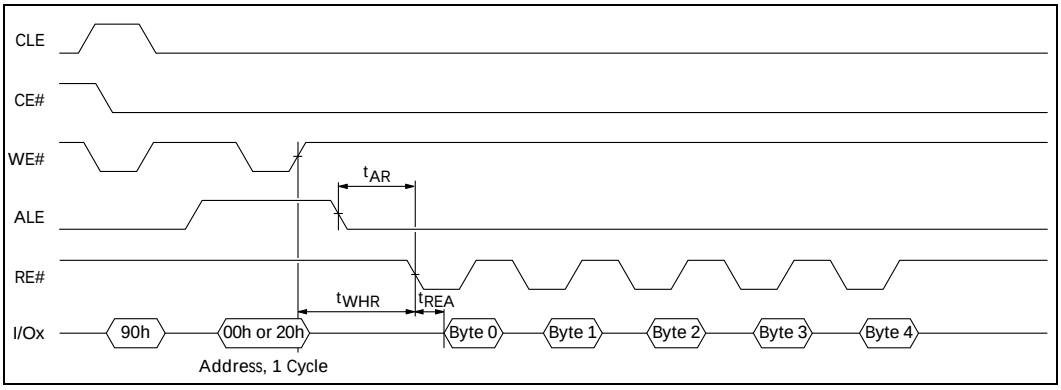


7.1.4 READ ID 90h

The READ ID command is used to read the 5 bytes of identifier codes programmed into the devices. The READ ID command reads a 5-byte table that includes Manufacturer's ID, device configuration, and part-specific information. See Table 15 on page 29, which shows complete listings of all configuration details.

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued. Issuing a READ ID command followed by a 20H on the address bus will read the ONFI id as shown in Table 16 on page 30.

Figure 17. READ ID Operation



Note: See Table 16 on page 30 for byte definitions.

Table 15. Device ID and Configuration Codes for Address 00h

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	Manufacturer ID										
	Intel	1	0	0	0	1	0	0	1	89h	
Byte 1	Device ID										
	8Gb, x8, 3V	1	1	0	1	0	1	0	1	D5h	
	16Gb, x8, 3V	1	1	0	1	0	1	0	1	D5h	2
	32Gb, x8, 3V	1	1	0	1	0	1	1	1	D7h	3
Byte 2											
Number of die per CE	1							0	0	00b	
	2							0	1	01b	
Cell type	MLC					0	1			01b	
Number of simultaneously programmed pages	2			0	1					01b	
Interleaved operations between multiple die	Not supported		0							0b	
	Supported		1							1b	
Cache programming	Supported	1								1b	
Byte value	16Gb device	1	0	0	1	0	1	0	0	94h	
	32Gb device	1	0	0	1	0	1	0	0	94h	
	64Gb device	1	1	0	1	0	1	0	1	D5h	
Byte 3											
Page size	4KB							1	0	10b	

Table 15. Device ID and Configuration Codes for Address 00h (Continued)

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Spare area size (bytes)	218B						1			1b	
Block size (w/o spare)	512KB			1	1					11b	
Organization	x8		0							0b	
Serial access (MIN)	20ns	0				1				0xxx1b	
Byte value		0	0	1	1	1	1	1	0	3Eh	
Byte 4											
Reserved								0	0	00b	
Planes per CE#	2					0	1			01b	
	4					1	0			10b	
Plane size	8Gb		1	1	1					111b	
Reserved		0								0b	
Byte value	16Gb device	0	1	1	1	0	1	0	0	74h	
	32Gb device	0	1	1	1	0	1	0	0	74h	
	64Gb device	0	1	1	1	1	0	0	0	78h	3

1. b = binary
2. Device ID code reflects the configuration of each 16Gb section.
3. Device ID code reflects the configuration of each 32Gb section

Table 16. Device ID and Configuration Codes for ONFI Address (20h)

Address = 20h	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	“O”	0b	1b	0b	0b	1b	1b	1b	1b	4Fh	
Byte 1	“N”	0b	1b	0b	0b	1b	1b	1b	0b	4Eh	
Byte 2	“F”	0b	1b	0b	0b	0b	1b	1b	0b	46h	
Byte 3	“I”	0b	1b	0b	0b	1b	0b	0b	1b	49h	
Byte 4	Undefined	Xb	Xb	Xb	Xb	Xb	Xb	Xb	Xb	XXh	

Note: b = binary, h = hex

7.1.5 READ PARAMETER PAGE ECh

The READ PARAMETER PAGE function retrieves the data structure that describes the device's organization, features, timings, and other behavioral parameters. The data structure is repeated at least five times.

The RANDOM DATA READ (05h-E0h) command is permitted during data output.

Details of the parameter page are listed in Table 17 on page 31.

Figure 18. Read Parameter Page

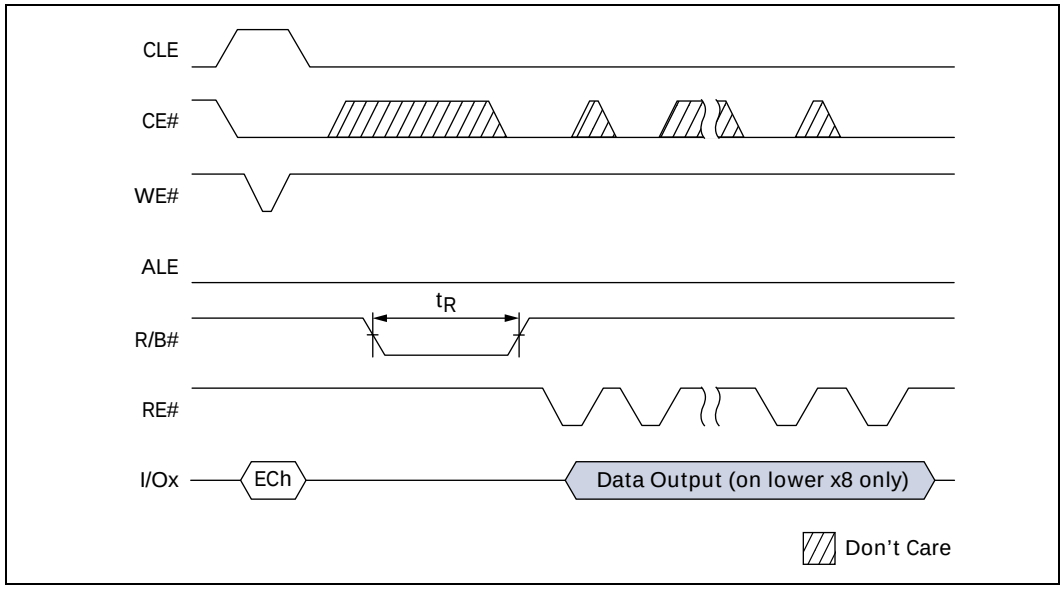


Table 17. Parameter Page Data Structure

Byte	Description	MD516 Value
	Revision Information and Features Block	
0-3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	Revision number Bit 2-15: Reserved (0) Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	02h, 00h
6-7	Features supported Bit 5-15: Reserved (0) Bit 4: 1 = supports odd to even page Copyback Bit 3: 1= supports interleaved operations Bit2: 1= supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit0: 1 = supports 16-bit data bus width	1Ah, 00h

Byte	Description	MD516 Value
8-9	Optional commands supported Bit 6-15: Reserved (0) Bit 5:1 = supports Read Unique ID Bit 4:1 = supports Copyback Bit 3: 1 = supports Read Status Enhanced Bit 2: 1 = supports Get Features and Set Features Bit 1: 1 = supports Read Cache commands Bit 0: 1 = supports Page Cache Program command	1Dh, 00h
10-31	Reserved (0)	
	Manufacturer information block	
32-43	Device manufacturer (12 ASCII characters)	49h, 4Eh, 54h, 45h, 4Ch, 00h, 00h, 00h, 00h, 00h, 00h, 00h
44-63	Device model (20 ASCII characters)	4Ah, 53h, 32h, 39h, 46h, 31h, 36h, 47h, 30h, 38h, 41h, 41h, 4Dh, 43h, 31h, 00h, 00h, 00h, 00h, 00h
64	JEDEC manufacturer ID	89h
65-66	Date code	0Fh, 07h
67-79	Reserved (0)	
	Memory Organization Block	
80-83	Number of data bytes per page	00h, 10h, 00h, 00h
84-85	Number of spare bytes per page	DAh, 00h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	1Bh, 00h
92-95	Number of pages per block	80h, 00h, 00h, 00h
96-99	Number of blocks per logical unit (LUN)	00h, 10h, 00h, 00h
100	Number of logical units (LUNs)	01h
101	Number of address cycles Bit 4-7: Column address cycles Bit 0-3: Row address cycles	23h
102	Number of bits per cell	10h
103-104	Bad blocks maximum per LUN	50h, 00h
105-106	Block endurance	01h, 04h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance for guaranteed valid blocks	E8h, 03h
110	Number of programs per page	01h
111	Partial programming attributes Bit 5-7: Reserved Bit 4:1 = partial page layout is partial page data followed by partial page spare Bit 1-3: Reserved Bit 0: 1 = partial page programming has constraints	00h
112	Number of bits ECC correctability	08h

Byte	Description	MD516 Value
113	Number of interleaved address bits Bit 4-7: Reserved (0) Bit 0-3: Number of interleaved address bits	01h
114	Interleaved operation attributes Bit 4-7: Reserved (0) Bit 3: Address restrictions for program cache Bit 2: 1 = program cache supported Bit 1: 1 = no block address restrictions Bit 0: Overlapped / concurrent interleaving support	0Eh
115-127	Reserved (0)	
	Electrical Parameters Block	
128	I/O pin capacitance	0Ah
129-130	Timing mode support Bit 6-15Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1= supports timing mode 1 Bit 0: 1= supports timing mode 0, shall be 1	1Fh, 00h
131-132	Program cache timing mode support Bit 6-15: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	1Fh, 00h
133-134	tPROG Maximum page program time (µs)	98h, 08h
135-136	tBERS Maximum block erase time (µs)	0Ah, 00h
137-138	tR Maximum page read time (µs)	32h, 00h
139-140	tCCS Minimum change column setup time (ns)	3Ch, 00h
141-163	Reserved (0)	
	Vendor Block	
164-165	Vendor specific Revision number	00h, 00h
166-253	Vendor specific	00h, 00h ...
254-255	Integrity CRC	
	Redundant Parameter Pages	
256-511	Value of bytes 0-255	
512-767	Value of bytes 0-255	
768+	Additional redundant parameter pages	

7.1.6 READ STATUS 70h

The NAND Flash device has an 8-bit status register that the software can read during device operation.

After a READ STATUS command, all READ cycles will be from the status register until a new command is given. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ STATUS cycle to see these changes.

In devices that have more than one die sharing a common CE# pin, the READ STATUS (70h) command reports the status of the die that was last addressed. If concurrent operations are started on both die, then the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command must be used to select the die that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as both die will respond until the next operation is issued.

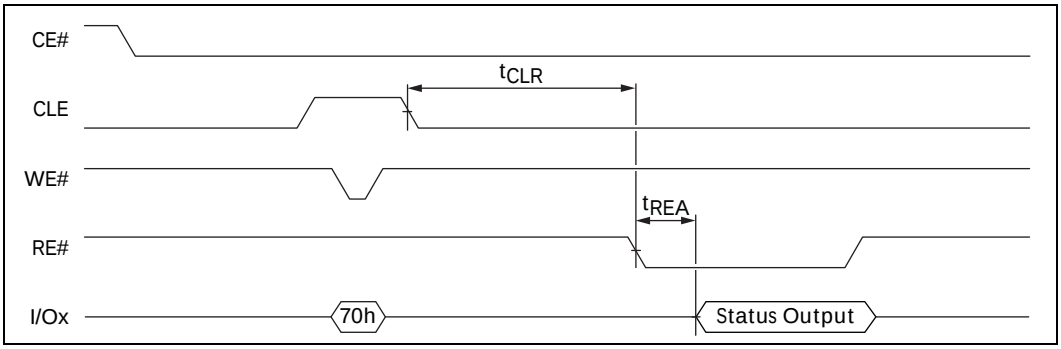
While monitoring the status register to determine when the ^{t}R (transfer from Flash array to data register) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

Table 18. Status Register Bit Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
01	Pass/fail	Pass/fail (N)	–	–	Pass/fail	"0" = Successful PROGRAM/ERASE "1" = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	"0" = Successful PROGRAM "1" = Error in PROGRAM
2	–	–	–	–	–	"0"
3	–	–	–	–	–	"0"
4	–	–	–	–	–	"0"
5	Ready/busy	Ready/busy[2]	Ready/busy	Ready/busy[2]	Ready/busy	"0" = Busy "1" = Ready
6	Ready/busy	Ready/busy cache[3]	Ready/busy	Ready/busy cache[3]	Ready/busy	"0" = Busy "1" = Ready
7[4]	Write protect	Write protect	Write protect	Write protect	Write protect	"0" = Protected "1" = Not protected
[15:8]	–	–	–	–	–	"0"

Notes:
1. Status register bit 0 reports a "1" if a TWO-PLANE PROGRAM operation fails on one or both planes. Status register bit 1 reports a "1" if a TWO-PLANE PROGRAM PAGE CACHE MODE operation fails on one or both planes. Use TWO-PLANE/ MULTIPLE-DIE READ STATUS (78h) to determine the plane to which the operation failed.
2. Status register bit 5 is "0" during the actual programming operation. If cache mode is used, this bit will be "1" when all internal operations are complete.
3. Status register bit 6 is "1" when the cache register is ready to accept new data. R/B# follows bit 6.
4. Status register bit 7 typically mirrors the status of the WP# pin. However, when the OTP PROGRAM DATA command is used, status register bit 7 returns "0" if the OTP area is protected. This bit is not modified until the next PROGRAM or ERASE command is issued.

Figure 19. Status Register Operation



7.2 PROGRAM Operations

7.2.1 PROGRAM PAGE 80h-10h

Intel® NAND Flash devices are inherently page-programmed devices. Pages must be programmed consecutively within a block, the from the least significant page address to the most significant page address; that is, 0, 1, 2, ... 127. Random page address programming is prohibited.

These Intel® NAND Flash devices do not support partial-page programming operations.

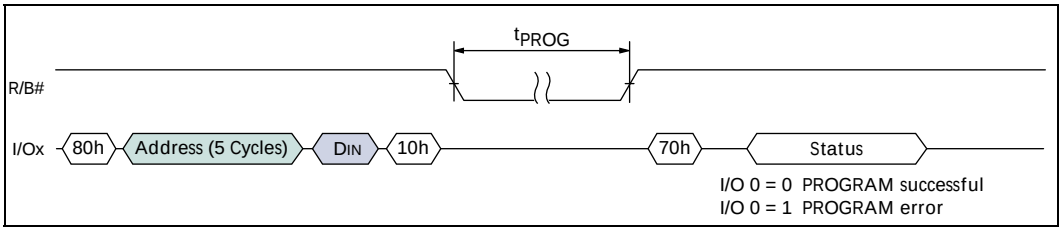
If a RESET (FFh) command is issued during a PROGRAM PAGE operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page will corrupt the data in another page within the block being programmed.

7.2.2 SERIAL DATA INPUT 80h

PROGRAM PAGE operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by five ADDRESS cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address. The PROGRAM (10h) command is written after the data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects “1s” that are not successfully written to “0s.”

R/B# goes low for the duration of array programming time, tPROG. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the programming operation. Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the program operation passed or failed. The command register stays in read status register mode until another valid command is written to it.

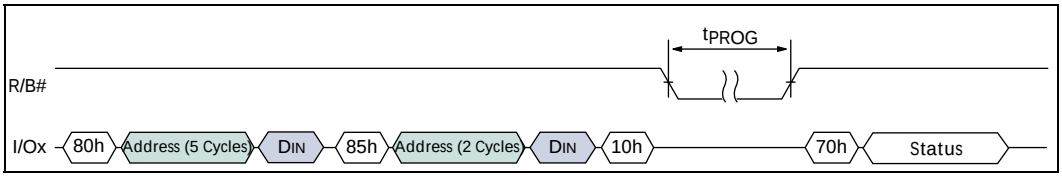
Figure 20. PROGRAM and READ STATUS Operation



7.2.3 RANDOM DATA INPUT 85h

After the initial data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command.

Figure 21. RANDOM DATA INPUT



Note: Command can be 70h or 78h

7.2.4 PROGRAM PAGE CACHE MODE 80h-15h

Cache programming is actually a buffered programming mode of the standard PROGRAM PAGE command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by five cycles of address, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE WRITE (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array. Random data input commands are allowed during Program Page Cache Mode operation.

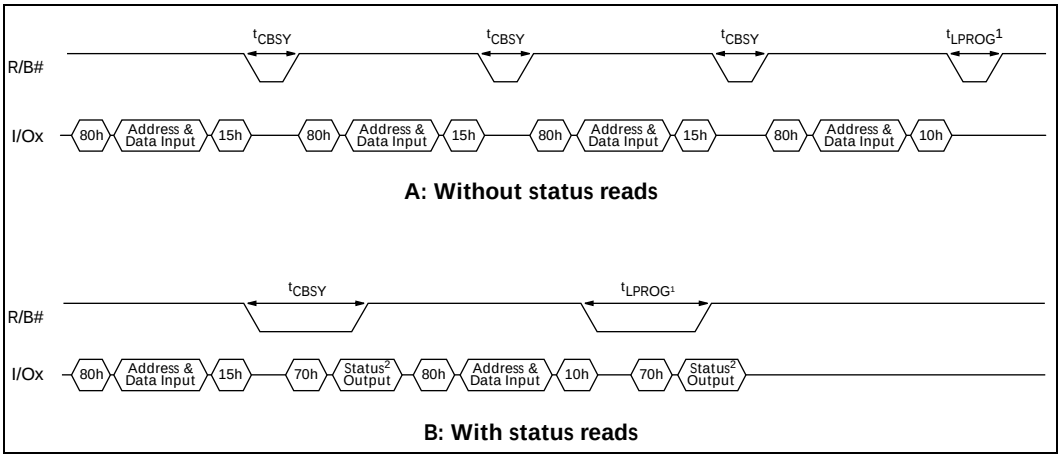
Bit 6 (Cache R/B#) of the status register can be read by issuing the READ STATUS (70h/78h) command to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6. Random Data Input command are allowed during Progam Page Cache Mode opertion (78h).

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

If just the R/B# pin is used to determine programming completion, the last page of the program sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete.

Bit 0 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a "1" (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a "1" (ready state).

Figure 22. PROGRAM PAGE CACHE MODE Example



Note:
1. Check I/O[6:5] for internal ready/busy. Check I/O[1:0] for pass fail. RE# can stay LOW or pulse multiple times after a 70h command.
2. Command can be 70h or 78h

7.3 Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. Data moves are only supported within the plane from which data is read.

7.3.1 READ FOR INTERNAL DATA MOVE 00h-35h

The READ for INTERNAL DATA MOVE (00h-35h) command is used in conjunction with the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. First, 00h is written to the command register, then the internal source address is written (five cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

The written column addresses are ignored even though all five ADDRESS cycles are required.

The memory device is now ready to accept the PROGRAM for INTERNAL DATA MOVE command. Please refer to the description of this command in the following section.

7.3.2 PROGRAM for INTERNAL DATA MOVE 85h-10h

After the READ for INTERNAL DATA MOVE (00h-35h) command has been issued and R/B# goes HIGH, the PROGRAM for INTERNAL DATA MOVE (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register and programming of the new destination page begins. The sequence: 85h, destination address (five cycles), then 10h, is written to the device. After 10h is written, R/B# goes LOW while the control logic automatically programs the new page. The READ STATUS command and bit 6 of the status register can be used instead of the R/B# line to determine when the write is complete. Bit 0 of the status register indicates if the operation was successful.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for INTERNAL DATA MOVE command sequence to modify a word or multiple words of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data is transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h.

Because INTERNAL DATA MOVE operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using INTERNAL DATA MOVE operations also use a robust ECC scheme that can correct two or more bits per sector.

Figure 23. INTERNAL DATA MOVE

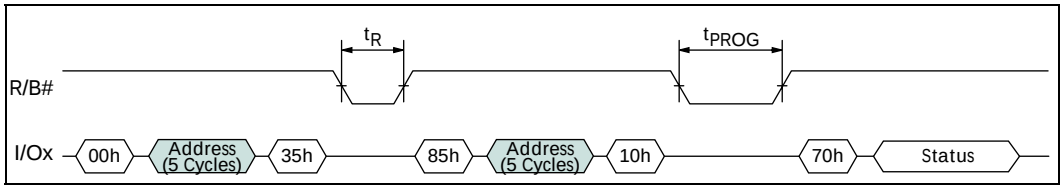
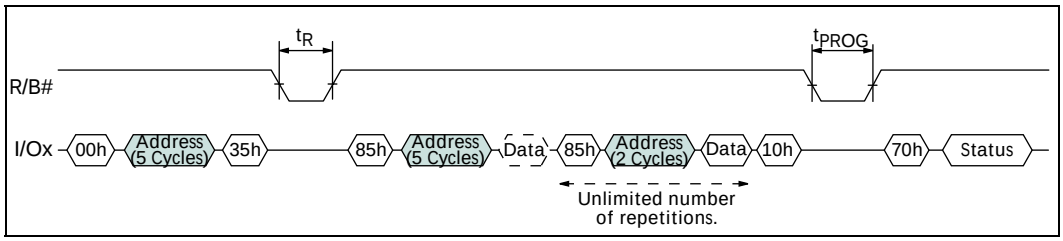


Figure 24. INTERNAL DATA MOVE with RANDOM DATA INPUT



7.4 BLOCK ERASE Operation

7.4.1 BLOCK ERASE 60h-D0h

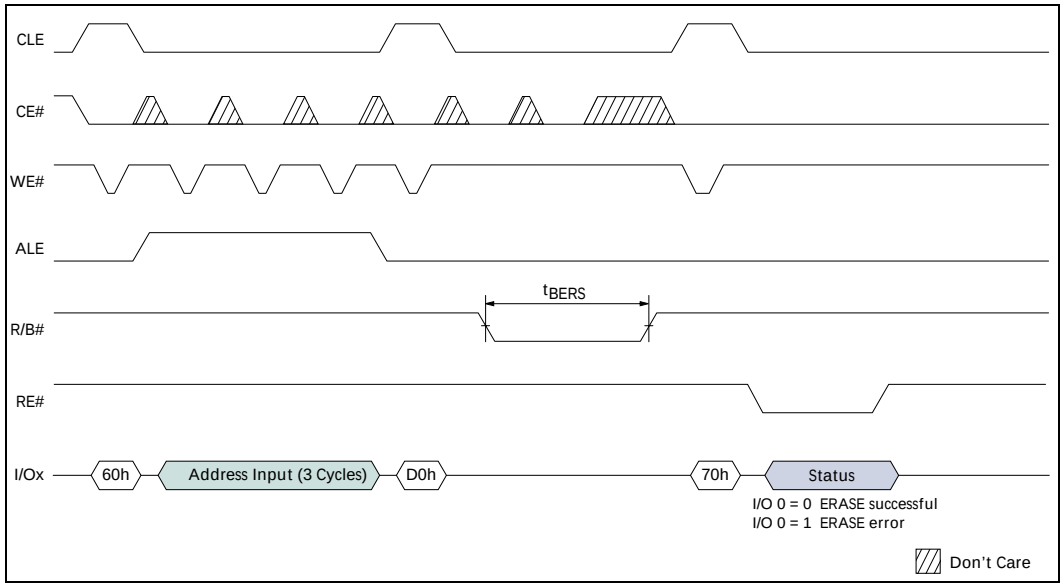
Erasing occurs at the block level. For example, a 4-Gbit device has 4,096 erase blocks, organized into 128 pages per block, 4,224 bytes per page (4,096 + 128 bytes). Each block is 132K bytes (128K + 4K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 25).

Three cycles of addresses of the five cycle addressing are required for a block erase operation. The first of two cycles of addresses must not be used. Although the page address bits are loaded, they are a “Don’t Care” and are ignored for BLOCK ERASE operations. See Section 2.2, “Memory Map and Addressing” on page 8 for addressing details.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then three cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire tBERS erase time.

The READ STATUS (70h/78h) command can be used to check the status of the error. When bit 6 = “1” the ERASE operation is complete. Bit 0 indicates a pass/fail condition where “0” = pass (see Figure 25, and Table 18 on page 34).

Figure 25. BLOCK ERASE Operation



7.5 One-Time Programmable (OTP) Area

This Intel® NAND Flash device offers a protected, one-time programmable Flash memory area. Ten full pages (4,314 bytes) of OTP data is available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Intel® NAND Flash devices, the OTP area leaves the factory in a non-written state (all bits are “1s”). Programming or partial-page programming enables the user to program only “0” bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as “one-time programmable,” Intel provides a unique way to program and verify data—before permanently protecting it and preventing future changes.

OTP programming and protection are accomplished in two discrete operations. First, using the OTP DATA PROGRAM (A0h-10h) command, an OTP page is programmed entirely in one operation, or in up to four partial-page programming sequences. Programming can occur on other pages within the OTP area in a similar manner. Second, the OTP area is permanently protected from further programming using the OTP DATA PROTECT (A5h-10h) command. The pages within the OTP area can always be read using the OTP DATA READ (AFh-30h) command, whether or not it is protected.

To determine whether or not the device is busy during an OTP operation, you can monitor R/B#, or you can use the READ STATUS (71h) or READ STATUS PSEUDO PASS (70h) command. Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS PSEUDO PASS (78h) command is prohibited during and following OTP operations.

7.5.1 OTP DATA PROGRAM A0h-10h

The OTP DATA PROGRAM (A0h-10h) command is used to write data to the pages within the OTP area. An entire page can be programmed at one time, or a page can be partially programmed up to four times. There is no ERASE operation for the OTP pages.

The OTP DATA PROGRAM enables programming into an offset of an OTP page, using the two bytes of column address (CA[11:0]). The command is compatible with the RANDOM DATA INPUT (85h) command. The OTP DATA PROGRAM command will not execute if the OTP area has been protected.

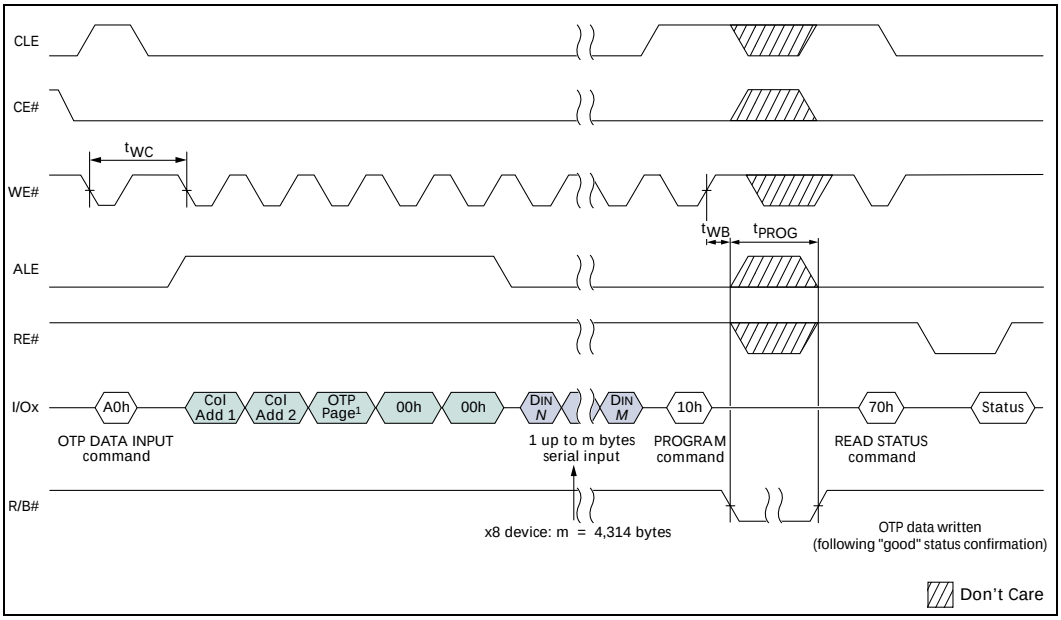
To use the OTP DATA PROGRAM command, issue the A0h command. Issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Next, write from 1 to 4,314 bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification. Program verification only detects “1s” that are not successfully written to “0s.”

R/B# goes LOW during the duration of the array programming time (tPROG). The READ STATUS (70h) command is the only command valid during the OTP DATA PROGRAM operation. Bit 5 of the status register will reflect the state of R/B#. If bit 7 is “0,” then the OTP area has been protected; otherwise, it will be a “1.”

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed.

It is possible to program each MLC OTP page only one time.

Figure 26. OTP DATA PROGRAM

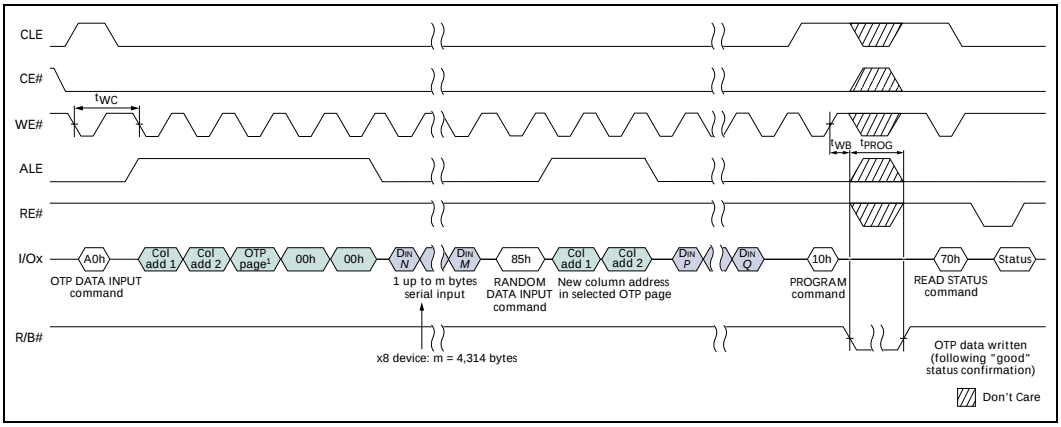


1. The OTP page must be within the range 02h–0Bh.

The OTP DATA PROGRAM command also accepts the RANDOM DATA INPUT (85h) command.

If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for ^{t}DBSY.

Figure 27. OTP PROGRAM with Random Data Input



Note: The OTP page must be within the range 02h–08h.

7.5.2 OTP DATA PROTECT A5h-10h

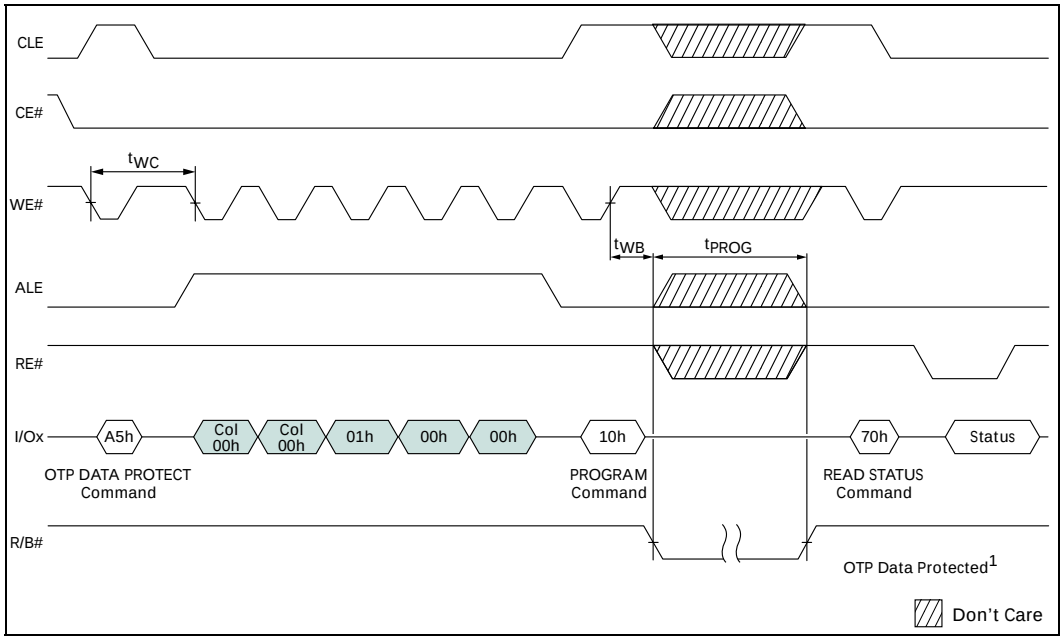
The OTP DATA PROTECT (A5h-10h) command is used to protect all the data in the OTP area. After the data is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the OTP DATA PROTECT command, issue the A5h command. Next, issue the following five ADDRESS cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

R/B# goes LOW while the OTP area is being protected. The protect command duration is similar to a normal page programming operation, tPROG. The READ STATUS (70h) command is the only command valid during the OTP DATA PROTECT operation. Bit 5 of the status register will reflect the state of R/B#.

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed.

Figure 28. OTP DATA PROTECT



1. OTP data is protected following "good" status confirmation.

7.5.3 OTP DATA READ AFh-30h

The OTP DATA READ (AFh-30h) command is used to read data from a page within the OTP area. An OTP page within the OTP area is available for reading data whether or not the area is protected.

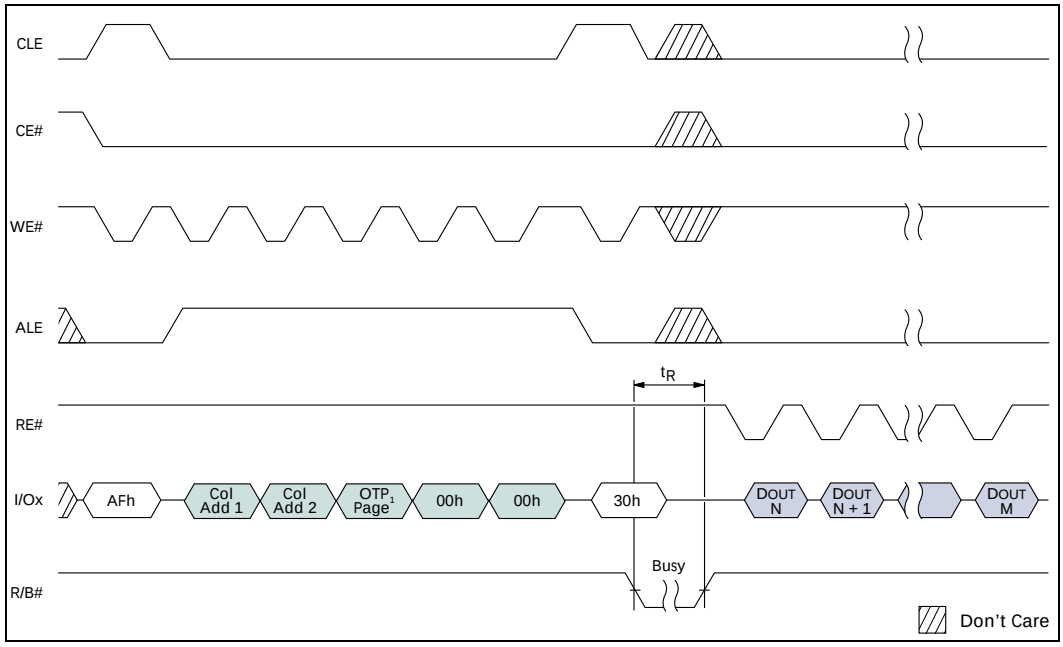
To use the OTP DATA READ command, issue the AFh command. Next, issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Finally, issue the 30h command.

R/B# goes LOW (tR) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the OTP DATA READ operation. Bit 5 of the status register will reflect the state of R/B#..

Normal READ operation timings apply to OTP read accesses. Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

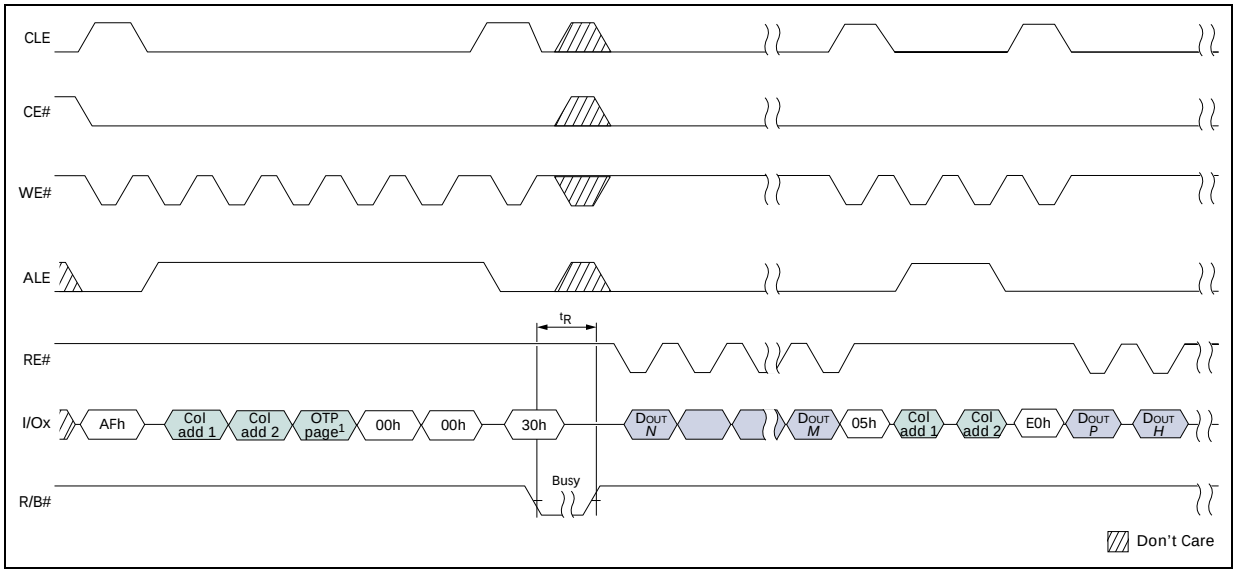
The OTP Data Read command is compatible with Random Data OTP command (105h - E0h).

Figure 29. OTP DATA READ Operation



1. The OTP page must be within the range 02h–0Bh.

Figure 30. OTP Data Read with Random Data Read Operation



7.6 Features Operations

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to alter the NAND Flash device's default behaviors. They use a one-byte Feature Address to determine which feature is to be read or modified. Features are in the range of 0 to FFH.

The GET FEATURES (EEh) command reads the sub-feature parameters (P1-P4) at the specified feature address. The SET FEATURES (EFh) command places parameters at the specified feature address..

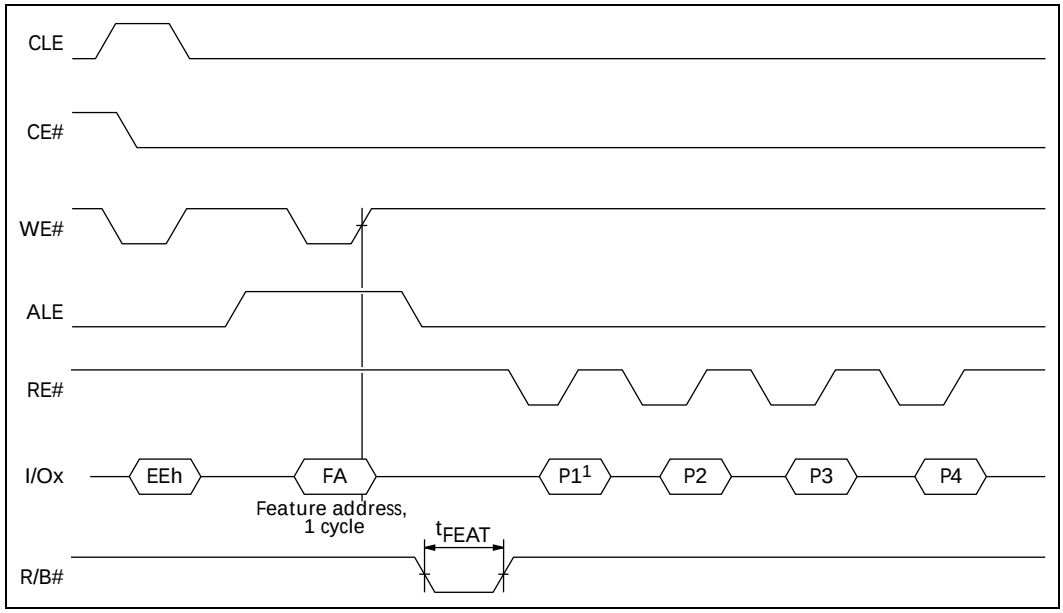
When a feature is set, by default it lasts until the device is power-cycled. It is volatile. Unless otherwise specified in the Features table, once a device is set it remains set, even if a RESET (FFh) command is issued.

7.6.1 GET FEATURES EEh

The GET FEATURES command is used to return the current sub-feature parameters at the specified feature address.

R/B# goes LOW (^{t}FEAT) while the sub-feature parameters are being loaded from the specified feature address. The READ STATUS (70h) command and the RESET (FFh) command are the only commands available during GET FEATURES operation. Bits 5 and 6 of the status register will reflect the state of R/B#.

Figure 31. Get Features Operation



7.6.2 SET FEATURES EFh

The SET FEATURES command is used to set the sub-feature parameters at a specified feature address. These parameters are stored in the device until the device is powered down. The sub-feature parameters are applied to all die on the CE# to which this command is issued.

R/B# goes LOW for ^{t}FEAT while the sub-feature parameters are written to the specified feature address. The READ STATUS (70h) command and the RESET (FFh) command are the only valid commands during SET FEATURES operation. Bits 5 and 6 of the status register will reflect the state of R/B#.

Figure 32. Set Features Operation

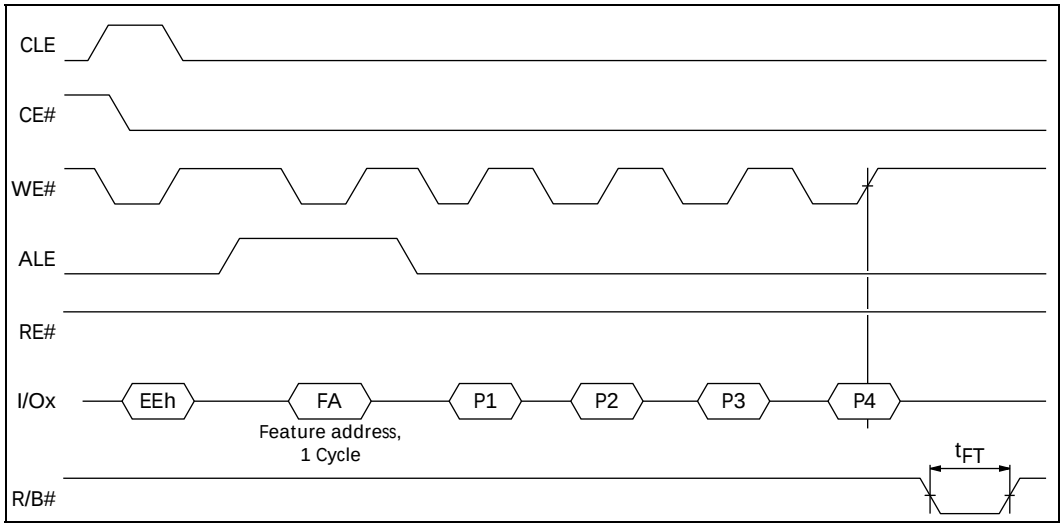


Table 19. Features Table

Feature Address	Description
00h	Reserved
01h	Timing Mode
02h	Cache timing mode
02h–7Fh	Reserved
80h	Vendor-specific parameter: Prog I/O drive strength
81h	Programmable R/B# Pull-Down Strength
82h-FFh	Reserved

Table 20. Feature 01h Timing Mode

Feature Parameter	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
P1	Reserved (0)				Timing mode number			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

TO DO: Add definitions for 81h, 82h.

7.7 TWO-PLANE Operations

This NAND Flash device is divided into two physical planes. Each plane contains a 4,314-byte data register, a 4,314-byte cache register, and a 2,048-block Flash array. Two-plane commands make better use of the flash arrays on these physical planes by performing PROGRAM, READ, or ERASE operations simultaneously, significantly improving system performance.

7.7.1 Two-Plane Addressing

Two-plane commands require two addresses, one address per plane. These two addresses are subject to the following requirements:

- The least significant block address bit, BA7, must be different for both addresses.
- The most significant block address bit, BA19, must be identical for both addresses.
- The page address bits, PA[6:0], must be identical for both addresses.

7.7.2 TWO-PLANE PAGE READ 00h-00h-30h

The TWO-PLANE PAGE READ (00h-00h-30h) operation is similar to the PAGE READ (00h-30h) operation. It transfers two pages of data from the Flash array to the data registers. Each page must be from a different plane on the same die.

To enter the TWO-PLANE PAGE READ mode, write the 00h command to the command register, then write five ADDRESS cycles for plane 0 (BA7 = “0”). Next, write the 00h command to the command register, then write five ADDRESS cycles for plane 1 (BA7 = “1”). Finally, issue the 30h command. The first plane and second plane addresses must meet the two-plane addressing requirements, and, in addition, they must have identical column addresses.

After the 30h command is written, page data is transferred from both planes to their respective data registers in tR. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# returns HIGH. To read out the data from the plane 0 data register, pulse RE# repeatedly. After the data cycle from the plane 0 address completes, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the plane 1 address, then repeatedly pulse RE# to read out the data from the plane 1 data register.

Alternately, the READ STATUS (70h) command can monitor the data transfers. When the transfers are complete, status register bit 6 is set to “1.” To read data from one of the two planes, the user must first issue the TWO-PLANE RANDOM DATA READ (06h-E0h) command followed by five ADDRESS cycles. To read out data from the plane and column address specified with the TWO-PLANE RANDOM DATA READ command, pulse RE# repeatedly. When the data cycle is complete, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the other plane. To output the data beginning at the specified column address, pulse RE# repeatedly.

Note: It is prohibited to use Two-Plane/Multiple Die Read Status operation during and following a Two Plane Page Read operation.

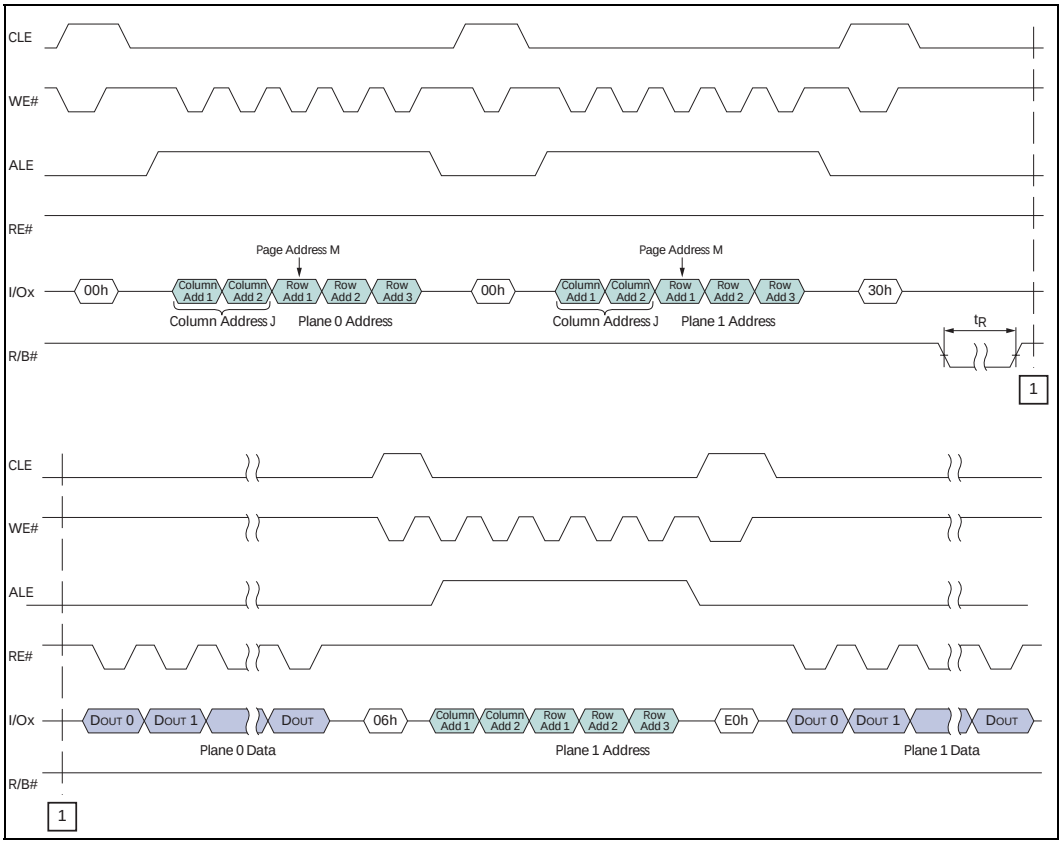
7.7.3 TWO-PLANE RANDOM DATA READ 06h-E0h

The TWO-PLANE RANDOM DATA READ (06h-E0h) command selects a plane and column address from which to read data after a TWO-PLANE PAGE READ (00h-00h-30h) command.

To issue a TWO-PLANE RANDOM DATA READ command, issue the 06h command, then five ADDRESS cycles, and follow with the E0h command. Pulse RE# repeatedly to read data from the new plane beginning at the specified column address.

The primary purpose of the TWO-PLANE RANDOM DATA READ command is to select a new plane and column address within that plane. If a new plane does not need to be selected, then it is possible to use the RANDOM DATA READ (05h-E0h) command instead.

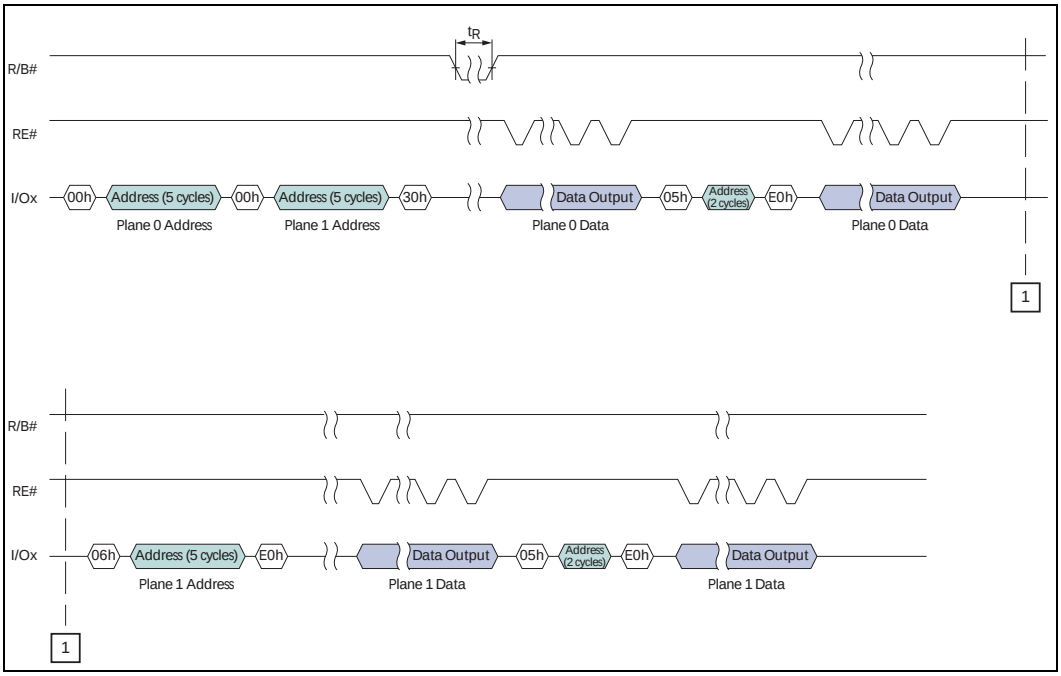
Figure 33. Two-Plane Page Read



Notes:

1. Column and page addresses must be the same.
2. The least-significant block address bit, BA7, must not be the same for the first and second plane addresses.

Figure 34. TWO-PLANE PAGE READ with RANDOM DATA READ



7.7.4 TWO-PLANE PROGRAM PAGE 80h-11h-81h-10h

The TWO-PLANE PROGRAM PAGE (80h-11h-81h-10h) operation is similar to the PROGRAM PAGE (80h-10h) operation. It programs two pages of data from the data registers to the Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to most significant page address. Random page programming within a block is prohibited. The first plane address and the second plane address must meet the two-plane addressing requirements.

To begin the TWO-PLANE PROGRAM PAGE operation, write the 80h command to the command register; write five ADDRESS cycles for the first plane; then write the data. Serial data is loaded on consecutive WE# cycles starting at the given address. Next, write the 11h command. The 11h command is a “dummy” command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for tDBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to “1.” The only valid commands during tDBSY are READ STATUS (70h) and RESET (FFh).

After tDBSY, write the 81h command to the command register; write five ADDRESS cycles for the second plane; then write the data. The PROGRAM (10h) command is written after the second-plane data input is complete.

After the 10h command is written, the control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operations to both planes. WRITE verification only detects “1s” that are not successfully written to “0s.”

R/B# goes LOW for the duration of the array programming time (tPROG). When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during tPROG are READ STATUS (70h), TWO-PLANE/ MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page will corrupt the data in another page within the block being programmed.

When the device is ready, if the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = "1"), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

During serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane.

Figure 35. TWO-PLANE PROGRAM PAGE

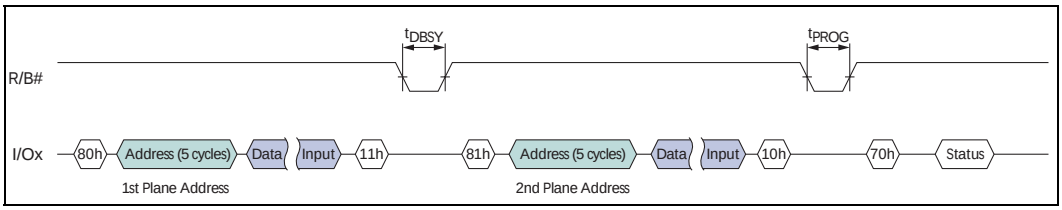
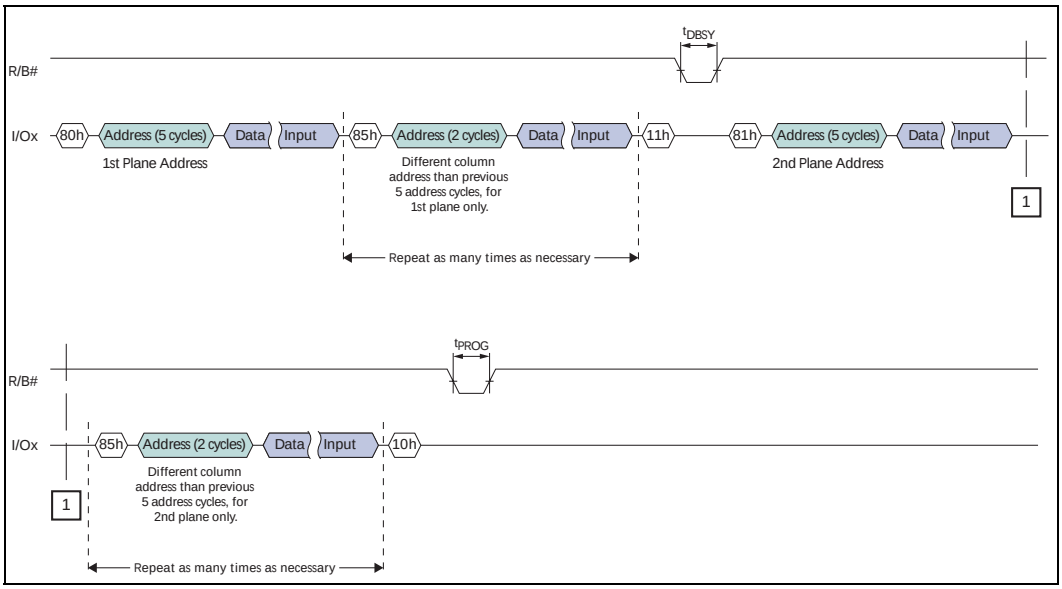


Figure 36. TWO-PLANE PROGRAM PAGE with RANDOM DATA INPUT



7.7.5 TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h

The TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) operation is similar to the PROGRAM PAGE CACHE MODE (80h-15h) operation. It cache programs two pages of data from the data registers to the NAND Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be

programmed consecutively from the least significant to the most significant page address. Random page programming within a block is prohibited. The first-plane and second-plane address must meet the two-plane addressing requirements.

To enter the TWO-PLANE PROGRAM PAGE CACHE MODE, write the 80h command to the command register, write 5 ADDRESS cycles for the first plane, then write the data. Serial data is loaded on consecutive WE# cycles, starting at the given address. Next, write the 11h command. The 11h command is a “dummy” command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS command also indicates that the device is ready when status register bit 6 is set to “1.”

The PROGRAM PAGE CACHE MODE command can cross block boundaries; it cannot cross die boundaries.

The only valid commands during ^{t}DBSY are READ STATUS (70h, 71h, 78h, 79h) and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register, write 5 ADDRESS cycles for the second plane, then write the data. The CACHE WRITE (15h) command is written after the second-plane data input is complete. Data is transferred from the cache registers to the data registers on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data registers and R/B# returns HIGH, memory array programming to both planes begins.

When R/B# returns HIGH, new data can be written to the cache registers by issuing another TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) sequence. The time that R/B# stays LOW (^{t}CBSY) is determined by the actual programming time of the previous operation. For the first cache operation, ^{t}CBSY duration is the time it takes for the data to be copied from the cache registers to the data registers. On the second and subsequent TWO-PLANE PROGRAM PAGE CACHE MODE operations, transfer from the cache registers to the data registers is delayed until the contents of the current data registers have been programmed into the arrays.

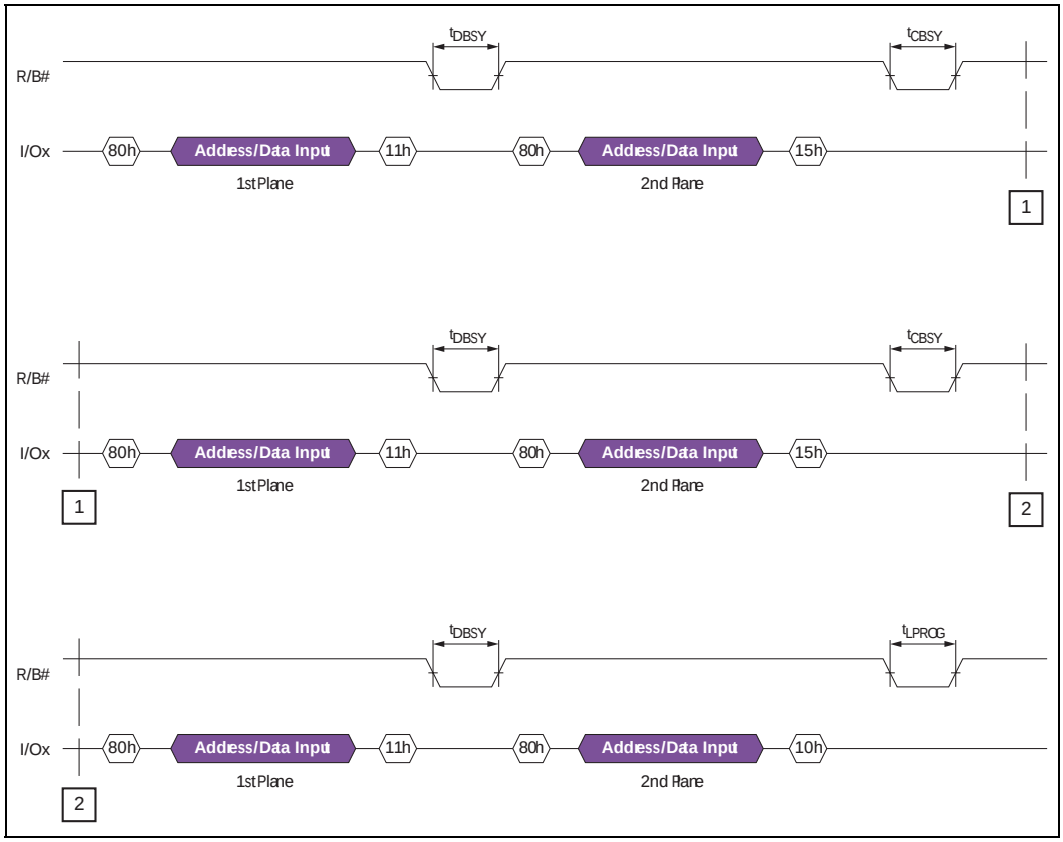
If the R/B# pin is used to determine programming completion, the last operation of the program sequence must use the TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) command instead of the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command. If the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command is used for the last operation, then use READ STATUS (70h, 78h, 79h) to monitor the operation's progress; status register bit 5 indicates when programming is complete.

To determine when the current TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-10h) operation has completed, issue the READ STATUS (71h) or the READ STATUS PSEUDO PASS (70h) command and check status register bits 5 and 6. When the device is ready, use status register bit 0 to determine if the current operation passed and status register bit 1 to determine if the previous operation passed. If either bit 0 = 1 or bit 1 = 1, indicating a failed operation, then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (79h) or the TWO-PLANE/MULTIPLE-DIE READ STATUS PSEUDO PASS (78h) command twice—once for each plane—to determine which current or previous plane operation failed.

During the serial data input for either plane, the RANDOM DATA INPUT (85h) command may be used any number of times to change the column address within that plane.

If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page will corrupt the data in another page within the block being programmed.

Figure 37. TWO-PLANE PROGRAM PAGE CACHE MODE



7.7.6 TWO-PLANE INTERNAL DATA MOVE 00h-00h-35h/85h-11h-85h-10h

A TWO-PLANE INTERNAL DATA MOVE operation is similar to an INTERNAL DATA MOVE operation, and requires two sequences. Issue a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command first, then the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command. Data moves are only supported within the planes from which data is read. The first plane and second plane addresses must meet the two-plane addressing requirements for both the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) and TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) commands.

7.7.7 TWO-PLANE READ for INTERNAL DATA MOVE 00h-00h-35h

The TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is used in conjunction with the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command. First, write 00h to the command register, then write the first-plane internal source address (5 cycles). Again, write 00h to the command register, followed by the second-plane internal source address (5 cycles). Finally, write 35h to the command register. After the 35h command, R/B# goes LOW for tR while two pages are read into their respective cache registers.

After a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is issued, the data transferred from the source pages into the cache registers may be read out by toggling RE#. Data is output sequentially from the column address originally specified by the TWO-PLANE READ FOR INTERNAL DATA MOVE (00h-00h-35h) command, starting with plane 0.

A TWO-PLANE RANDOM DATA READ (06h-E0h) command can be used to select the data transferred from the source pages of each plane. This command will change the starting column address on only the plane being selected. The column address on the plane moved from will remain unchanged from its previous location.

To read out data after the TWO-PLANE READ for INTERNAL DATA MOVE command, you can issue either the TWO-PLANE RANDOM DATA READ (06h-E0h) command without limit, or you can issue a combination of TWO-PLANE/MULTIPLE-DIE READ STATUS and RANDOM DATA READ (05h-E0h) commands.

The memory device is now ready to accept the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command.

Alternatively, two READ for INTERNAL DATA MOVE (00h-35h) commands may be issued, each addressing different planes on the same die, prior to issuing the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command.

7.7.8 TWO-PLANE PROGRAM for INTERNAL DATA MOVE 85h-11h-85h-10h

After the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command has been issued and R/B# goes HIGH (or the status register bit 6 is “1”), the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command is used. Pages must be read from and programmed to the same plane.

First, write 85h to the command register, then write the first plane destination address (five cycles), then write 11h to the command register. The 11h command is a “dummy” command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for tDBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to “1.” The only valid commands during tDBSY are READ STATUS (70h) and RESET (FFh).

After tDBSY, write the 85h command to the command register, then write the second plane destination address (five cycles), then write 10h to the command register. Data is transferred from the cache registers to the data registers on the rising edge of WE#, and programming begins on both planes.

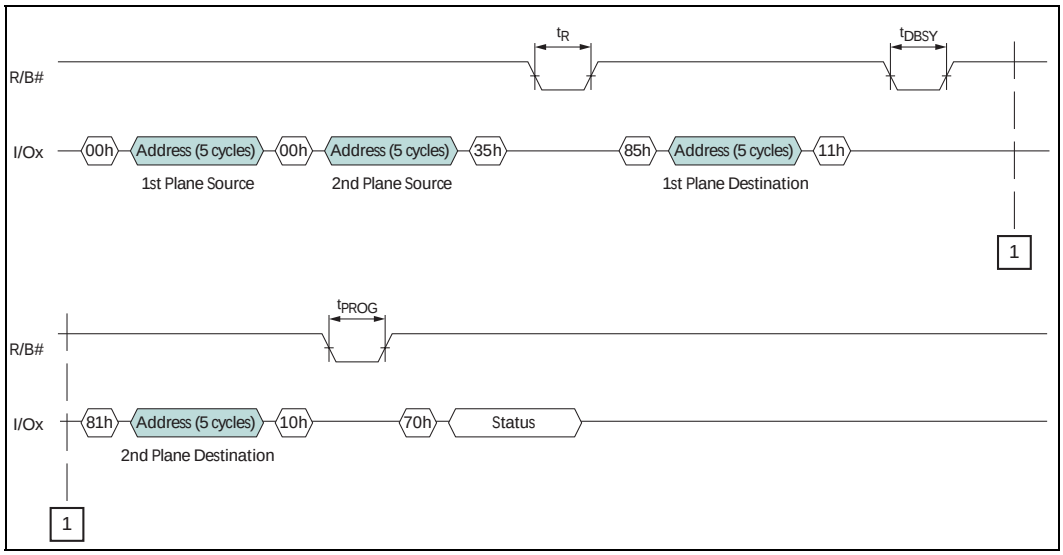
R/B# goes LOW for the duration of array programming time, tPROG. When programming and verification is complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to “1.” The only valid commands during tPROG are READ STATUS (70h), TWO-PLANE/ MULTIPLE-DIE READ STATUS (78h), and RESET (FFh).

If a RESET (FFh) command is issued during a TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page will corrupt the data in another page within the block being programmed.

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = “1”), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

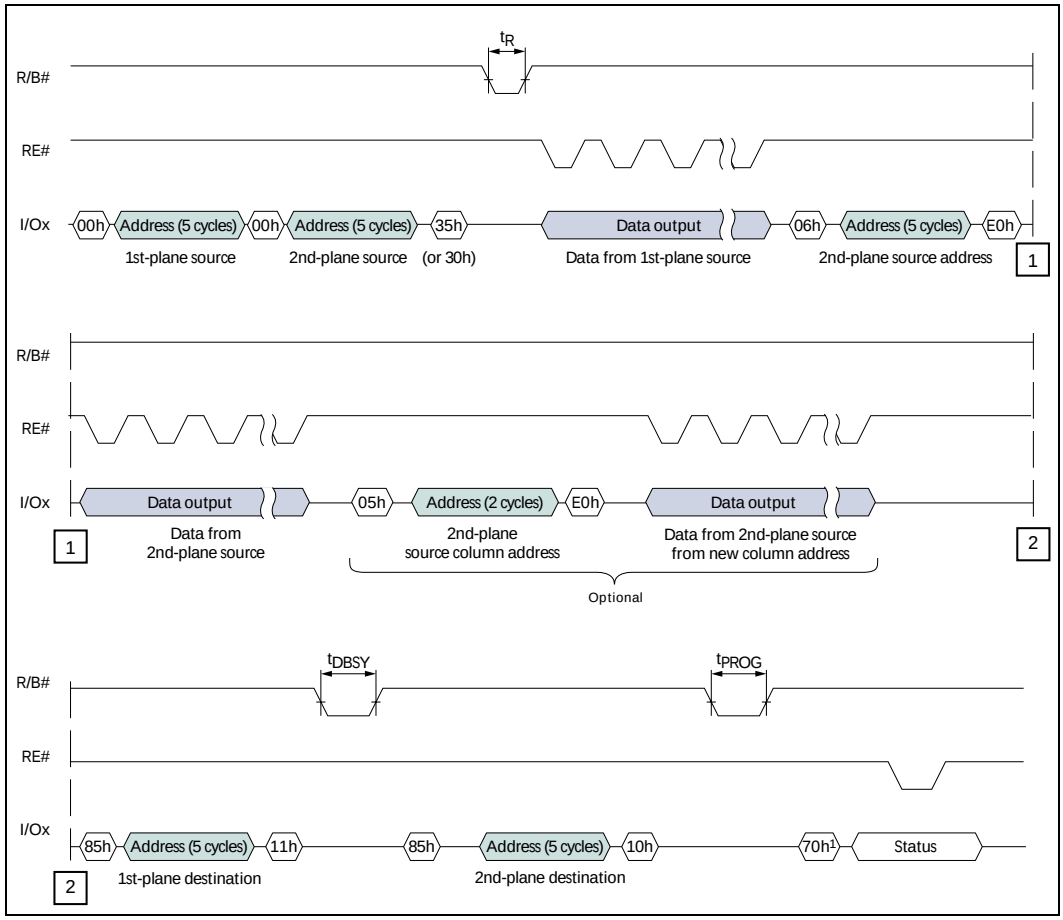
During the serial data input for either plane, the RANDOM DATA INPUT (85h) command may be used any number of times to change the column address within that plane.

Figure 38. TWO-PLANE INTERNAL DATA MOVE



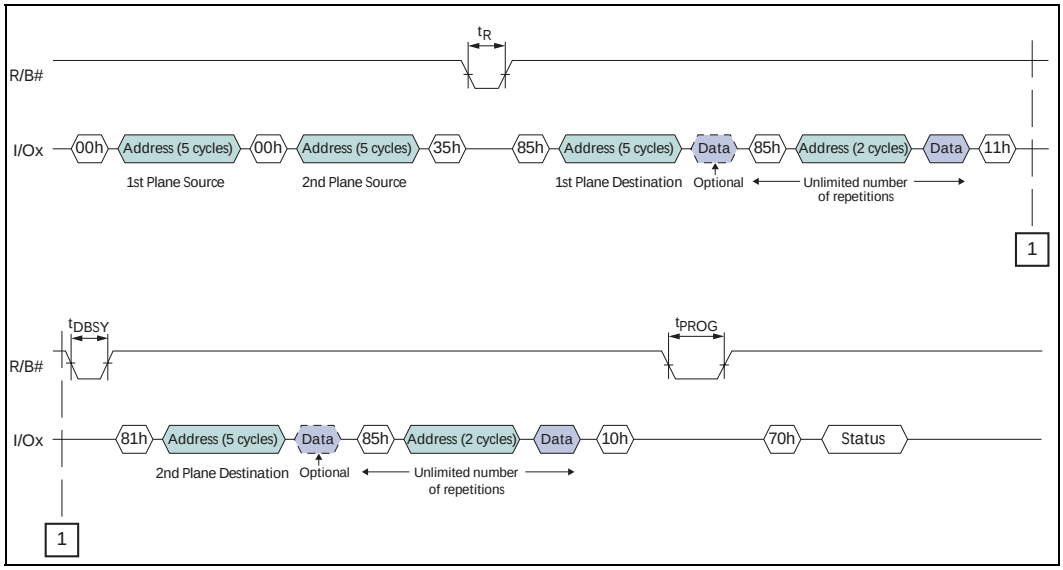
Note: Command can be 70h or 78h

Figure 39. TWO-PLANE INTERNAL DATA MOVE with TWO PLANE RANDOM DATA READ



Note: Command can be 70h or 78h

Figure 40. TWO-PLANE INTERNAL DATA MOVE with RANDOM DATA INPUT



Note: Command can be 70h or 78h

7.7.9 TWO-PLANE BLOCK ERASE 60h-D1h-60h-D0h

The TWO-PLANE BLOCK ERASE (60h-D1h-60h-D0h) operation is similar to the BLOCK ERASE (60h-D0h) operation. It erases two blocks instead of one. The blocks to be erased must be on different planes on the same die. The first-plane and second-plane addresses must meet the two-plane addressing requirements.

To begin the TWO-PLANE BLOCK ERASE operation, write the 60h command to the command register, followed by 3 ADDRESS cycles of the first-plane block address. Next, write the D1h command. The D1h command is a “dummy” command. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when the status register bit 6 is set to “1.” The only valid commands during ^{t}DBSY are READ STATUS (70h, 78h) and RESET (FFh).

After ^{t}DBSY, write the 60h command to the command register followed by 3 ADDRESS cycles for the second plane. Finally, issue the D0h command.

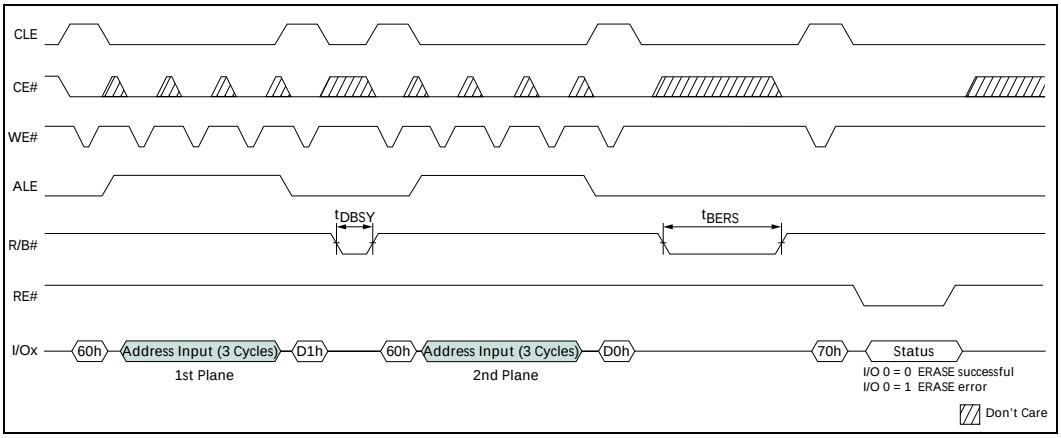
R/B# goes LOW for the duration of block erase time, ^{t}BERS. When block erasure is complete, R/B# returns HIGH. A READ STATUS command also indicates that the device is ready when status register bit 6 is set to “1.”

The only valid commands during ^{t}BERS are READ STATUS (70h, 78h,) commands and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = “1”), then use the TWO-PLANE/ MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

Alternatively, the D1h command may be omitted. In this case, there is no ^{t}DBSY time.

Figure 41. TWO-PLANE BLOCK ERASE Operation



7.8 Interleaved Die Operations

In devices that have more than one die sharing a common CE# pin, it is possible to significantly improve performance by interleaving operations between the die. When both die are idle (R/B# is HIGH or status register bit 5 is “1”), issue a command to the first die. Then, while the first die is busy (R/B# is LOW), issue a command to the other die.

7.8.1 TWO-PLANE/MULTIPLE-DIE READ STATUS 78h

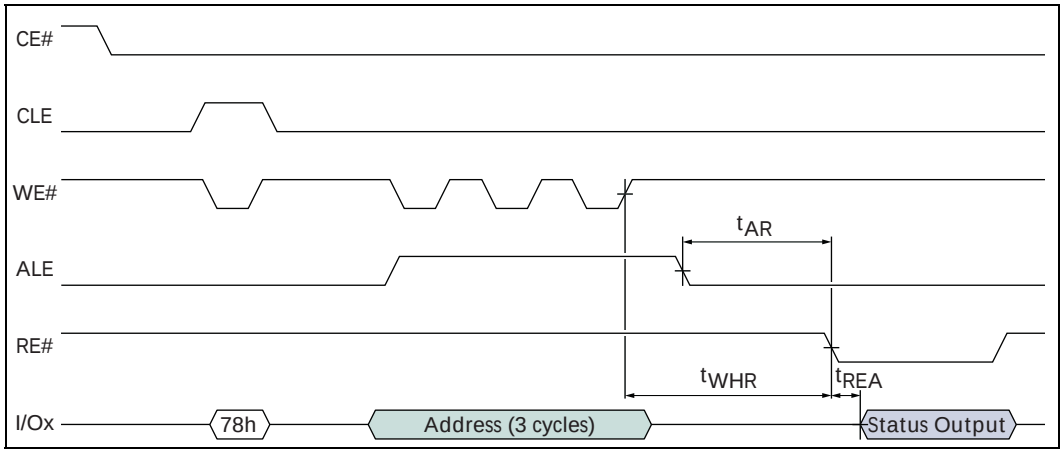
There are two methods to determine operation completion. The R/B# signal indicates when both die have finished their operations. R/B# remains LOW while either die is busy. When R/B# goes HIGH, then both die are idle and the operations are complete. Alternatively,the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command can report the status of each die individually. If a die is performing a cache operation, like PROGRAM PAGE CACHE MODE (80h-15h) or TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h), then the die is able to accept the data for another cache operation when status register bit 6 is “1.” All operations, including cache operations, are complete on a die when status register bit 5 is “1.”

During and following interleaved die operations, theREAD STATUS (70h) commandis prohibited. Instead, use the 78hcommand to monitor status. These commands select which die will report status. Interleaved two-plane commands must also meet the requirements in “Two-Plane Addressing” on page 47.

PAGE READ,PROGRAM PAGE, PROGRAM PAGE CACHE MODE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, BLOCK ERASE, and TWO-PLANE BLOCK ERASE can be used in any combination as interleaved operations on separate dies that share a common CE#.

In interleaved PROGRAM and READ operations, the PROGRAM operation must be issued before the READ operation. The data from the READ operation must be read out before the next PROGRAM operation.

Figure 42. TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle



7.8.2 Interleaved PROGRAM PAGE Operations

Shown here are two ways to determine if the interleaved PROGRAM PAGE operation is complete:

- Monitor the R/B# signal
- Issue the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command to monitor the status register

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE operations.

Figure 43. Monitor R/B# to Determine Interleaved PROGRAM PAGE Completion

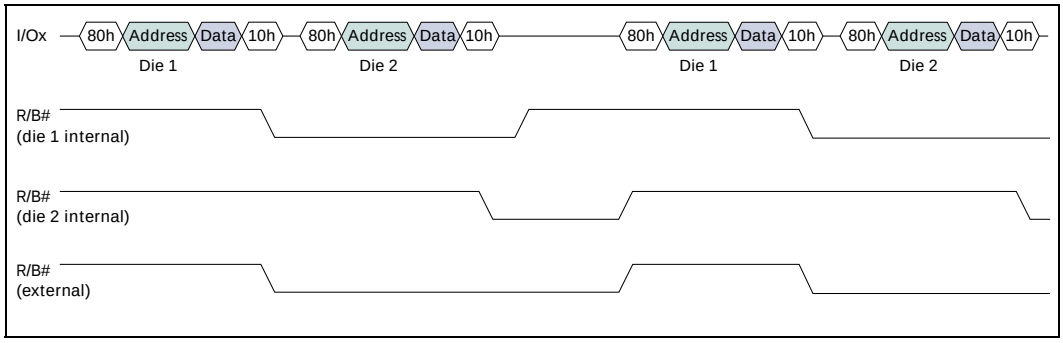
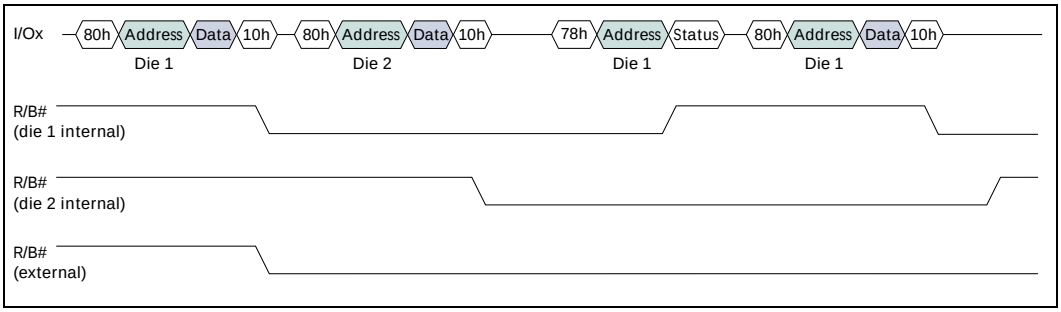


Figure 44. Monitor Status Register to Determine Interleaved PROGRAM PAGE Completion



7.8.3 Interleaved PROGRAM PAGE CACHE MODE Operations

Shown here are two ways to determine if the interleaved PROGRAM PAGE CACHE MODE operation is complete:

- Monitor the R/B# signal
- Issue the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command to monitor the status register

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE CACHE MODE operations.

Figure 45. Monitor R/B# to Determine Interleaved PROGRAM PAGE CACHE MODE Completion

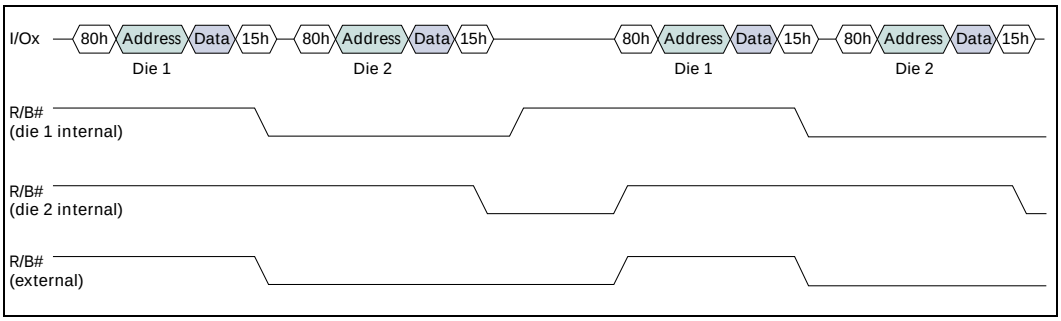
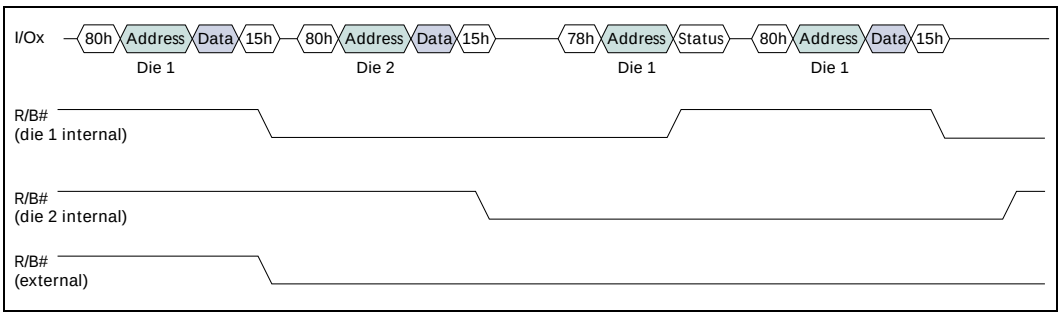


Figure 46. Monitor Status Register to Determine Interleaved PROGRAM PAGE CACHE MODE Completion



7.8.4 Interleaved TWO-PLANE PROGRAM PAGE Operation

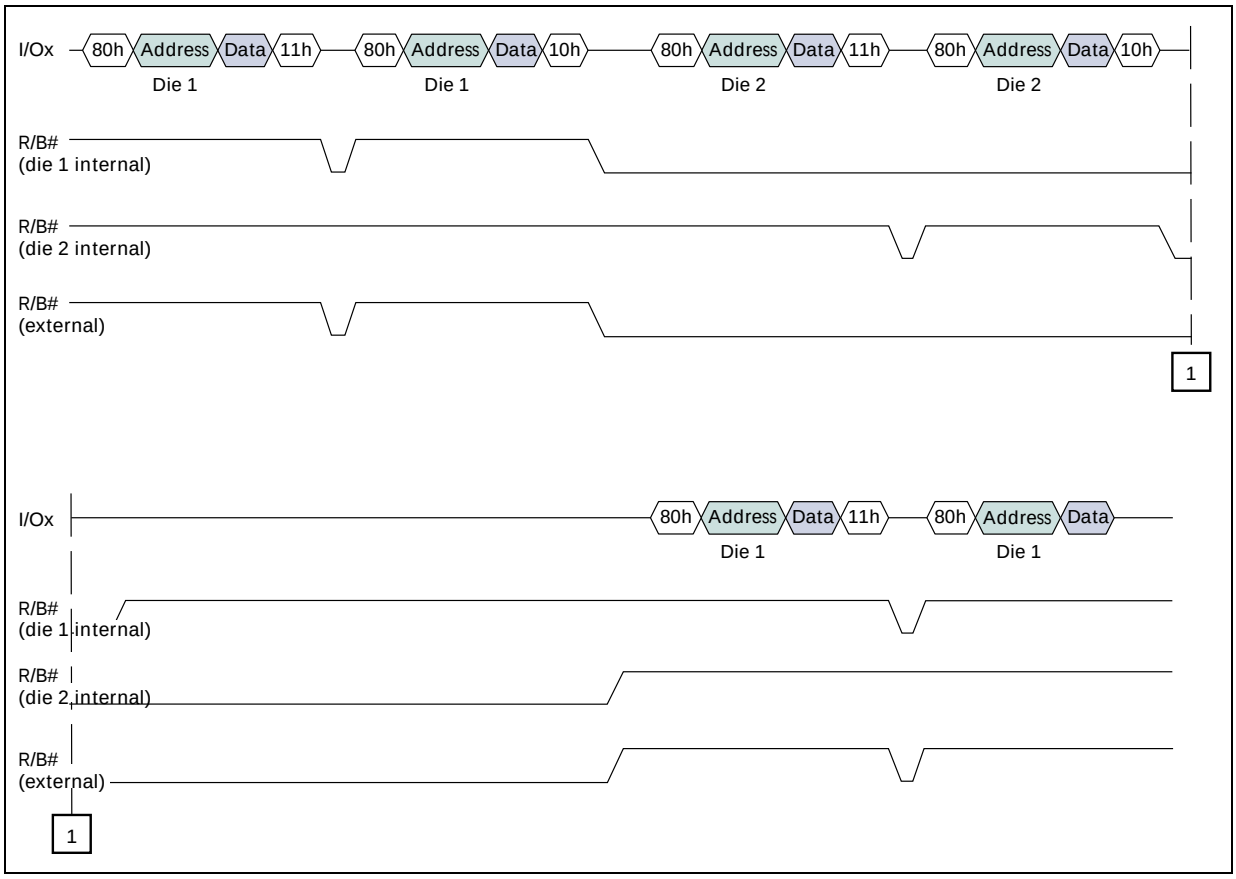
Shown here are two ways to determine if the interleaved TWO-PLANE PROGRAM PAGE operation is complete:

- Monitor the R/B# signal
- Issue the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command to monitor the status register

The interleaved TWO-PLANE PROGRAM PAGE operation must meet two-plane addressing requirements.

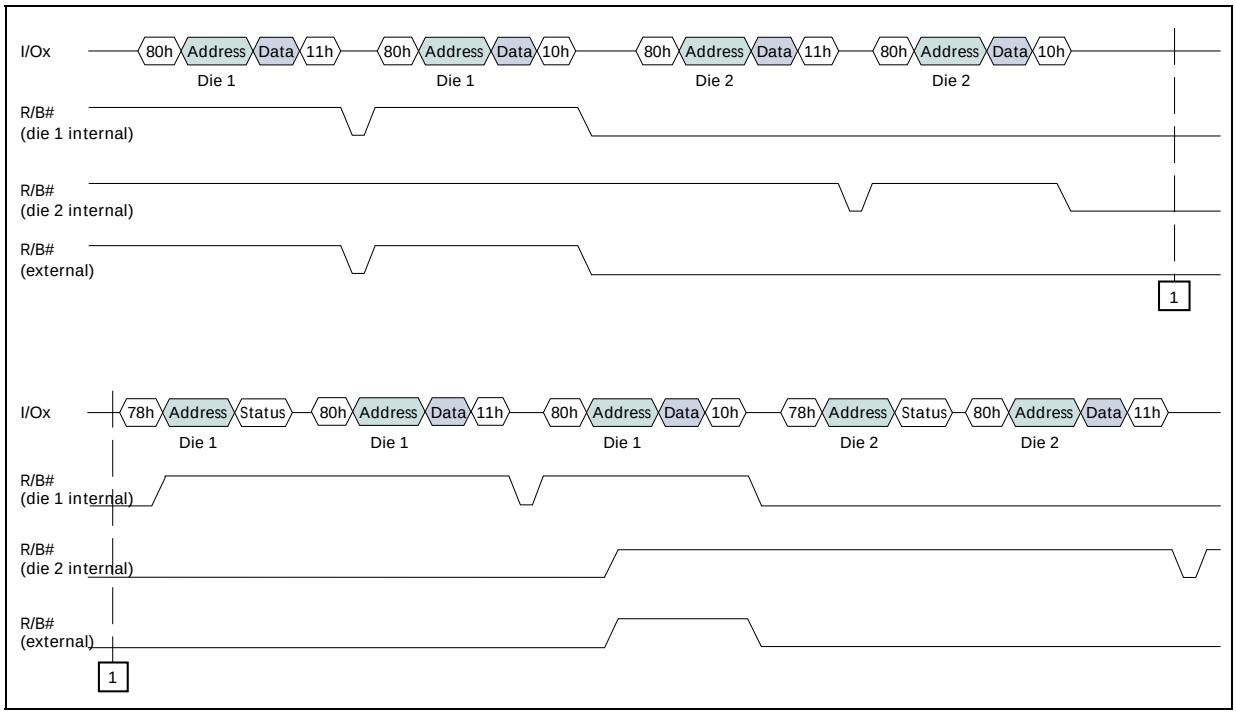
RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE operations.

Figure 47. Monitor R/B# to Determine Interleaved TWO-PLANE PROGRAM PAGE Completion



Note: Two-plane addressing requirements apply.

Figure 48. Monitor Status Register to Determine Interleaved TWO-PLANE PROGRAM PAGE Completion



Note: Two-plane addressing requirements apply.

7.8.5 Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE Operations

Shown here are two ways to determine if the interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operation is complete:

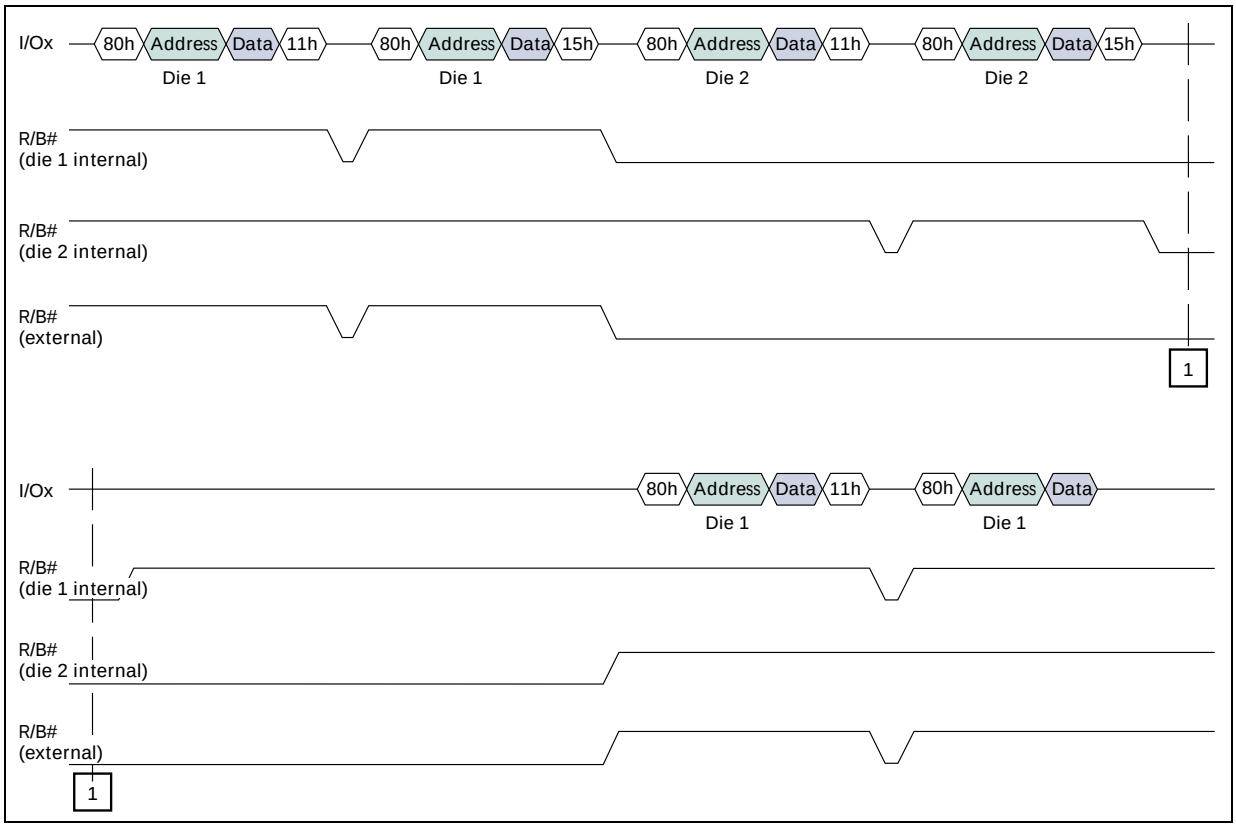
- Monitor the R/B# signal
- Issue the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command to monitor the status register

The interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operation must meet two-plane addressing requirements.

RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations.

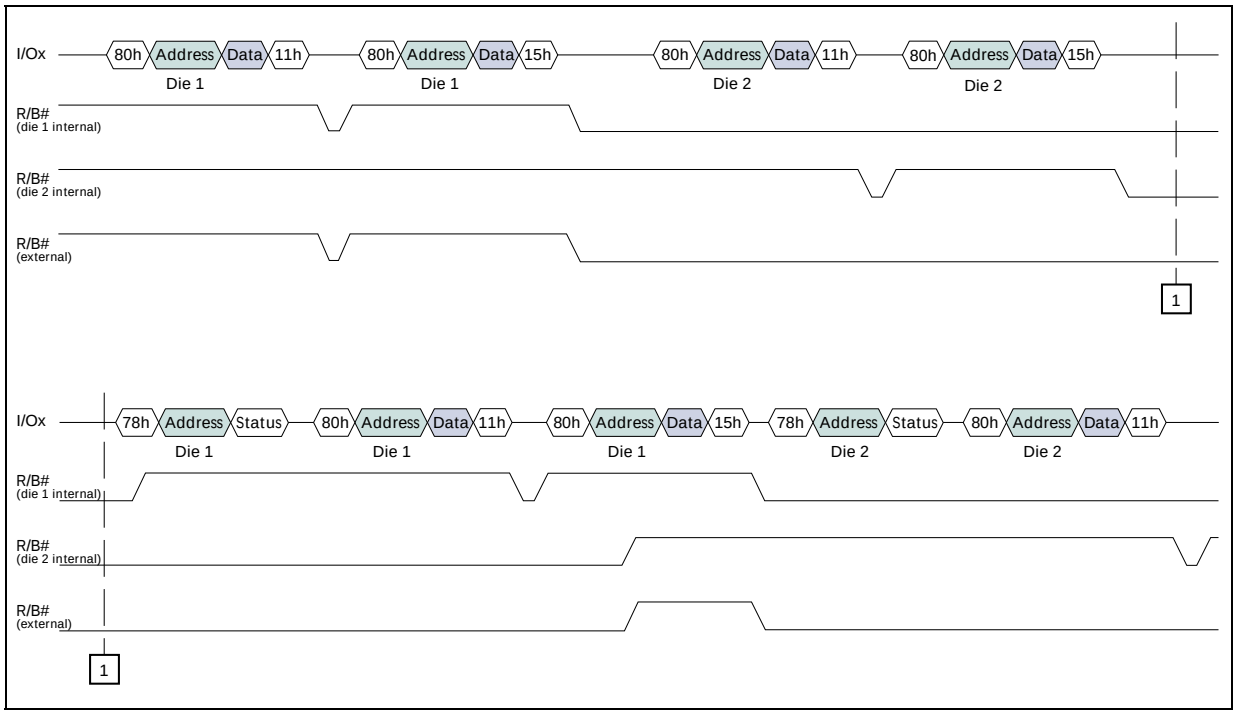
A RANDOM DATA INPUT command will change the starting column address on only the plane and die currently being programmed. The column addresses from any other planes will remain unchanged from their previous locations.

Figure 49. Monitor R/B# to Determine Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE Completion



Note: Two-plane addressing requirements apply.

Figure 50. Monitor Status Register to Determine Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE Completion



Note: Two-plane addressing requirements apply.

7.8.6 Interleaved BLOCK ERASE Operations

Shown here are two ways to determine if the interleaved BLOCK ERASE operation is complete:

- Monitor the R/B# signal
- Issue the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command to monitor the status register

TheTWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command is used to monitor the status register for operation completion.

Figure 51. Monitor R/B# to Determine Interleaved BLOCK ERASE Completion

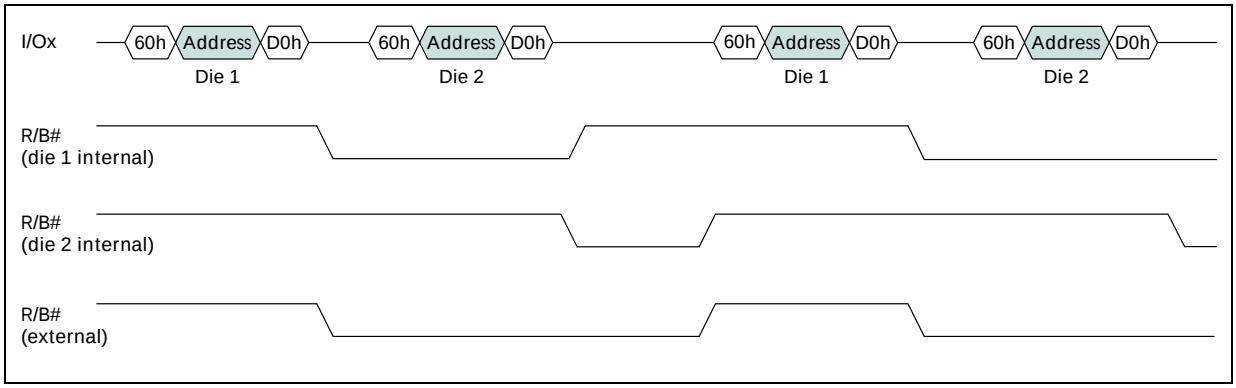
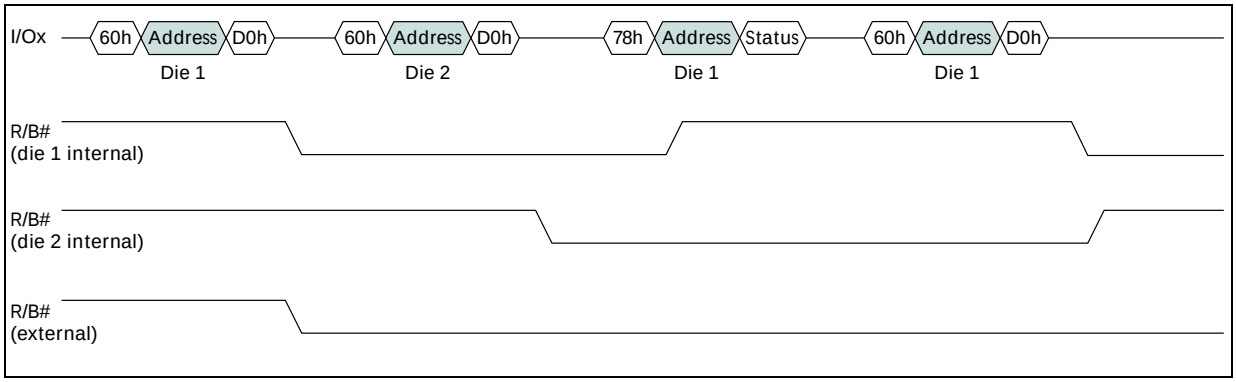


Figure 52. Monitor Status Register to Determine Interleaved BLOCK ERASE Completion



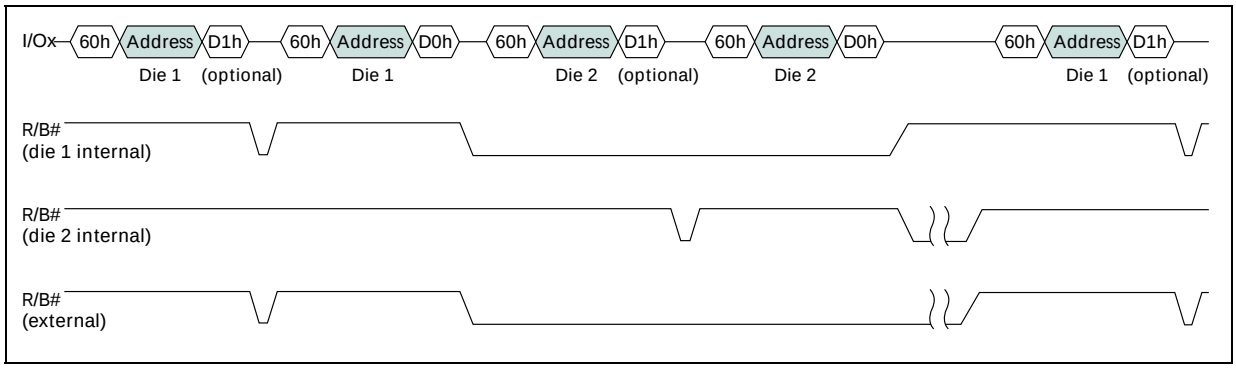
7.8.7 Interleaved TWO-PLANE BLOCK ERASE Operations

Shown here are two ways to determine if the interleaved TWO-PLANE BLOCK ERASE operation is complete:

- Monitor the R/B# signal
- Issue the TWO-PLANE/MULTIPLE-DIE READ STATUS(78h) command to monitor the status register

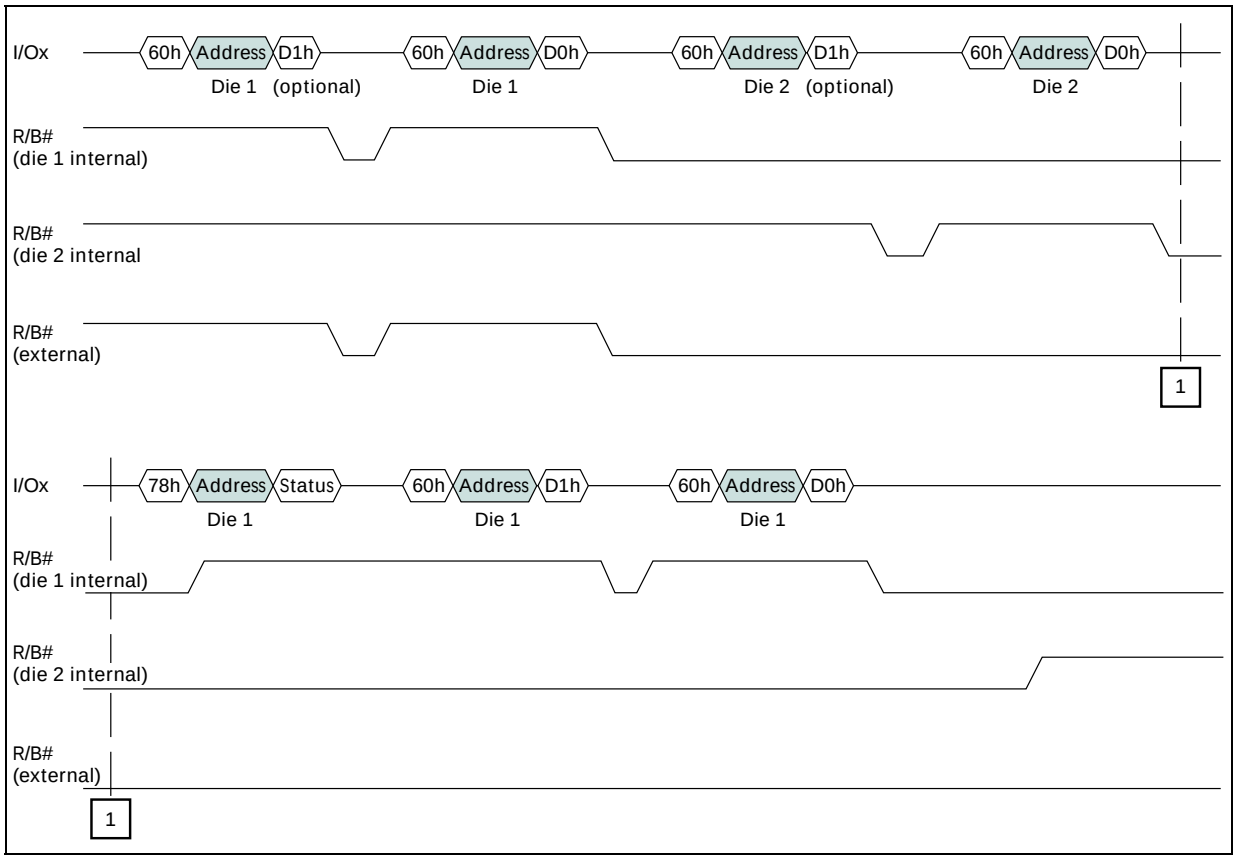
The interleaved TWO-PLANE BLOCK ERASE operation must meet two-plane addressing requirements.

Figure 53. Monitor R/B# to Determine Interleaved TWO-PLANE BLOCK ERASE Completion



Note: Two-plane addressing requirements apply.

Figure 54. Monitor Status Register to Determine Interleaved TWO-PLANE BLOCK ERASE Completion



Note: Two-plane addressing requirements apply.

7.9 RESET Operation

7.9.1 RESET FFh

The RESET (FFh) command is used to put the memory device into a known condition and to abort a command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

If a RESET (FFh) command is issued during any type of programming operation (PROGRAM PAGE, PROGRAM PAGE CACHE MODE, PROGRAM for INTERNAL DATA MOVE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, or TWO-PLANE PROGRAM for INTERNAL DATA MOVE) while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting any programming operation on one page will corrupt the data in another page within the block being programmed.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes low for tRST after the RESET command is written to the command register.

The RESET command must be issued to all CE#s after power-on. The device will be busy for a maximum of 1ms. During and following the initial RESET command, and prior to issuing the next command, use of the TWO PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited.

Figure 55. RESET Operation

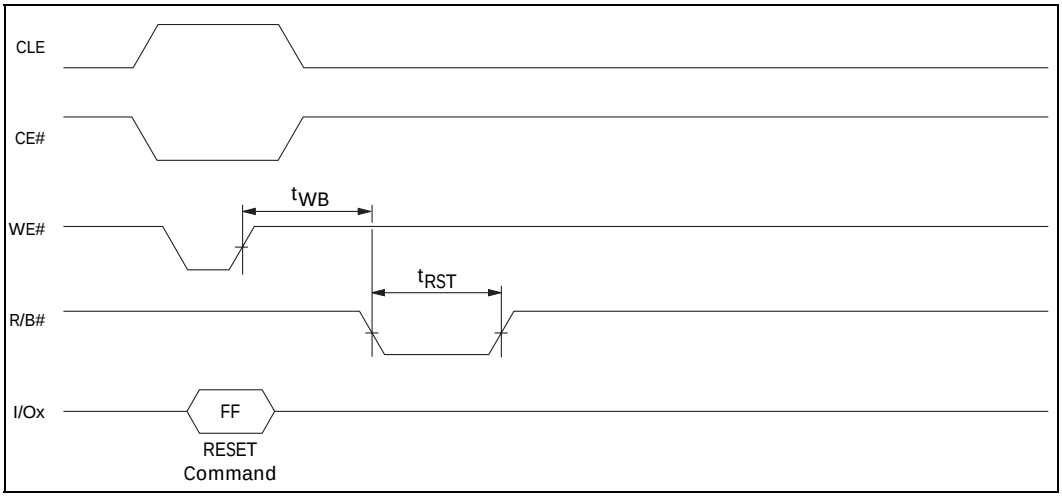


Table 21. Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

7.10 WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using WP#. The Enable and Disable waveforms here illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, WP# must not be toggled until the command is complete and the device is ready (status register bit 5 is “1”).

Figure 56. ERASE Enable

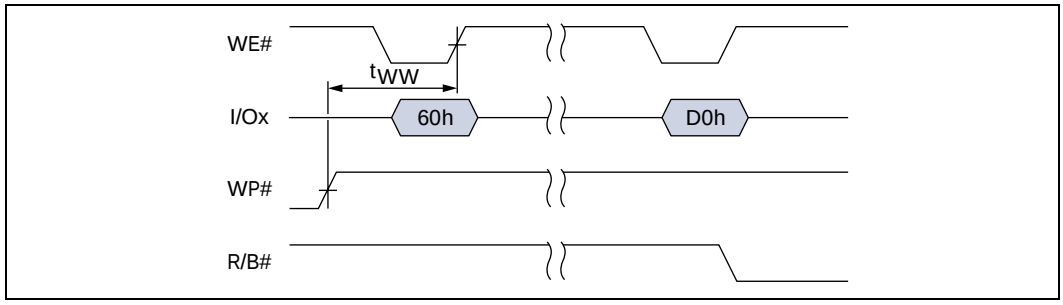


Figure 57. ERASE Disable

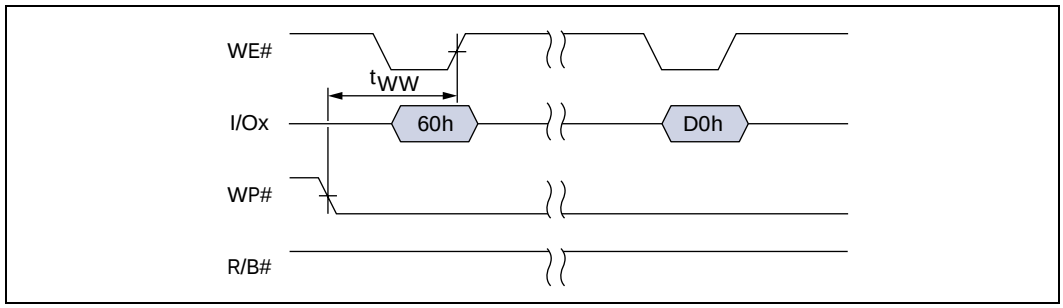


Figure 58. PROGRAM Enable

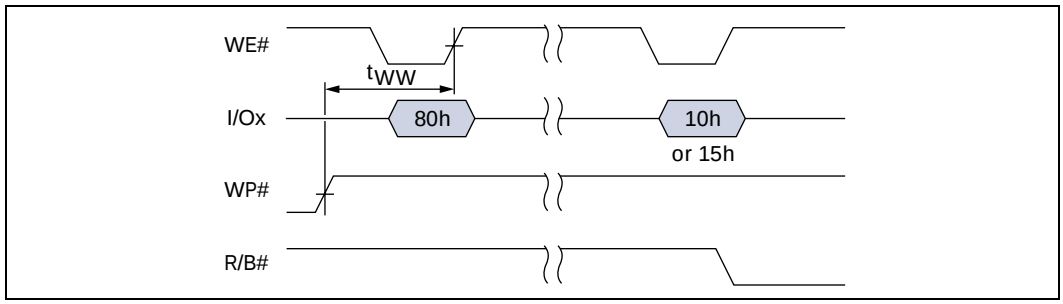


Figure 59. PROGRAM Disable

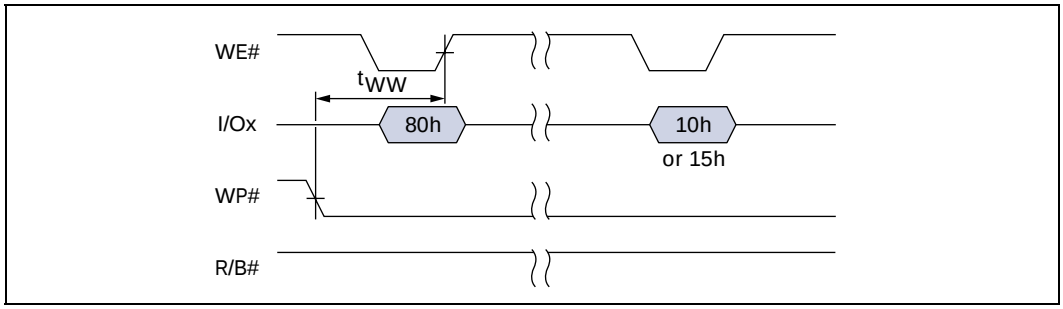


Figure 60. PROGRAM for INTERNAL DATA MOVE Enable

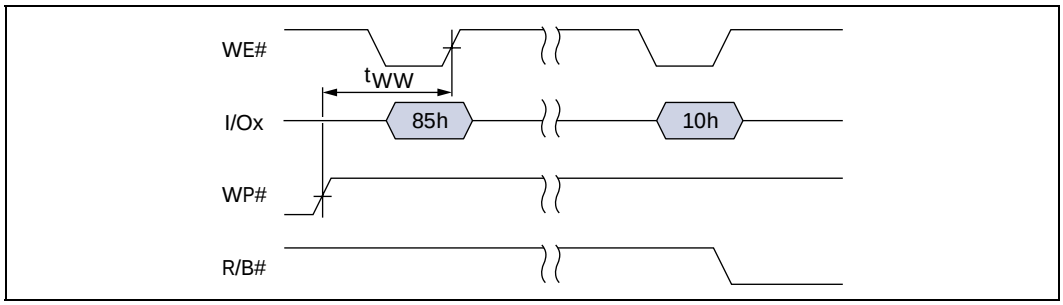


Figure 61. PROGRAM for INTERNAL DATA MOVE Disable

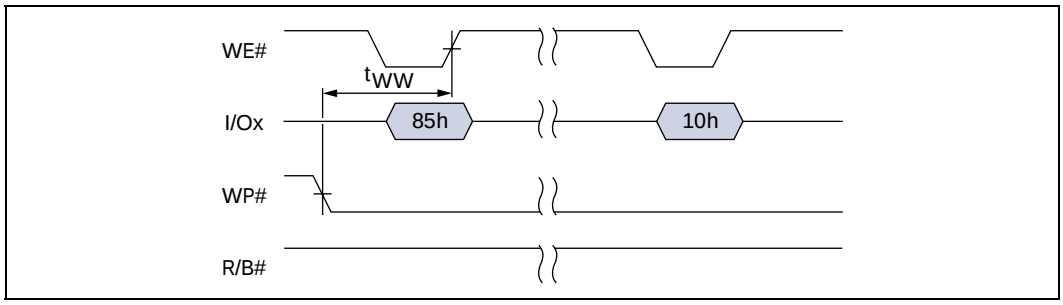


Figure 62. TWO-PLANE ERASE Enable

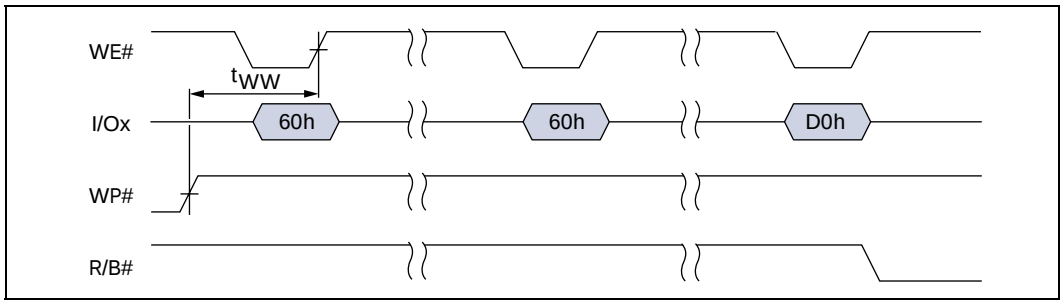


Figure 63. TWO-PLANE ERASE Disable

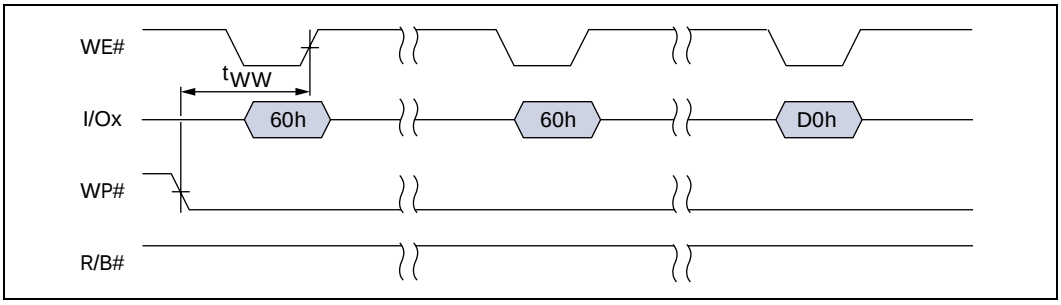


Figure 64. TWO-PLANE PROGRAM Enable

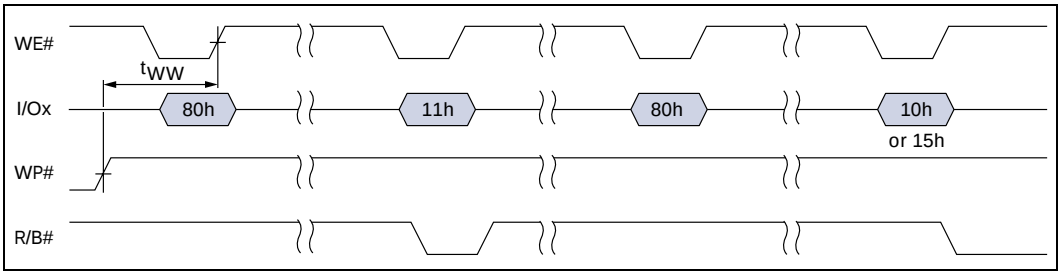


Figure 65. TWO-PLANE PROGRAM Disable

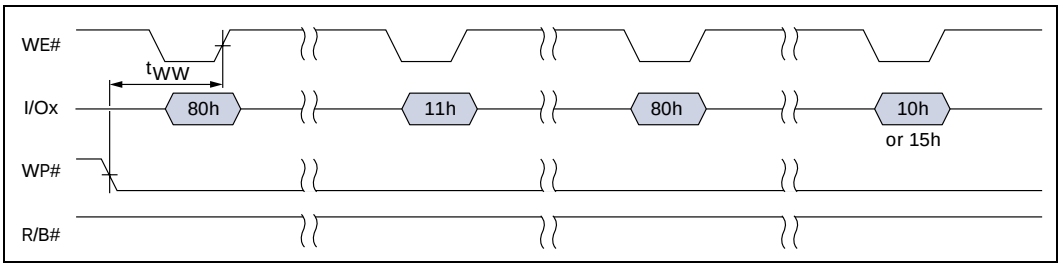


Figure 66. TWO-PLANE PROGRAM for INTERNAL DATA MOVE Enable

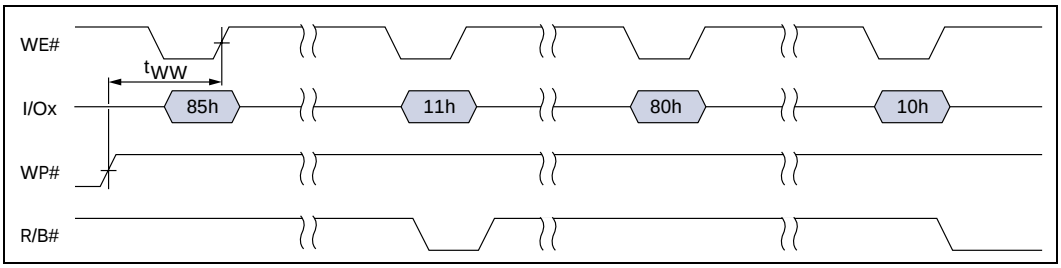
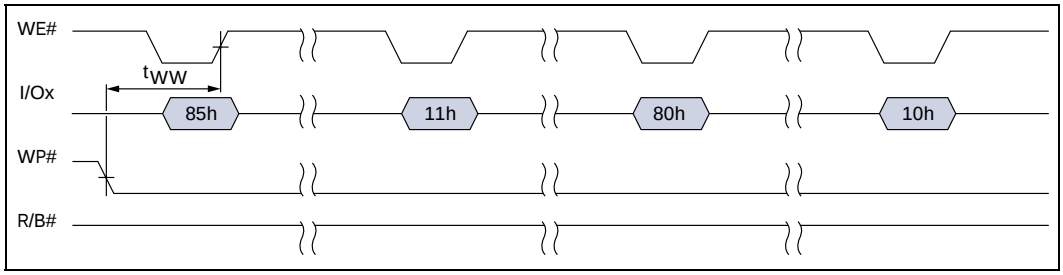


Figure 67. TWO-PLANE PROGRAM for INTERNAL DATA MOVE Disable



8.0 Error Management

This NAND Flash device is specified to have a minimum of 3,936 MLC blocks (Nvb) out of 4.096 total available blocks. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains one or more bad bits. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

The first block (physical block address 00h) for each CE# is guaranteed to be valid for MLC devices, with ECC, when shipped from the factory.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming 00h into the first spare location (column address 4,096) of the first page of each bad block.

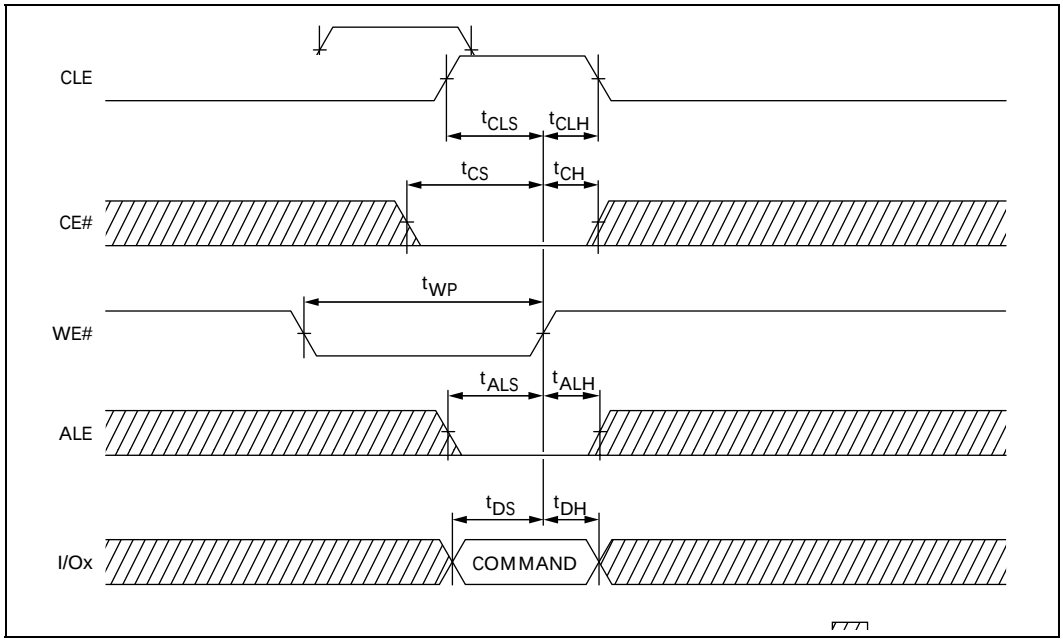
System software should check columns 4096 to 4313 on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad block table can then be created, allowing system software to map around these areas. Factory testing is performed under worst-case conditions. Because blocks marked “bad” may be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Check status after a PROGRAM, ERASE, or INTERNAL DATA MOVE operation.
- Under typical-use conditions, a minimum of 8-bit ECC for MLC devices is required per 539 bytes of data.
- Use bad block management and a wear-leveling algorithm.

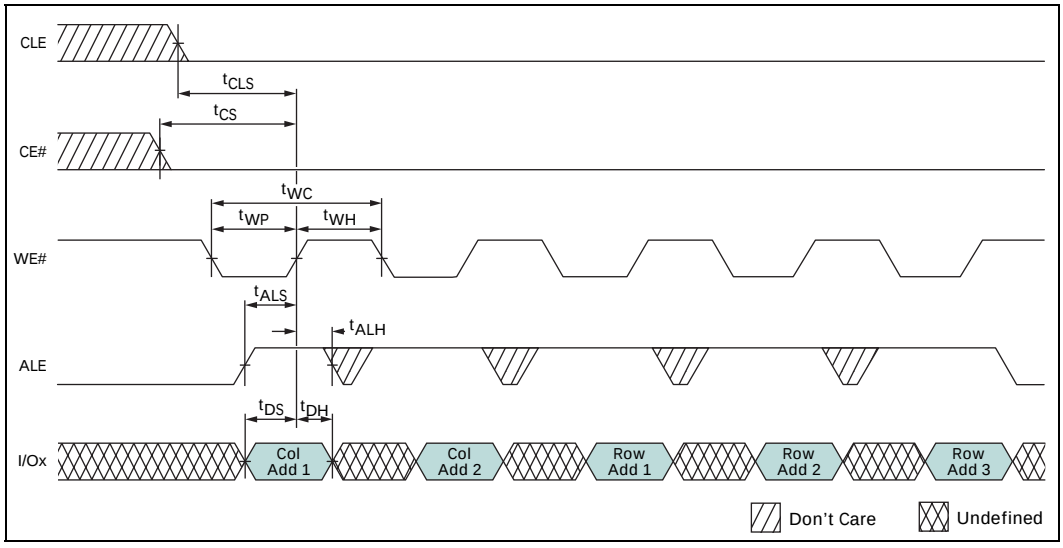
9.0 Timing Diagrams

Figure 68. COMMAND LATCH Cycle



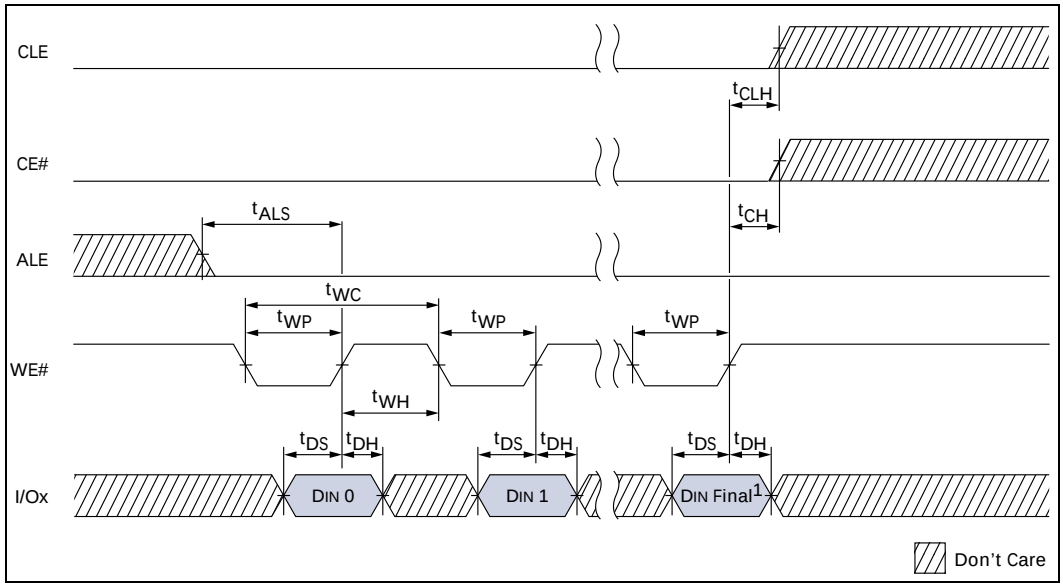
Note: x16: I/O[15:8] must be set to "0.

Figure 69. ADDRESS LATCH Cycle



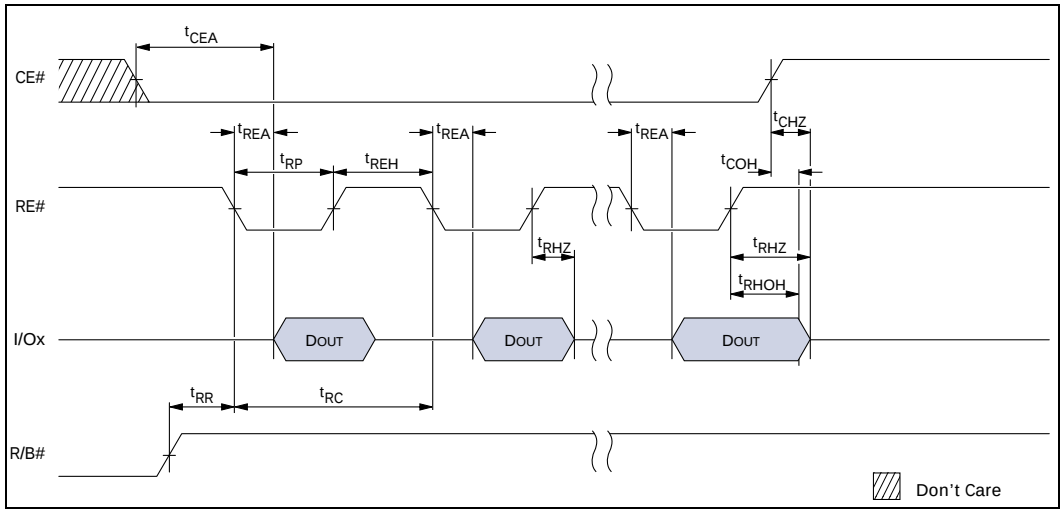
Note: x16: I/O [15:8] must be set to "0."

Figure 70. INPUT DATA LATCH



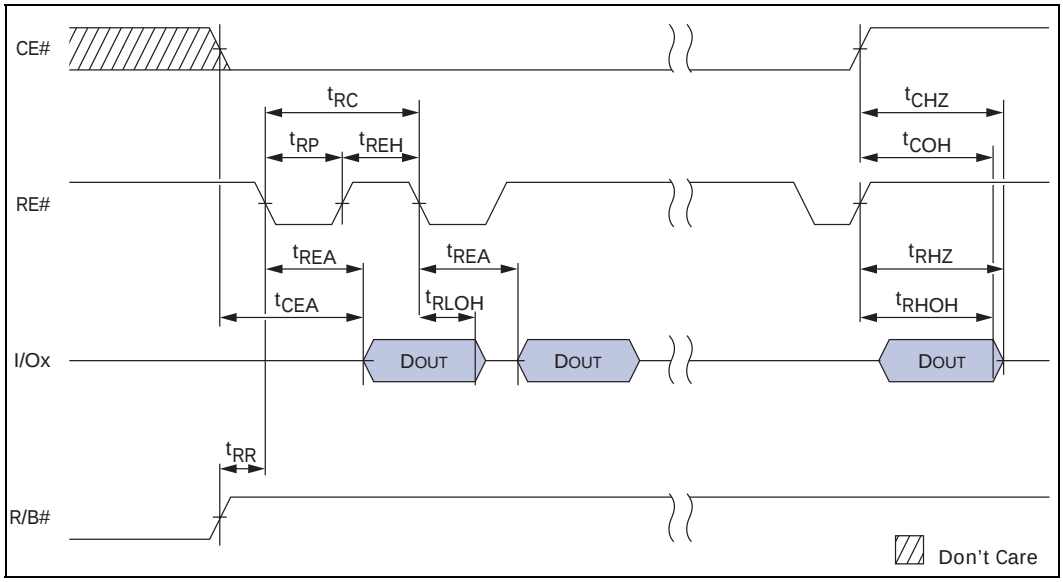
1. DIN Final = 2,111 (x8) or 1,055 (x16).

Figure 71. SERIAL ACCESS Cycle After READ



Note: Use this timing diagram for $^{t}RC \geq 30ns$.

Figure 72. SERIAL ACCESS Cycle After READ (EDO Mode)



Note: Use this timing diagram for $^{t}RC < 30ns$.

Figure 73. READ STATUS Cycle

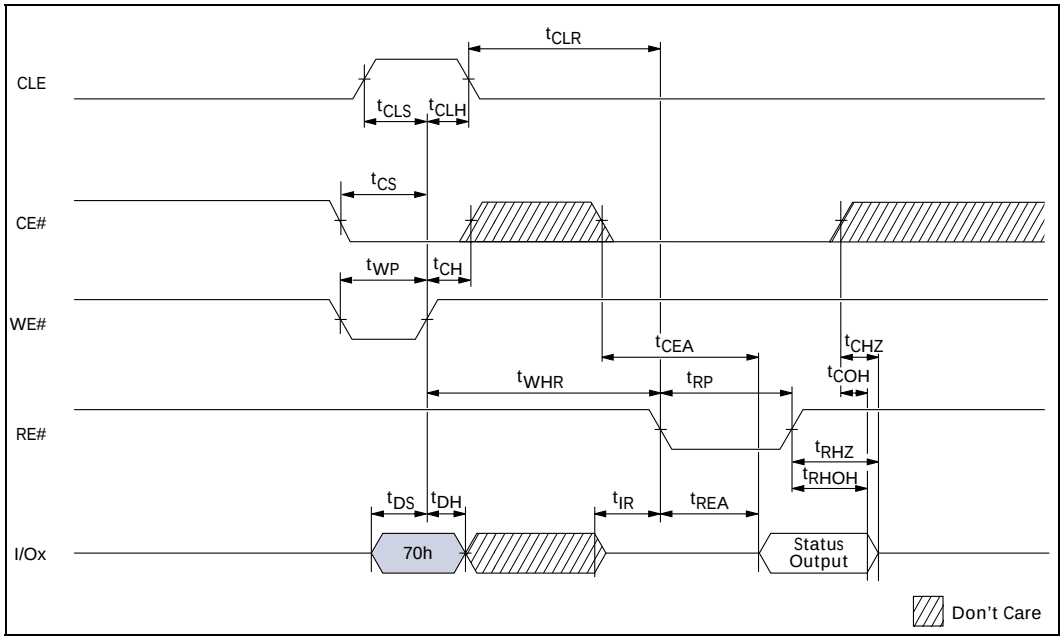


Figure 74. PAGE READ

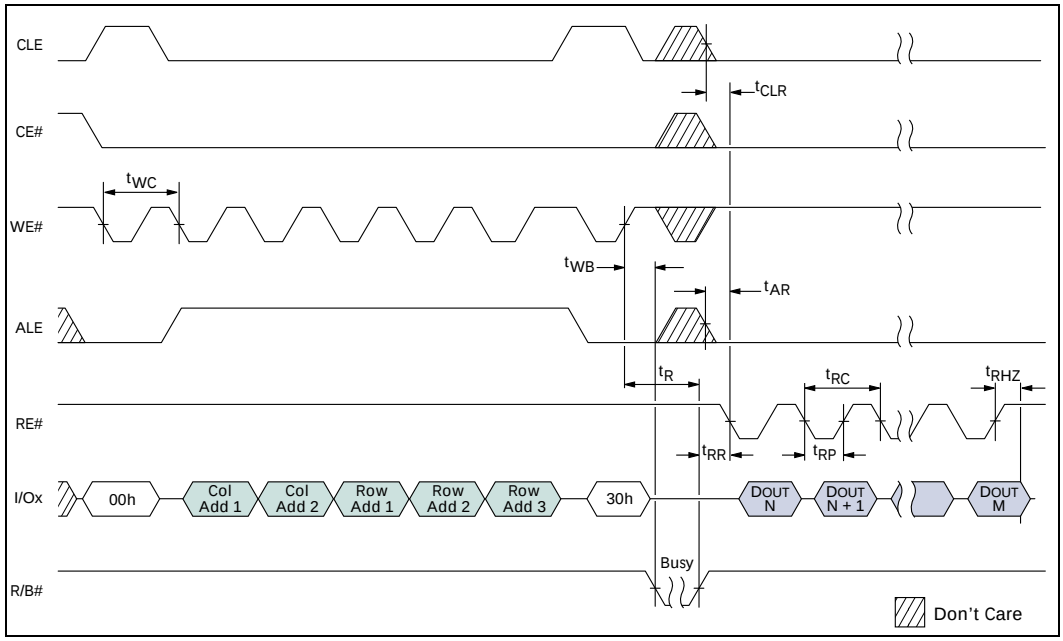


Figure 75. READ Operation with CE# "Don't Care"

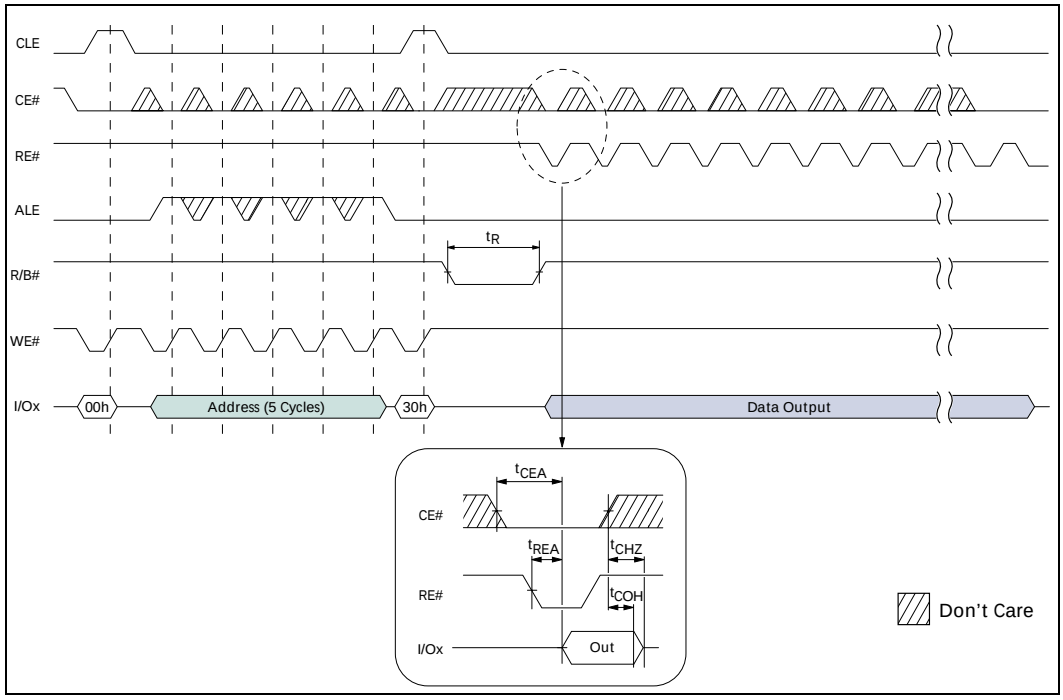


Figure 76. RANDOM DATA READ

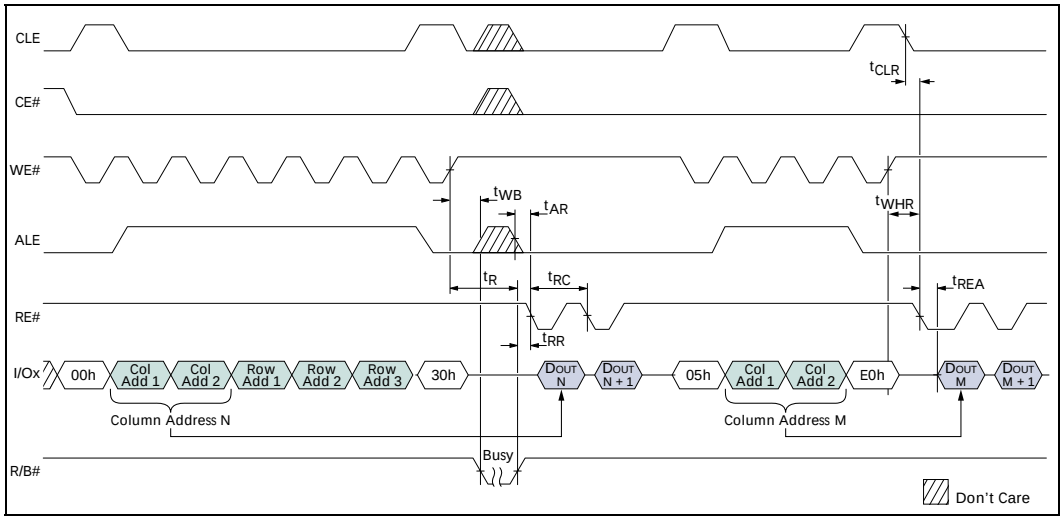


Figure 77. PAGE READ CACHE MODE Timing Diagram, Part 1 of 2

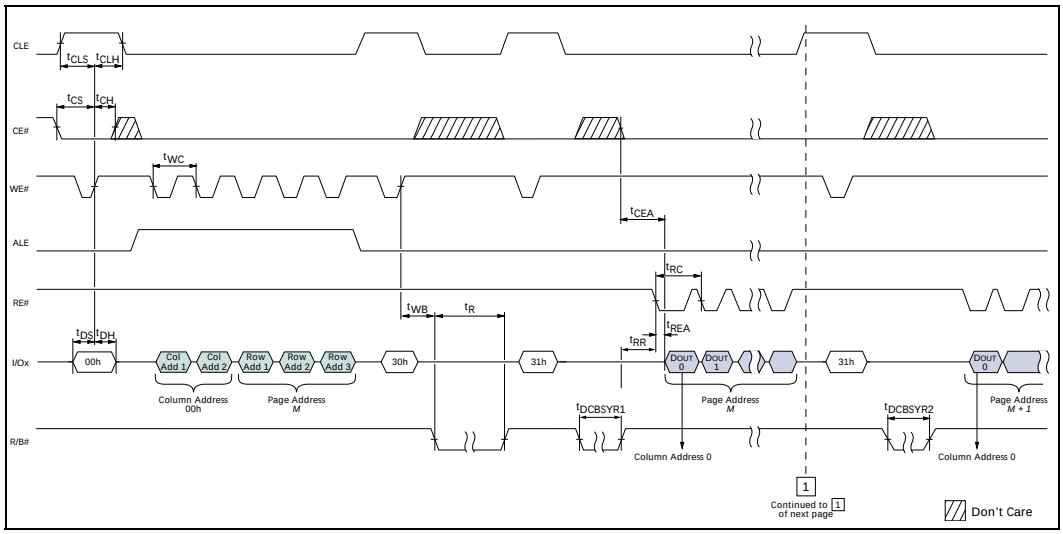


Figure 78. PAGE READ CACHE MODE Timing Diagram, Part 2 of 2

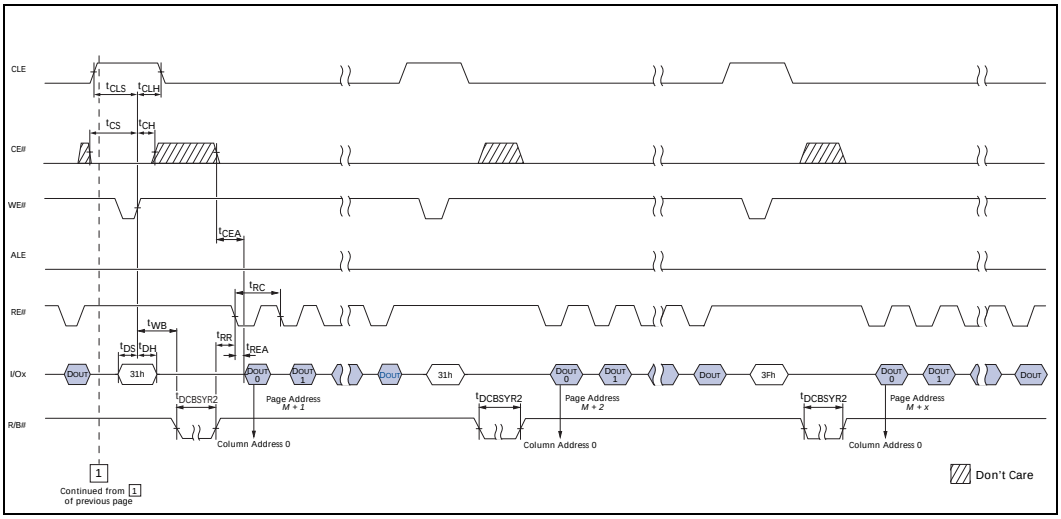


Figure 79. PAGE READ CACHE MODE Timing without R/B#, Part 1 of 2

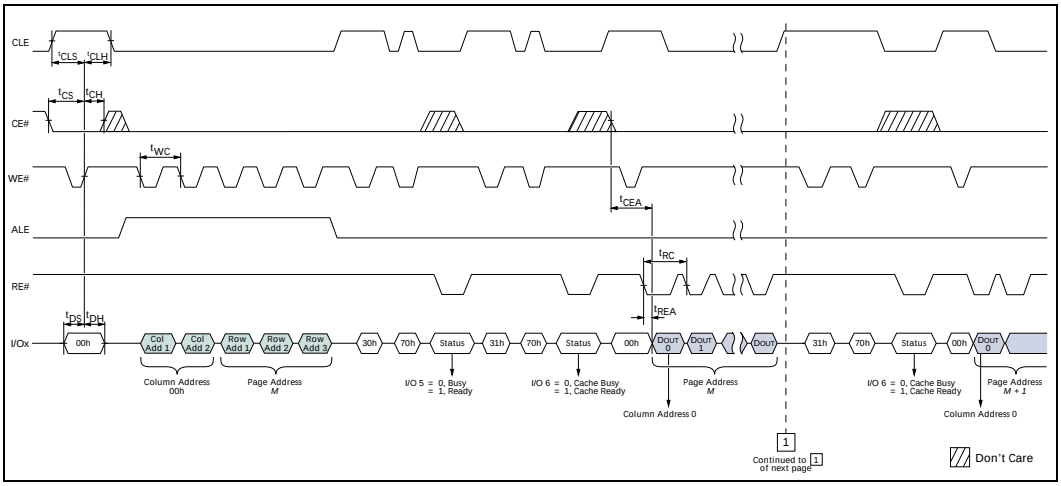


Figure 80. PAGE READ CACHE MODE Timing without R/B#, Part 2 of 2

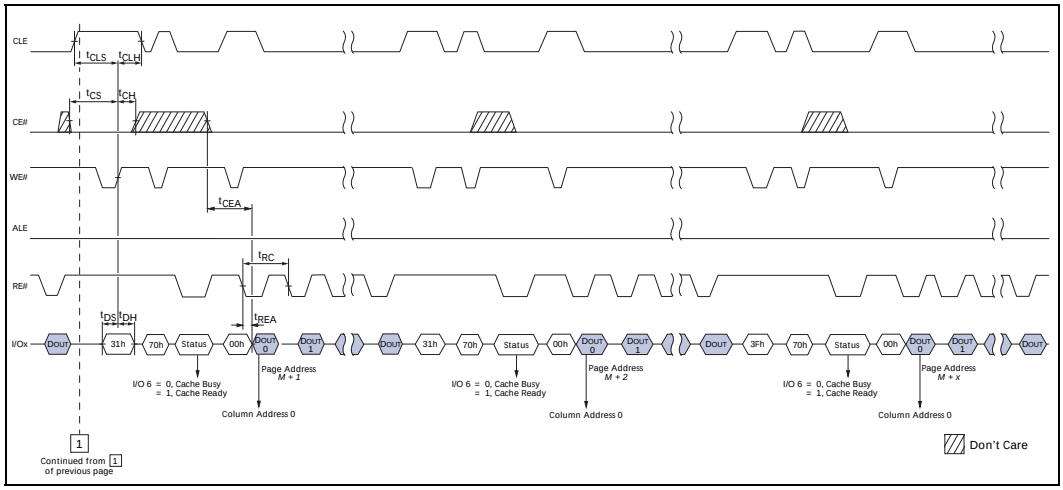
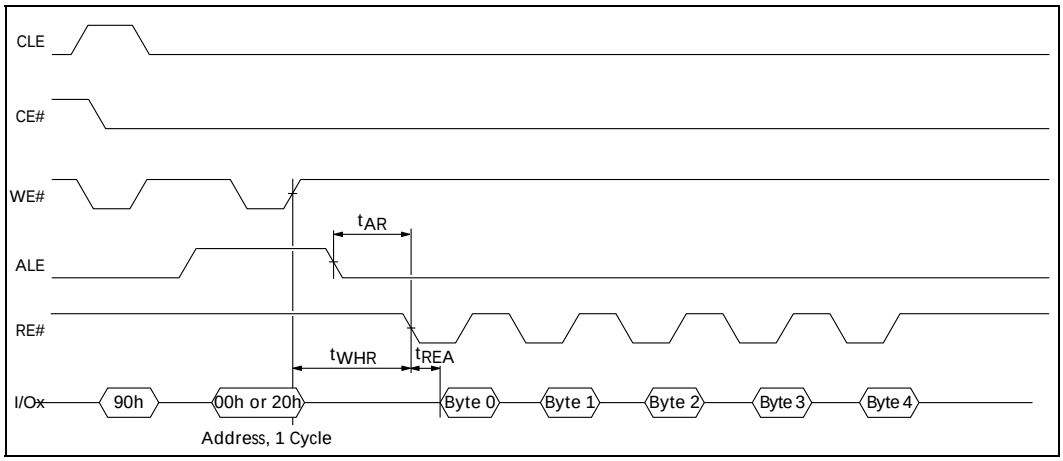


Figure 81. READ ID Operation



Note: See Table 16 on page 30 for actual values.

Figure 82. PROGRAM PAGE Operation

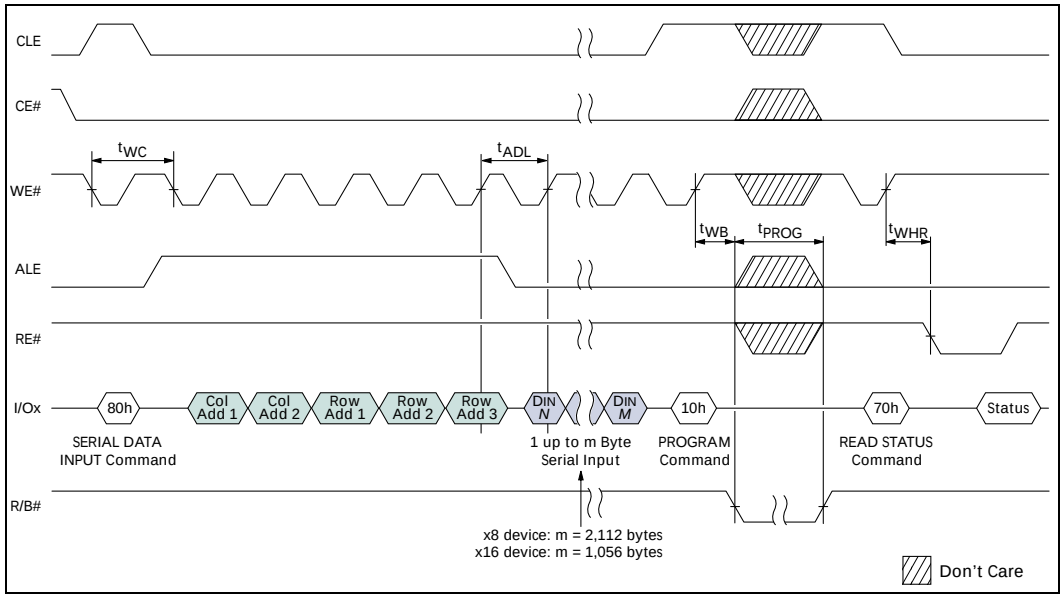


Figure 83. Program Operation with CE# "Don't Care"

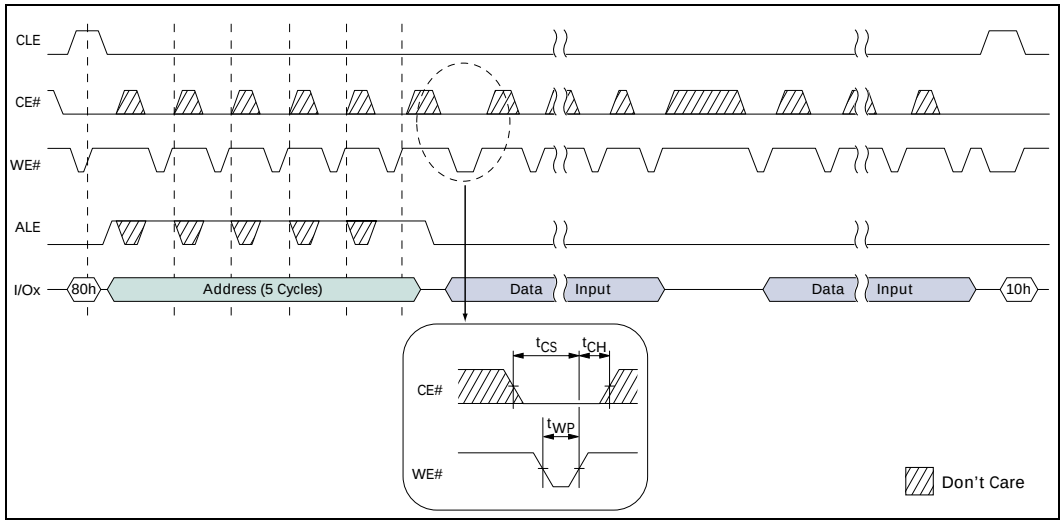


Figure 84. PROGRAM PAGE Operation with RANDOM DATA INPUT

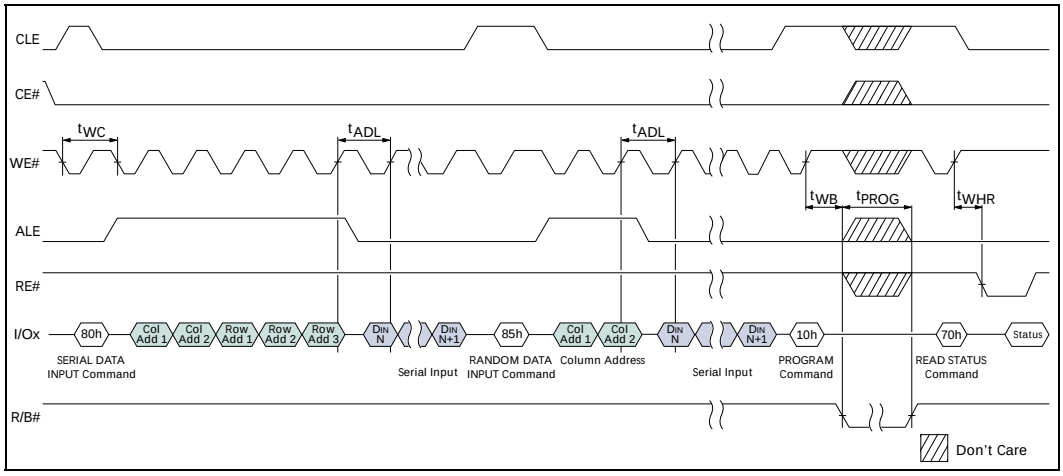


Figure 85. INTERNAL DATA MOVE

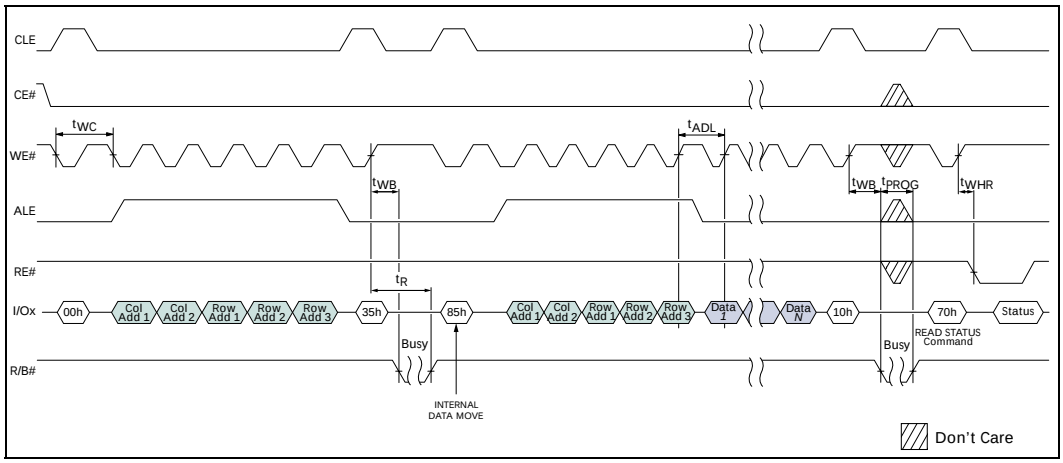
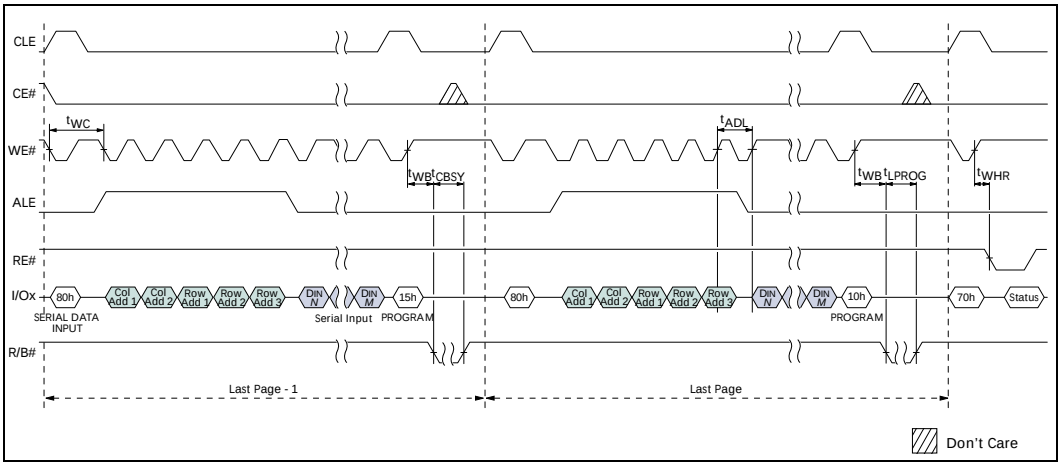


Figure 86. PROGRAM PAGE CACHE MODE



Note: PROGRAM PAGE CACHE MODE operations must not cross block boundaries.

Figure 87. PROGRAM PAGE CACHE MODE Ending on 15h

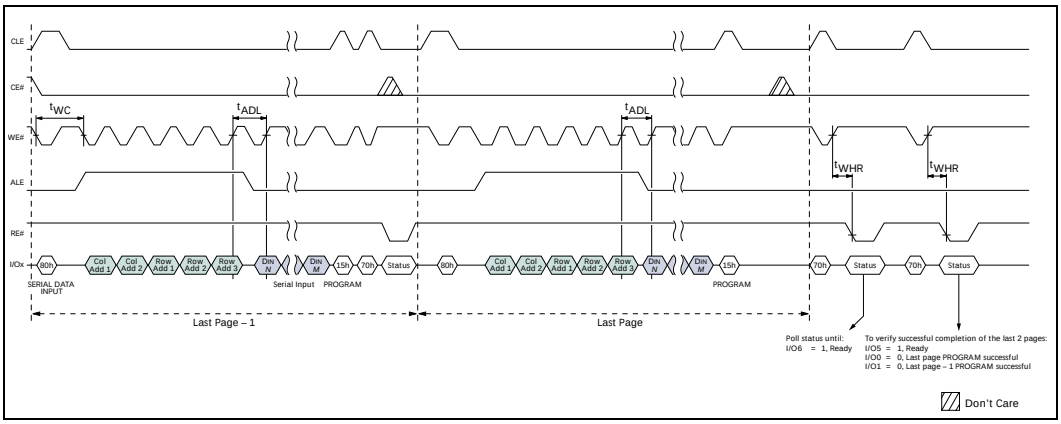


Figure 88. BLOCK ERASE Operation

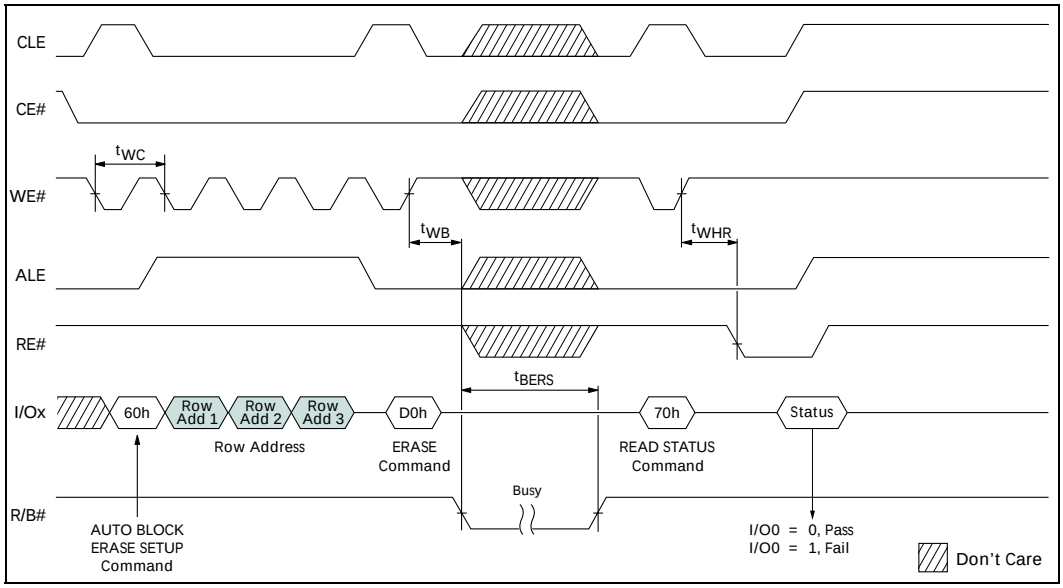
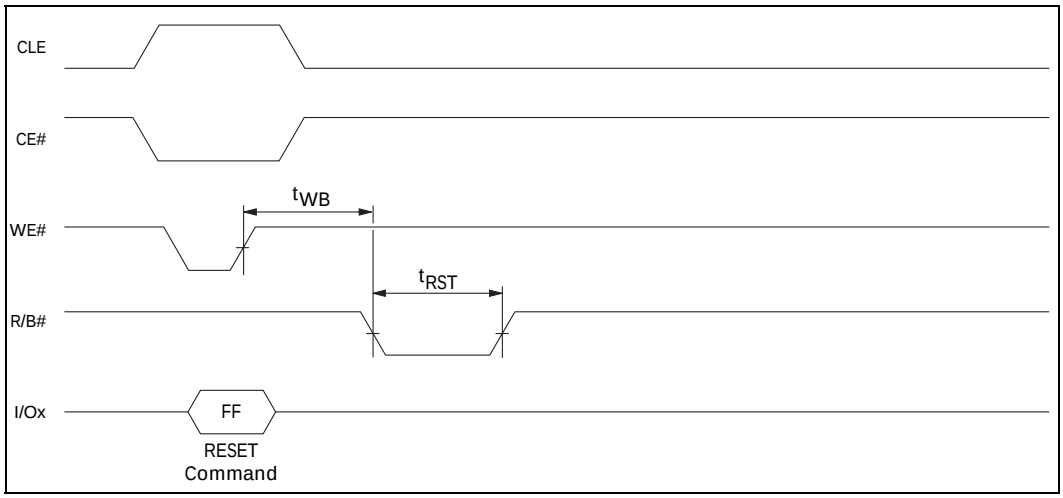


Figure 89. RESET Operation



Appendix A Order Information

Intel® NAND Flash devices are available in several different configurations and densities.

Figure 90. Decoder

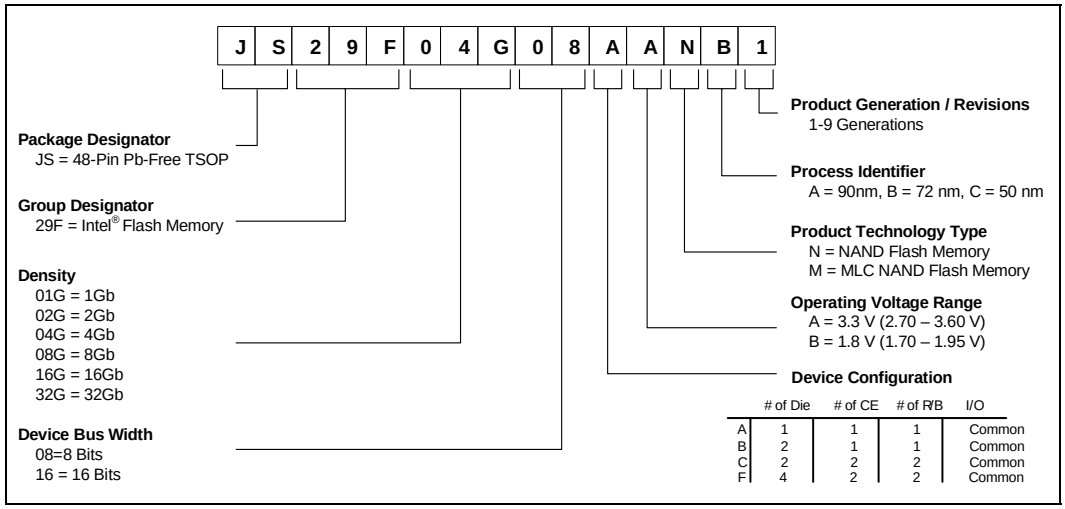


Table 22. Intel® NAND Flash Memory Ordering Information

IM L1 Part Number	Marking Device # (1st Mark Line)	MM #	Device Nomenclature
JS29F16G08AAMC1	29F16G08AAMC1	886222	16Gb, x8, 2 die, 3 V, 1 CE, NAND, 50 nm, 1st Gen Intel Si (1000pc T&R), Pb-Free
		886221	16Gb, x8, 2 die, 3 V, 2 CE, NAND, 50 nm, 1st Gen Intel Si (1000pc Tray Pack), Pb-Free
JS29F32G08BAMC1	29F32G08CAMC1	889840	32Gb, x8, 2 die, 3 V, 2 CE, NAND, 50 nm, 1st Gen Intel Si (1000pc Tray Pack), Pb-Free
		889798	32Gb, x8, 2 die, 3 V, 2 CE, NAND, 50 nm, 1st Gen Intel Si (1000pc T&R), Pb-Free
JS29F64G08FAMC1	29F64G08FAMC1	889841	64Gb, x8, 4 die, 3 V, 2 CE, NAND, 50 nm, 1st Gen Intel Si (1000pc Tray), Pb-Free
		889799	64Gb, x8, 4 die, 3 V, 2 CE, NAND, 50 nm, 1st Gen Intel Si (1000pc T&R), Pb-Free