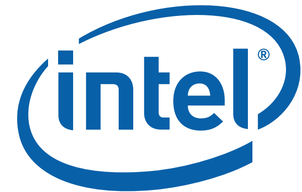


Intel® MD332B NAND Flash Memory

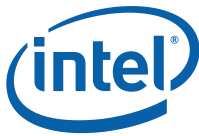
JS29F32G08AAMDB, JS29F64G08CAMDB, JS29F16B08JAMDB

Preliminary Datasheet

Product Features

- Open NAND Flash Interface (ONFI) 2.0 Compliant
- Multilevel cell (MLC) technology
- Organization:
  - — Page size: 4,320 bytes (4,096 + 224 bytes)
  - — Block size: 256 pages (1,024K + 56K bytes)
  - — Plane size: 2,048 blocks
- Read performance
  - — Random read: 50 µs
  - — Sequential read: 20 ns
- Write performance
  - — Page program: 900 µs (TYP)
  - — Block erase: 2 ms (TYP)
- Endurance:
  - — 5,000 PROGRAM/ERASE cycles
  - — Data Retention: JEDEC compliant
- Operating Temperature:
  - — Commercial: 0°C to +70°C
  - — Extended: -40°C to +85°C
- Core Voltage (VCC): 2.7 V - 3.6 V
- First block (block address 00h) guaranteed to be valid when shipped from factory
- Ready/busy# (R/B#) signal provides a hardware method of detecting PROGRAM or ERASE cycle completion
- WP# signal: Entire device hardware write protect
- Advanced command set:
  - — PAGE CACHE PROGRAM
  - — READ CACHE (RANDOM, SEQUENTIAL, END)
  - — Multi-plane commands
- Operation status byte provides a software method of detecting:
  - — Operation completion
  - — Pass/fail condition
  - — Write-protect status

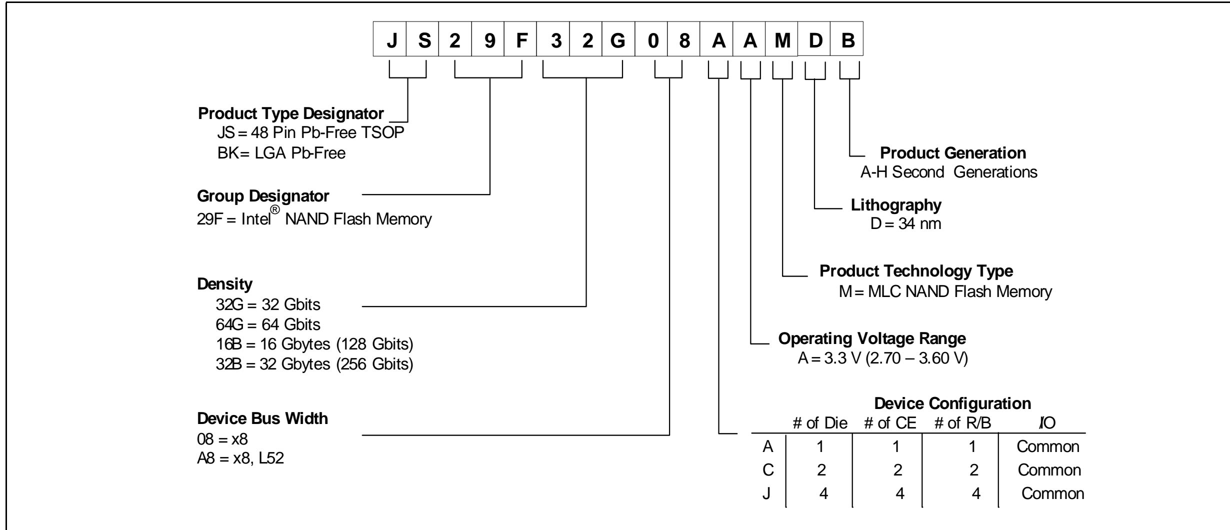
Density	Package	# of Die		# of CE# and R/B#	Bus I/O Configuration	Device ID
32 Gb	TSOP	SDP	1	1	single x8	89h, 68h, 04h, 46h, A9h
64 Gb	TSOP	DDP	2	2	single x8	89h, 68h, 04h, 46h, A9h
128 Gb	TSOP	QDP	4	4	single x8	89h, 68h, 04h, 46h, A9h



Ordering Information

Intel® NAND Flash devices are available in several different configurations and densities.

Decoder



Intel® NAND Flash Memory Ordering Information

Device Name	MM #	Device Nomenclature
JS29F32G08AAMDB	903681	32 Gb x8 SDP, 1 CE, 1 R/B, 3.3 V TSOP (T & R 1,000 pc.)
JS29F64G08CAMDB	903682	64 Gb x8 DDP, 2 CE, 2 R/B, 3.3 V TSOP (T & R 1,000 pc.)
JS29F16B08JAMDB	903683	128 Gb x8 QDP, 4 CE, 4 R/B, 3.3 V TSOP (T & R 1,000 pc.)

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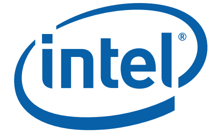

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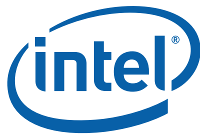

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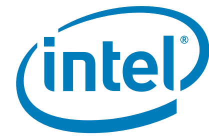


1.0 Overview

NAND Flash technology provides a cost-effective solution for applications requiring high-density solid-state storage for:

- 32 Gb NAND Flash memory device
- 64 Gb two-die stack that operates as two independent 32 Gb devices
- 128 Gb four-die stacks that operates as four independent 32 Gb devices

Intel® NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

1.1 Architecture

Intel NAND Flash devices use a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Two additional pins control hardware write protection (WP#) and monitor device status (R/B#).

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

The 32 Gb device contain two planes in a single die. Each plane consists of 2,048 blocks. Each block is subdivided into 256 programmable pages. Each page consists of 4,320 bytes. The pages are further divided into a 4,096-byte data storage region with a separate 224-byte area. The 224-byte area is typically used for error management functions.

The 64 Gb and 128 Gb devices are created by stacking 32 Gb memory.

The contents of each 4,320-byte page can be programmed in 900 µs, and an entire block can be erased in 2 ms. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/PROGRAM endurance is specified at 5,000 cycles when using appropriate error correcting code (ECC) and error management.

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

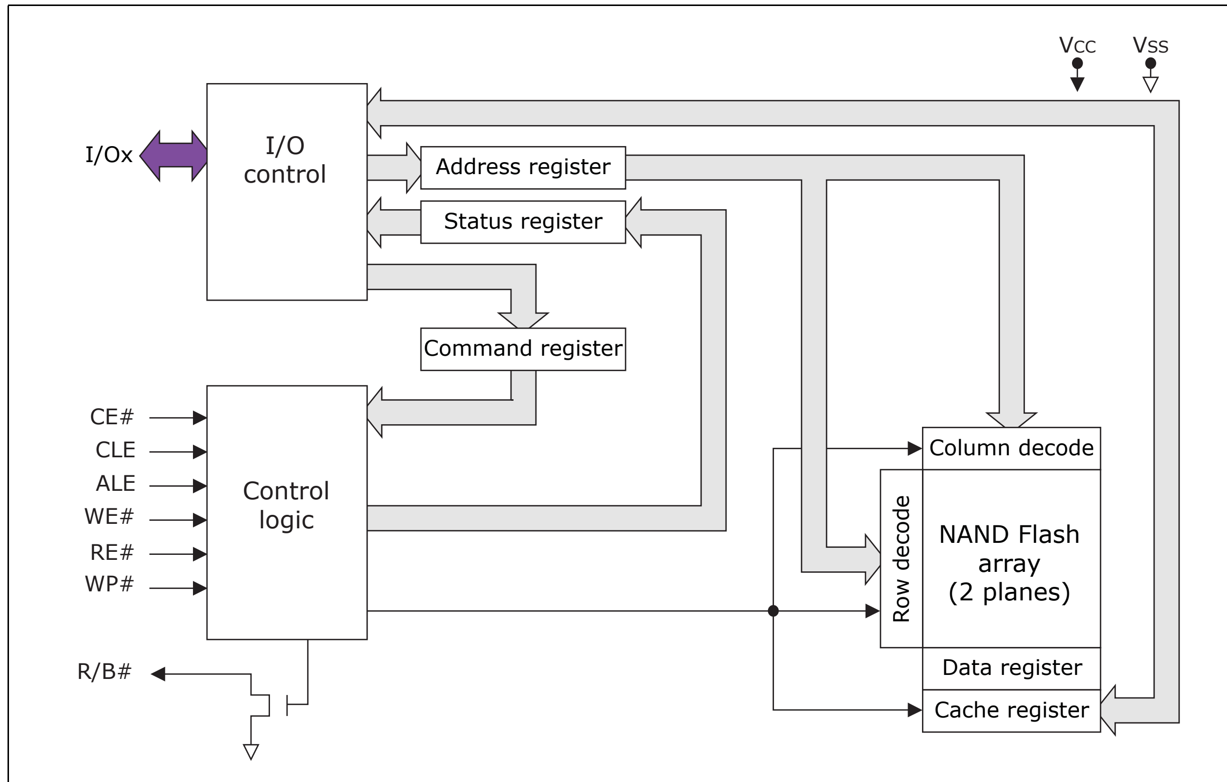
The data are transferred to or from the NAND Flash memory array, byte by byte (x8), through a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data, whereas the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations and is erased in block-based operations. During normal page operations, the data and cache registers are tied together and act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

These devices also have a status register that reports the status of device operation.

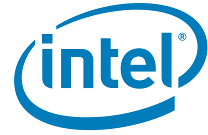
1.2 Block Diagram

Figure 1. NAND Flash Memory Functional Block Diagram



1.3 Addressing

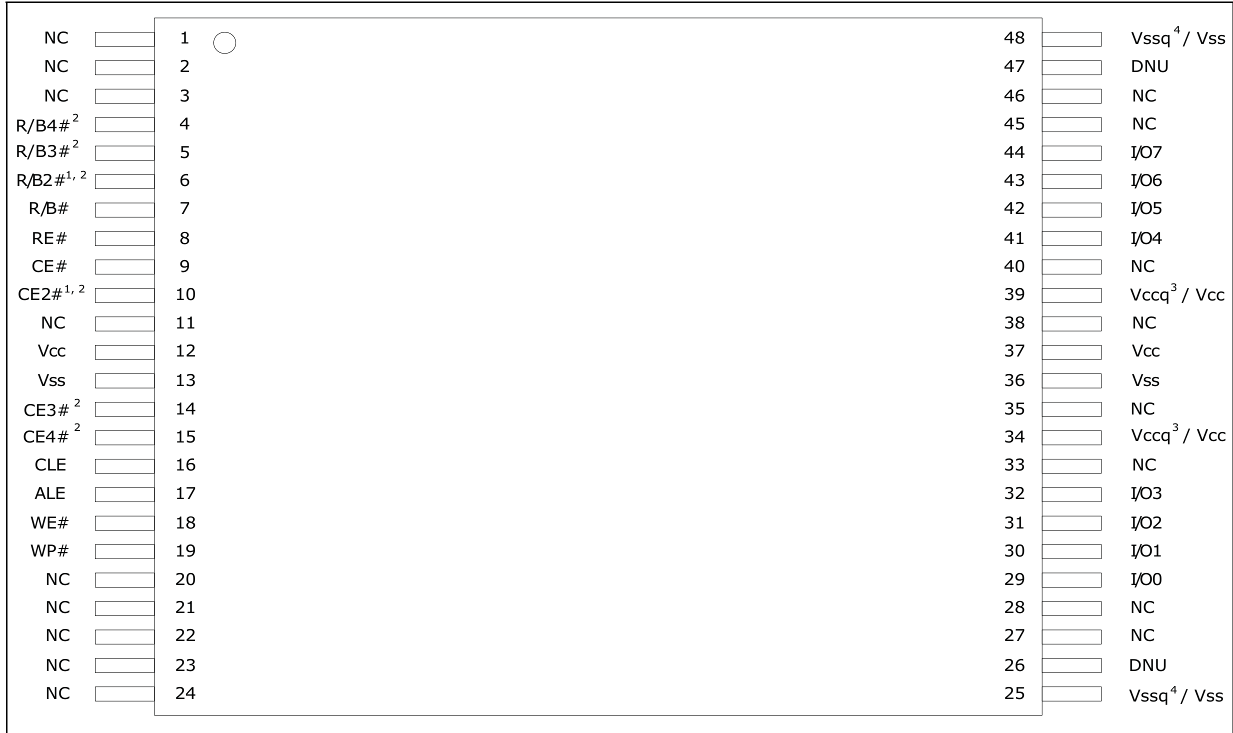
NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a five-cycle sequence as shown in Table 2, “Array Addressing: x8” on page 12. See Figure 8, “Memory Map (x8)” on page 13 for additional memory mapping and addressing details.



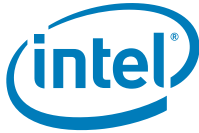
2.0 Packaging Information

2.1 Pin Assignments

Figure 2. TSOP 48-Pin Assignment (Top View)



Notes:
1. CE2# and R/B2# are used in Dual Die Package with two CE# and two R/B#. These pins are NC for Single Die Package configurations.
2. CE2#, CE3#, CE4#, R/B2#, R/B3# and R/B4# are also used in Quad Die Packages. These pins are NC for Single Die Package configurations. CE3#, CE4#, R/B3# and R/B4# are NC for Dual Die Package configurations.
3. VCCQ shall be driven by VCC.
4. VssQ shall be driven by Vss.



2.2 Signal Descriptions

Table 1. TSOP Signal Descriptions

Symbol	Type	Pin Function
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#, CE2#, CE3#, CE4#	Input	Chip enable: Gates transfers between the host system and the NAND Flash device. Once the device starts a PROGRAM or ERASE operation, CE# can be de-asserted. For the 64 Gb with two CE# configuration, CE# controls the first 32 Gb of memory; CE2# controls the second 32 Gb. For the 128 Gb with four CE# configuration, each CE# controls the 32 Gb of memory.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#	Input	Read enable: Gates transfers from the NAND Flash device to the host system.
WE#	Input	Write enable: Gates transfers from the host system to the NAND Flash device.
WP#	Input	Write protect: Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
I/O[7:0]	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#, R/B2#, R/B3#, R/B4#	Output	Ready/Busy: An *open-drain,* active-LOW output, that uses an external pull-up resistor. The pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during a READ operation to indicate when data is being transferred from the array into the serial data register. Once these operations have completed, R/B# returns to the high-impedance state. For the 64 Gb with two CE# and two R/B# configuration, R/B# is for the 32 Gb of the memory enabled by CE#; R/B2# is for the 32 Gb of memory enabled by CE2#. For the 128 Gb with four CE# and four R/B# configuration, each R/B# is for the 32 Gb of memory enabled by corresponding CE#.
V_{CC}	Supply	Power supply pin.
V_{CCQ}	Supply	Power supply for I/Os.
V_{SS}	Supply	Ground connection.
V_{SSQ}	Supply	Ground connection for I/Os.
NC	–	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	–	Do not use: DNUs must be left disconnected.

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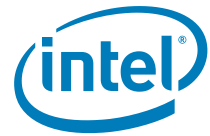
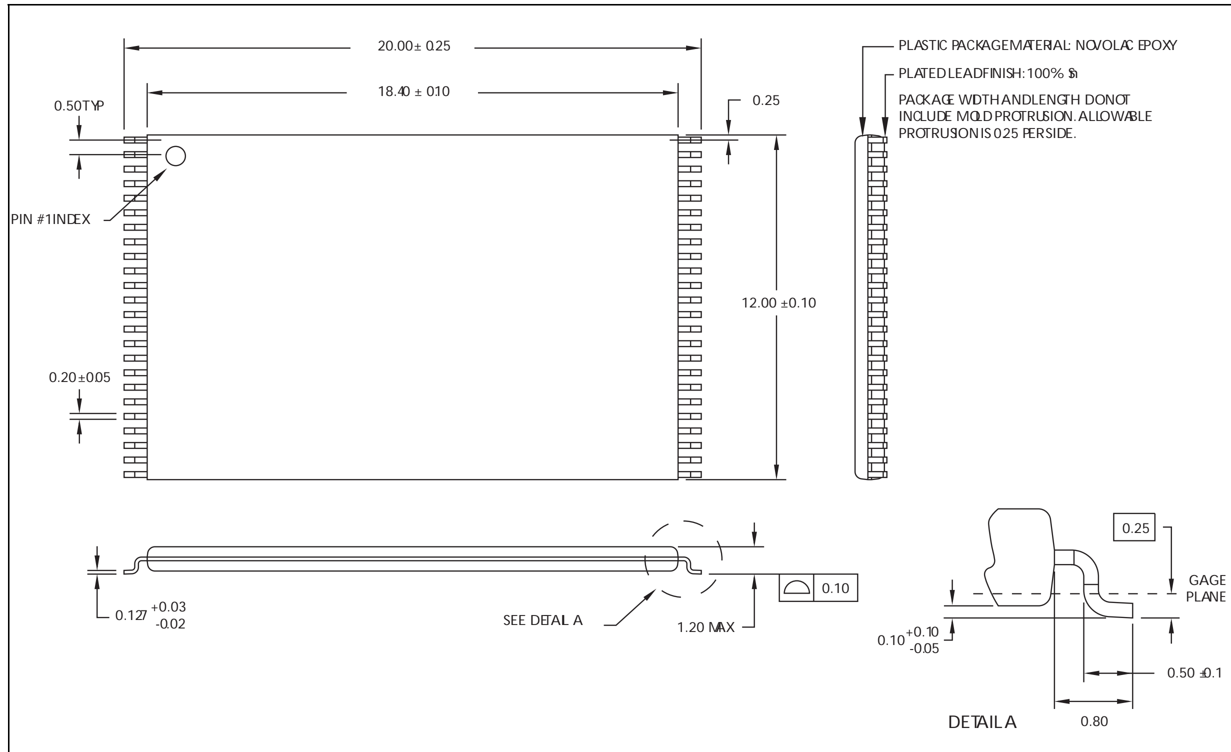
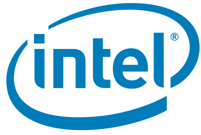


2.3 Mechanical Drawings

Figure 3. TSOP Type 1 Package Dimensions



Note: All dimensions in millimeters; MIN/MAX, or typical, as noted.



3.0 Configurations

Figure 4. SDP TSOP Configuration

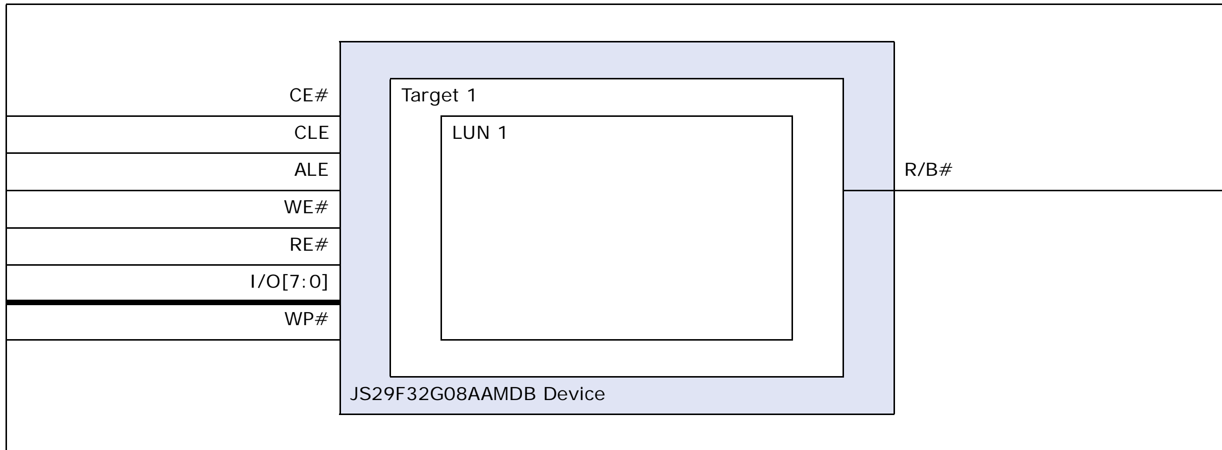
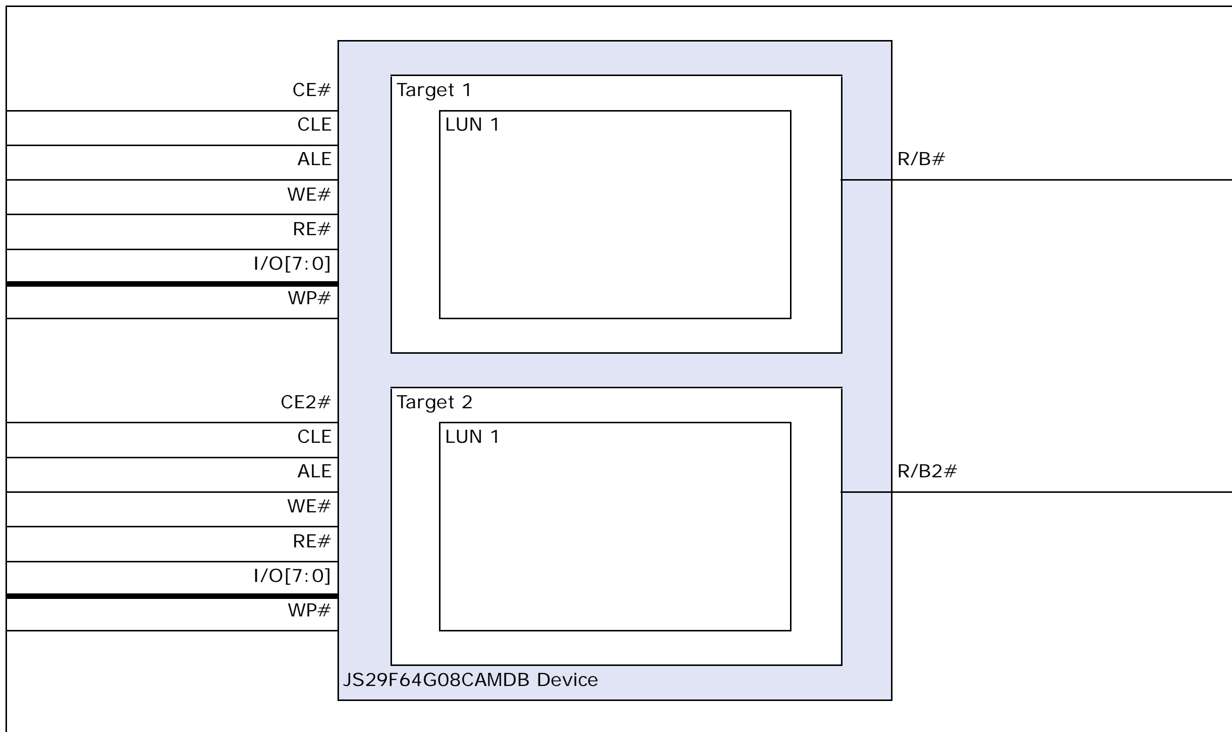


Figure 5. DDP TSOP Configuration



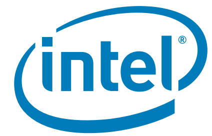


Figure 6. QDP TSOP Configuration

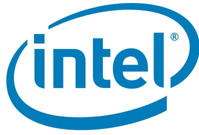
CE#
CLE
ALE
WE#
RE#
I/O[7:0]
WP#
Target 1
LUN 1
R/B#

CE2#
CLE
ALE
WE#
RE#
I/O[7:0]
WP#
Target 2
LUN 1
R/B2#

CE3#
CLE
ALE
WE#
RE#
I/O[7:0]
WP#
Target 3
LUN 1
R/B3#

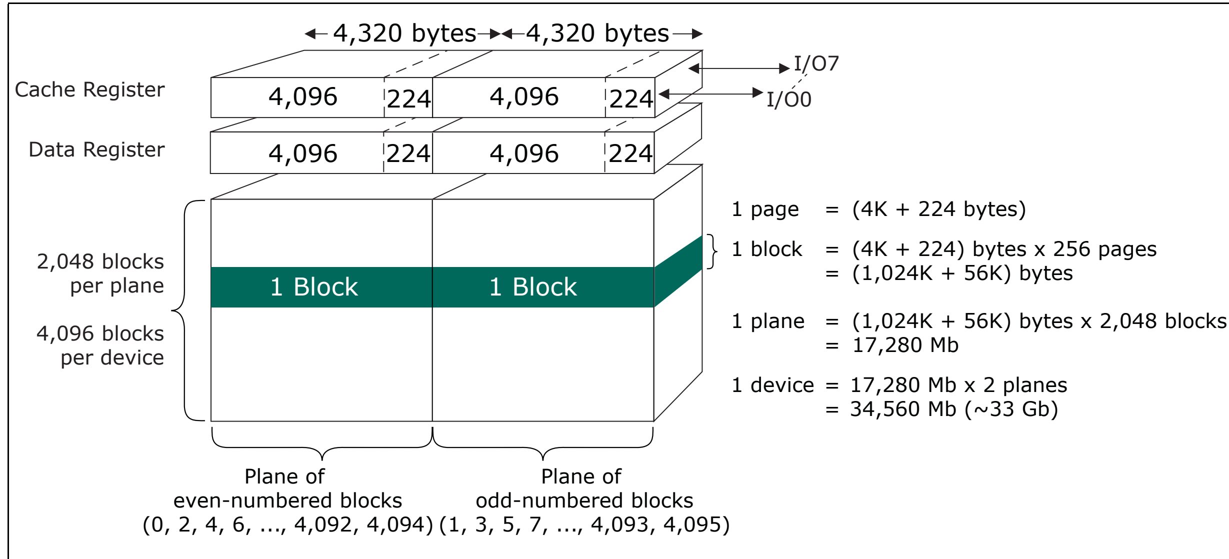
CE4#
CLE
ALE
WE#
RE#
I/O[7:0]
WP#
Target 4
LUN 1
R/B4#

JS29F16B08JAMDB Device



4.0 Array Organization

Figure 7. Array Organization for 32 Gb x8

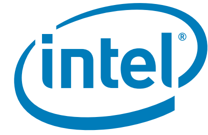


Notes:
1. For the 64 Gb with 2 CE#, the 32 Gb array organization shown here applies to each die enable by CE#.
2. For the 128 Gb with 4 CE#, the 32 Gb array organization shown here applies to each die enable by CE#.

Table 2. Array Addressing: x8

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8[2]
Fifth	LOW	LOW	LOW	LOW	BA19	BA18	BA17	BA16

Notes:
1. Block address concatenated with page address = actual page address.
   CAx = column address;
   PAx = page address;
   BAx = block address.
2. Plane select bit (BA8)
   0 = Plane of even-numbered blocks.
   1 = Plane of odd-numbered blocks.



5.0 Memory Map

Figure 8. Memory Map (x8)

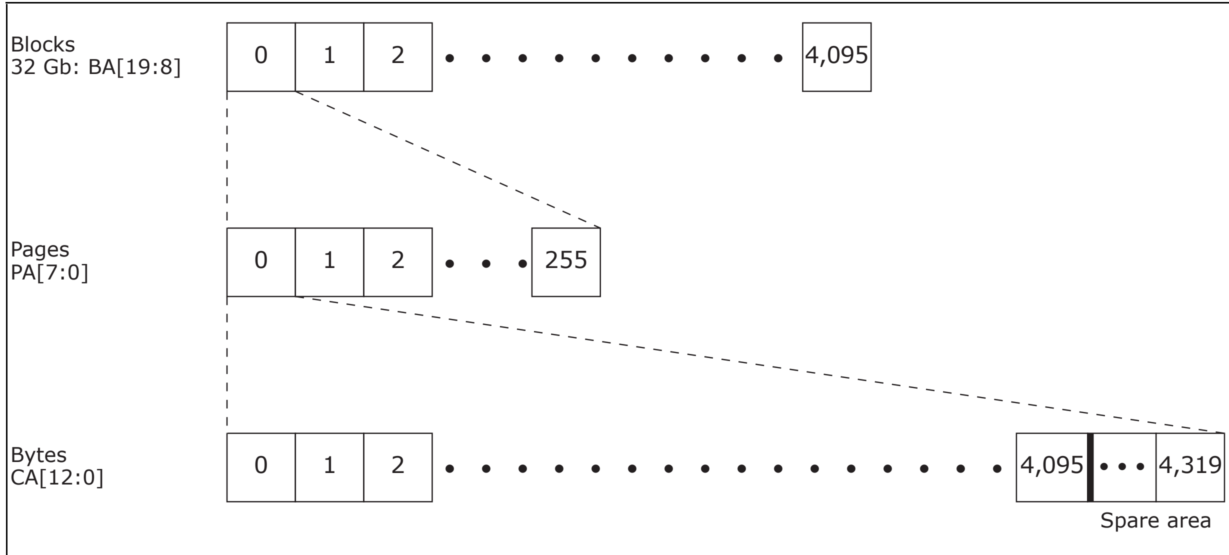
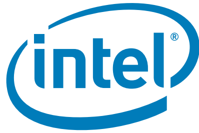


Table 3. Operational Example (x8)

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x00000010DF	0x00000010E0–0x0000001FFF
0	1	0x0000010000	0x00000110DF	0x00000110E0–0x0000011FFF
0	2	0x0000020000	0x00000210DF	0x00000210E0–0x0000021FFF
...	...	...	...	
4,095	254	0x0FFFFE0000	0x0FFFFE10DF	0x0FFFFE10E0–0x0FFFFE1FFF
4,095	255	0x0FFFFF0000	0x0FFFFF10DF	0x0FFFFF10E0–0x0FFFFF1FFF

Note: As shown in Table 2, "Array Addressing: x8" on page 12, the three most significant bits in the high nibble of ADDRESS cycle 2 are not assigned; however, these 3 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.

The 13-bit column address is capable of addressing from 0 to 8,191 bytes on a x8 device; however, only bytes 0 through 4,313 are valid. Bytes 4,314 through 8,191 of each page are "out of bounds," do not exist in the device, and cannot be addressed.



6.0 Bus Operation

The bus on these Intel NAND Flash Memory devices is multiplexed. Data I/O, addresses, and commands all share the same pins, I/O[7:0].

The command sequence normally consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and one or more DATA cycles—either READ or WRITE.

6.1 Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control Flash device READ and WRITE operations. On the 64 Gb, CE# and CE2# each control independent 32 Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#. On the 128 Gb, CE#, CE2#, CE3# and CE4# each control independent 32 Gb arrays. CE2#, CE3# and CE4# function the same as CE# for its own array; all operations described for CE# also apply to CE2#, CE3# and CE4#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the Flash memory will accept command, address, and data information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 88 on page 93 and Figure 96 on page 97 for examples of CE# "Don't Care" operations.

The CE# "Don't Care" operation allows the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus. One device can be programmed while another is being read.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

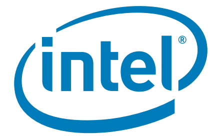
6.2 Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- the device is not busy.

As exceptions, the device accepts the READ STATUS (70h), READ STATUS ENHANCED (78h), and RESET (FFh) commands when busy. Commands are transferred to the command register on the rising edge of WE# (see Figure 80, "COMMAND LATCH Cycle" on page 89).

Commands are input on I/O[7:0] only.



6.3 Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are low, and
- ALE is high.

Addresses are input on I/O[7:0] only. Bits not part of the address space must be LOW (see Figure 81 on page 89).

The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements. See Tables 5–6, starting on page 19.

6.4 Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy.

Data is input on I/O[7:0] for x8 devices. See Figure 82, "INPUT DATA LATCH" on page 90 for additional data input details.

6.5 READs

After a READ command is issued, data is transferred from the memory array to the data register from the rising edge of WE#. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. R/B# returns to HIGH at this time. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 87, "READ" on page 92 for detailed timing information.

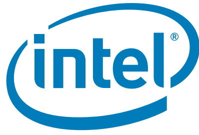
The READ STATUS (70h) command, READ STATUS ENHANCED (78h) command, or the R/B# signal can be used to determine when the device is ready.

If a controller is using a timing of 30 ns or longer for ^{t}RC, use Figure 83 on page 90 for proper timing. If ^{t}RC is less than 30 ns, use Figure 84 on page 91 for extended data output (EDO) timing.

6.6 Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically R/B# would be connected to an interrupt pin on the system controller (see Figure 11 on page 17**).**

On the 64 Gb device, R/B# provides a status indication for the 32 Gb section enabled by CE#, and R/B2# does the same for the 32 Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 32 Gb section.



On the 128 Gb device, R/B1#, R/B2#, R/B3#, and R/B4# can be tied together, or they can be used separately to provide independent indications for each 32 Gb section, respectively.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC; see the figure below).

Figure 9. Time Constants

$$TC = R \times C$$

Where R = Rp and C = total capacitive load

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figure 12 on page 17, and Figure 13 on page 18, which depict approximate Rp values using a circuit load of 100 pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

Figure 10. Minimum Rp

$$Rp\ (MIN,\ 3.3V\ part) = \frac{V_{CC}\ (MAX) - V_{OL}\ (MAX)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where ΣI_L is the sum of the input currents of all devices tied to the R/B# pin.

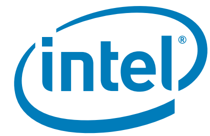


Figure 11. Ready/Busy# Open Drain

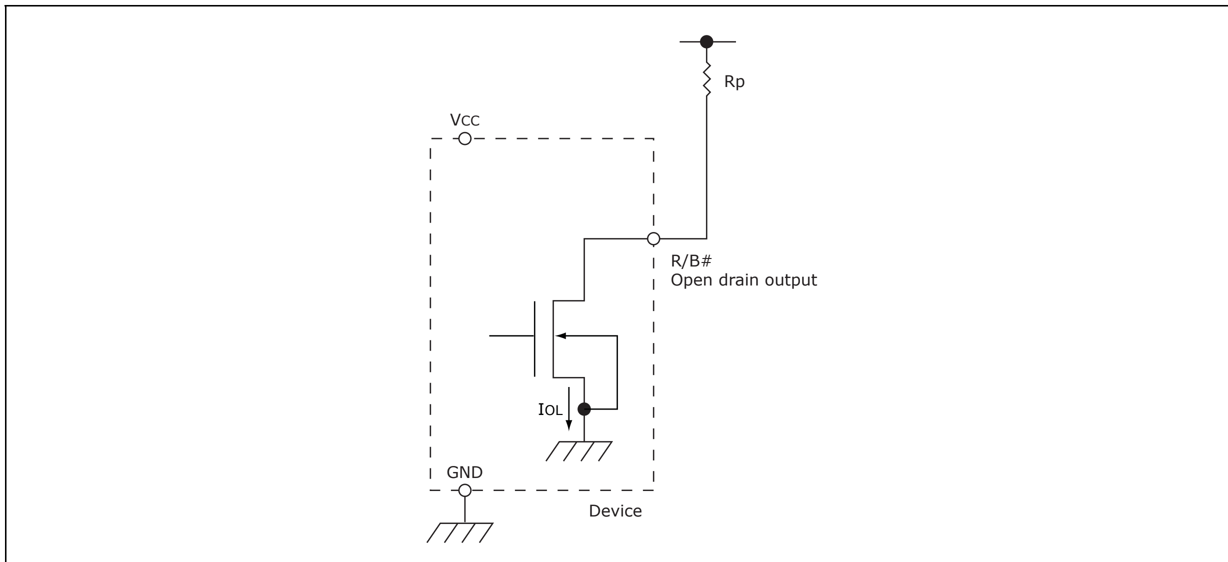
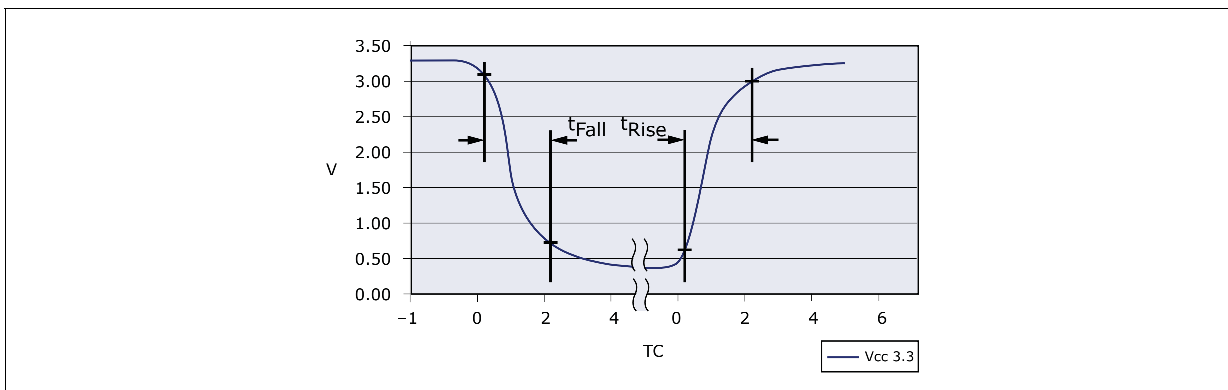


Figure 12. ^{t}Fall and ^{t}Rise



Notes:

1. ^{t}Fall and ^{t}Rise calculated at 10 percent–90 percent points.
2. ^{t}Rise dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}Rise primarily dependent on external pull-up resistor and external capacitive loading.
4. ^{t}Fall ≈ 10 ns at 3.3 V.
5. See TC values in Figure 14 on page 18 for approximate Rp value and TC.

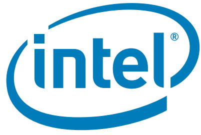


Figure 13. IOL versus Rp

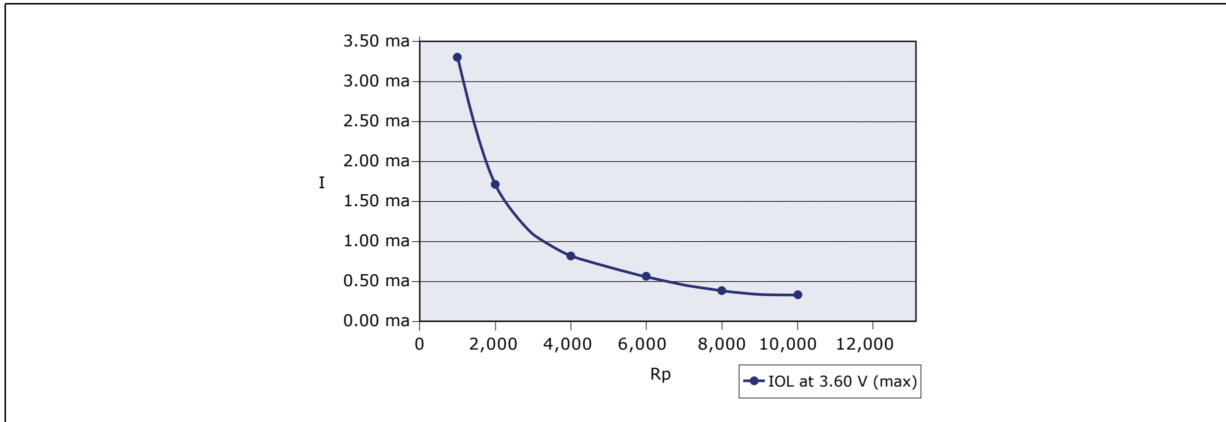
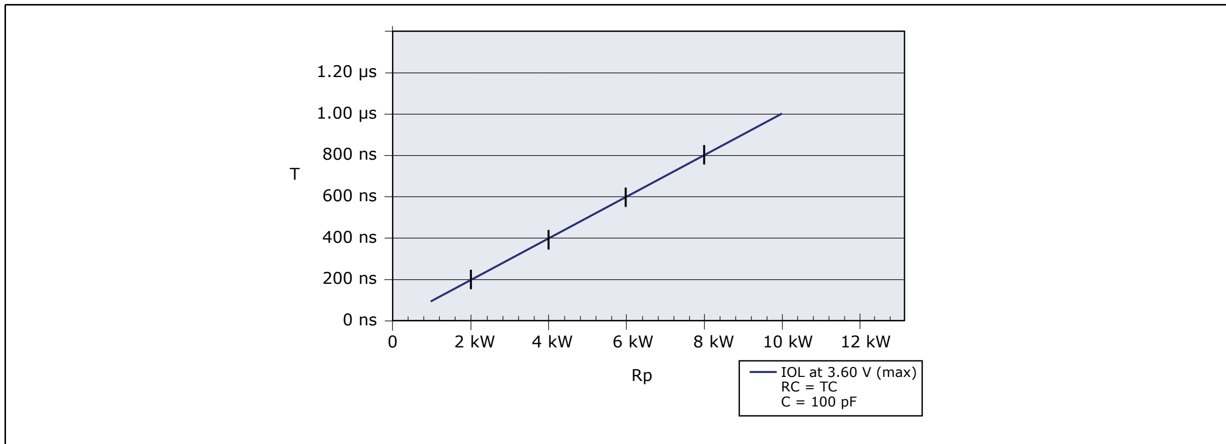


Figure 14. TC versus Rp



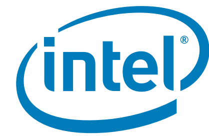


Table 4. Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read mode	Command input
L	H	L	↑	H	X		Address input
H	L	L	↑	H	H	Write mode	Command input
L	H	L	↑	H	H		Address input
L	L	L	↑	H	H	Data input	
L	L	L	H	↓	X	Sequential read and data output	
X	X	X	H	H	X	During read (busy)	
X	X	X	X	X	H	During program (busy)	
X	X	X	X	X	H	During erase (busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0 V/Vcc[1]	Standby	

Notes:
1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table:
   H = Logic level HIGH;
   L = Logic level LOW;
   X = V_{IH} or V_{IL}.

7.0 Command Definitions

Table 5. Command Set

Command	Command Cycle 1	Number of Address Cycles	Data Input Cycles	Command Cycle 2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Reset Commands							
RESET	FFh	0	–	–	Yes	Yes	
Identification Commands							
READ ID	90h	1	–	–			
READ PARAMETER PAGE	ECh	1	–	–			
READ UNIQUE ID	EDh	1	–	–			
One Time Programmable (OTP) Commands							
OTP DATA PROGRAM	A0h-10h						
OTP DATA PROTECT	A5h-10h						
OTP DATA READ	Afh-30h						
Configuration Commands							
SET FEATURES	EFh	1	4	–			3
GET FEATURES	EEh	1	–	–			
Status Commands							
READ STATUS	70h	0	–	–	Yes		
Column Address Commands							
CHANGE READ COLUMN	05h	2	–	E0h		Yes	
CHANGE WRITE COLUMN	85h	5	Yes	10h		Yes	

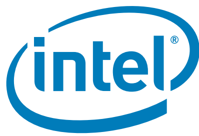


Table 5. Command Set (Continued)

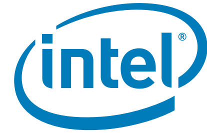
Command	Command Cycle 1	Number of Address Cycles	Data Input Cycles	Command Cycle 2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Read Commands							
READ	00h	5	–	30h		Yes	
Read Cache Commands							
READ CACHE SEQUENTIAL	31h	–	–	–		Yes	4
READ CACHE RANDOM	00h	5	–	31h		Yes	4
READ CACHE END	3Fh	0	–	–		Yes	4
Program Commands							
PAGE PROGRAM	80h	5	Yes	10h		Yes	
PAGE CACHE PROGRAM	80h	5	Yes	15h		Yes	5
Erase Commands							
BLOCK ERASE	60h	3	–	D0h		Yes	
Commands							
COPYBACK READ	00h	5	–	35h		Yes	
COPYBACK PROGRAM	85h	5	Optional	10h		Yes	

Notes:
1. Busy means SR6 = "0".
2. These commands may be used for Multi-LUN operations.
3. The SET FEATURES (Eh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
4. Issuing a READ CACHE series (31h, 00h-31h, 00h-32h, 3Fh) command during Array Busy is permissible if the previous command is a READ (00h-30h) or READ CACHE series command, otherwise it is prohibited.
5. Issuing a PAGE CACHE PROGRAM command during Array Busy (SR[6:5] = "10") is permissible if the previous command is a PAGE CACHE PROGRAM command, otherwise it is prohibited.

Table 6. MULTI-PLANE Command Set

Command	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Command Cycle 3	Valid During Busy	Notes
READ MULTI-PLANE	00h	5	32h-00h	5	30h	No	1
SELECT CACHE REGISTER	06h	5	E0h	–	–	No	
READ STATUS ENHANCED	78h	3	–	–	–	Yes	3
PAGE PROGRAM MULTI-PLANE	80h	5	11h-80h	5	10h	No	3
PAGE CACHE PROGRAM MULTI-PLANE	80h	5	11h-80h	5	15h	No	3
COPYBACK READ MULTI-PLANE	00h	5	00h	5	35h	No	2
COPYBACK PROGRAM MULTI-PLANE	85h	5	11h-85h	5	10h	No	2,3
ERASE BLOCK MULTI-PLANE	60h	3	D1h-60h	3	D0h	No	3

Notes:
1. READ MULTI_PLANE sequence: 00h-5addr(P0)-32h-tDBSY-00h-5addr(P1)-30h
   Refer to Section 7.11.1, "READ MULTI-PLANE 00h-32h-00h-30h" on page 50 for more details.
2. Do not cross plane address boundaries when using COPYBACK READ MULTI-PLANE and COPYBACK PROGRAM MULTI-PLANE. See Figure 7 on page 12 for plane address boundary definitions.
3. These commands are valid during busy when interleaved die operations are being performed.
4. Multi-plane read cache mode is supported. 00h-5addr(P0)-00h-5addr(P1)-31h as well as 00h-5addr(P0)-32h-00h-5addr(P1)-31h are acceptable.



7.1 Reset Commands

The RESET (FFh) command is used to put the memory device into a known condition and to abort a command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

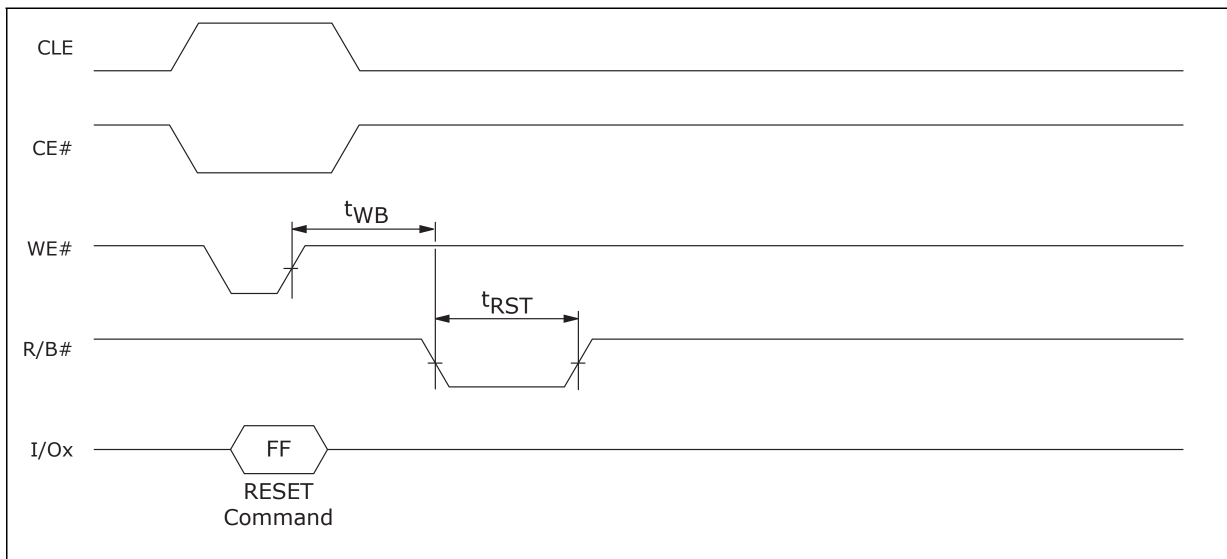
If a RESET (FFh) command is issued during any type of programming operation (PAGE PROGRAM, PAGE CACHE PROGRAM, COPYBACK PROGRAM, PAGE PROGRAM MULTI-PLANE, PAGE CACHE PROGRAM MULTI-PLANE, or COPYBACK READ MULTI-PLANE) while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting any programming operation on one page could corrupt the data in another page within the block being programmed.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes low for ^{t}RST after the ‘RESET command is written to the command register (see Figure 15 and Table 7).

The RESET command must be issued as the first command to all CE#s after power-on. The device will be busy for a maximum of 1 ms. During and following the initial RESET command, and prior to issuing the next command, use of the READ STATUS ENHANCED (78h) command is prohibited.

If the RESET command is issued during or following an interleaved-die operation then the READ STATUS ENHANCED (78h) command must be issued, once per die, to determine completion of the RESET operation. Use of the READ STATUS (70h) command is not permitted until the 78h command is issued.

Figure 15. RESET Operation



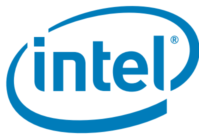


Table 7. Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

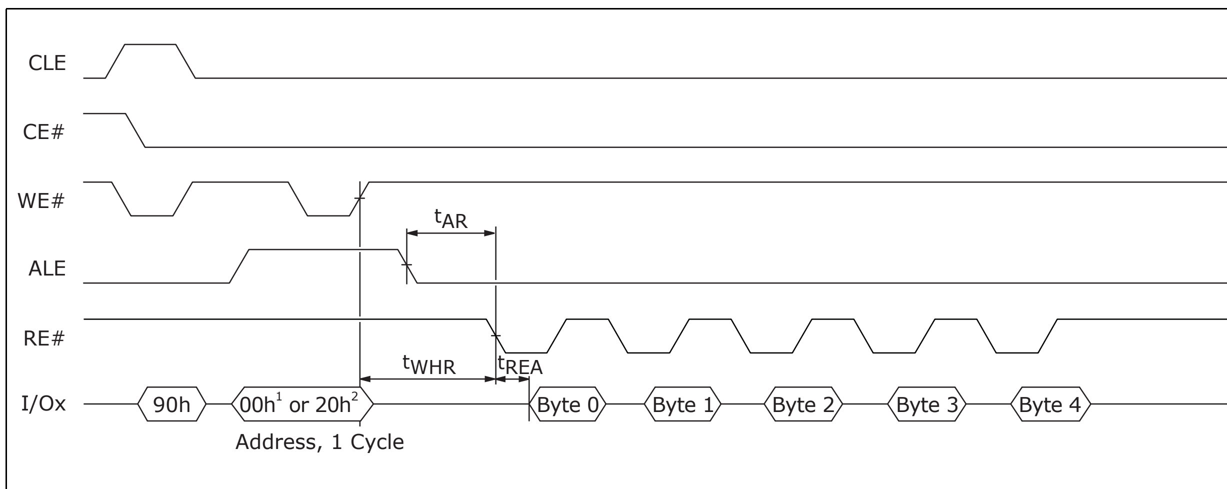
7.2 Identification Commands

7.2.1 READ ID 90h

The READ ID command is used to read the five bytes of identifier codes programmed into the devices. The READ ID command reads a five-byte table that includes Manufacturer's ID, device configuration, and part-specific information. See Table 8 on page 23 and Table 9 on page 23 which shows complete listings of all configuration details.

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued (see figure below**). For address 00h, bytes 5 to 7 are unknown reserve bytes.** The device will repeatedly output the same eight bytes of data if the host continues to toggle RE#. For address 20h, the device will repeatedly output the same four bytes of data if the host continues to toggle RE#.

Figure 16. READ ID Operation



Notes:
1. See Table 8 on page 23 for byte definitions with address 00h.
2. See Table 9 on page 23 for byte definitions with address 20h.

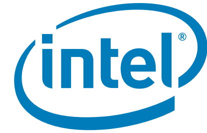


Table 8. Device ID and Configuration Codes

	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value[1]
Byte 0	**Manufacturer ID**									
	Intel	1	0	0	0	1	0	0	1	89h
Byte 1	**Device ID**									
Vcc	3.3 V					1	0	0	0	
Density per CE#	32 Gb, x8, 3 V	0	1	1	0					
	64 Gb, x8, 3 V	1	0	0	0					
	128 Gb, x8, 3 V	1	0	1	0					
Byte Value	MLC SDP with 1 CE#	0	1	1	0	1	0	0	0	68h
Byte 2										
Number of LUN per CE	1							0	0	00b
Cell type	MLC					0	1			01b
VccQ	Not Used	0	0	0	0					00b
Byte value										04h
Byte 3										
Page Size	4 KB							1	0	10b
Spare area size per 512 B	28 B					0	1			01b
Page per block	256		1	0	0					100b
Multi-LUN operations	Not Supported	0								0b
Byte value		0	1	0	0	0	1	1	0	46h
Byte 4										
Planes per LUN	2							0	1	01b
Block per LUN	4,096				0	1	0			010b
Timing Mode Asynchronous	5 (20 ns)	1	0	1						1000b
Byte Value		1	0	1	0	1	0	0	1	A9h

Note: b = binary, h = hex

Table 9. Device ID and Configuration Codes for ONFI Address (20h)

Address = 20h	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value*
Byte 0	"O"	0b	1b	0b	0b	1b	1b	1b	1b	4Fh
Byte 1	"N"	0b	1b	0b	0b	1b	1b	1b	0b	4Eh
Byte 2	"F"	0b	1b	0b	0b	0b	1b	1b	0b	46h
Byte 3	"I"	0b	1b	0b	0b	1b	0b	0b	1b	49h

Note: b = binary, h = hex

7.2.2 READ PARAMETER PAGE ECh

When issued the READ PARAMETER PAGE (ECh) command returns information about the device configuration. CHANGE READ COLUMN (05h-E0h) is permitted during data output. READ STATUS (70h) may be used to check the status of the Read Parameter Page command. After reading status, issue 00h to resume reading parameter page. Refer to the Open NAND Flash Interface Specification (ONFI) for the parameter page data structure definition. The data structure is defined at least five times. Reading bytes beyond the final parameter page copy returns indeterminate values.

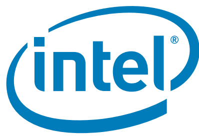
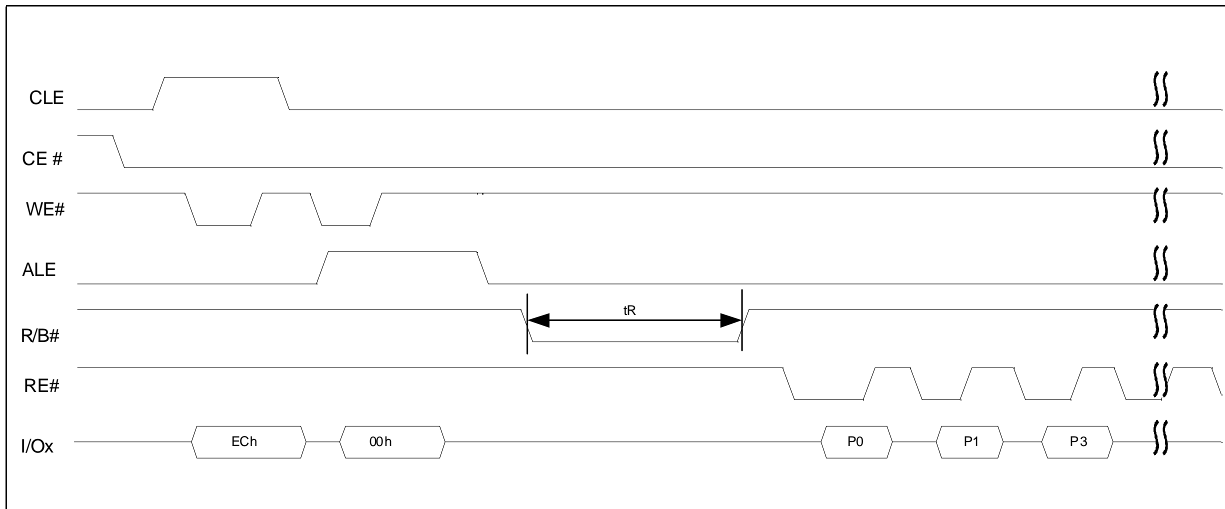


Figure 17. READ PARAMETER PAGE (ECh)



The following table shows the values returned by the READ PARAMETER PAGE (ECh) command.

Table 10. Read Parameter Data Structure

Byte	O/M	Description	MD332B Value
Revision Information and Features Block			
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number Bit 2-15: Reserved (0) Bit 1: 1 = supports ONFI version 2.0 Bit 0: Reserved (0)	06h, 00h
6-7	M	Features supported Bit 5-15: Reserved (0) Bit 4: 1 = supports odd to even page copyback Bit 3: 1 = supports interleaved operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple logical unit (LUN) operations Bit0: 1 = supports 16-bit data bus width	18h, 00h

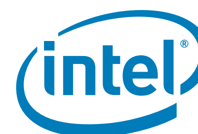


Table 10. Read Parameter Data Structure (Continued)

Byte	O/M	Description	MD332B Value
8-9	M	Optional commands supported Bit 6-15: Reserved (0) Bit 5:1 = supports READ UNIQUE ID Bit 4:1 = supports COPYBACK READ Bit 3:1 = supports READ STATUS ENHANCED Bit 2:1 = supports GET FEATURES and SET FEATURES Bit 1:1 = supports read cache commands Bit 0:1 = supports PAGE CACHE PROGRAM command	3Fh, 00h
10-31		Reserved (0)	00h
Manufacturer information block			
32-43	M	Device manufacturer (12 ASCII characters)	49h, 4Eh, 54h, 45h, 4Ch, 00h, 00h, 00h, 00h, 00h, 00h, 00h
44-63	M	Device model (20 ASCII characters) JS29F32G08AAMDB JS29F64G08CAMDB JS29F16B08JAMDB	 4Ah, 53h, 32h, 39h, 46h, 33h, 32h, 47h, 30h, 38h, 41h, 41h, 4Dh, 44h, 42h, 00h, 00h, 00h, 00h, 00h 4Ah, 53h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 43h, 41h, 4Dh, 44h, 42h, 00h, 00h, 00h, 00h, 00h 4Ah, 53h, 32h, 39h, 46h, 31h, 36h, 42h, 30h, 38h, 4Ah, 41h, 4Dh, 44h, 42h, 00h, 00h, 00h, 00h, 00h
64	M	JEDEC manufacturer ID	89h
65-66	O	Date code	00h, 00h
67-79		Reserved (0)	00h
Memory Organization Block			
80-83	M	Number of data bytes per page 4096	00h, 10h, 00h, 00h
84-85	M	Number of spare bytes per page 224	E0h, 00h
86-89	M	Number of data bytes per partial page 512	00h, 02h, 00h, 00h
90-91	M	Number of spare bytes per partial page 28 (224/(4096/512)=28)	1Ch, 00h
92-95	M	Number of pages per block 256	00h, 01h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN) 4,096	00h, 10h, 00h, 00h
100	M	Number of logical units (LUNs): 32 Gb: 1 64 Gb: 1 128 Gb: 1	 01h 01h 01h

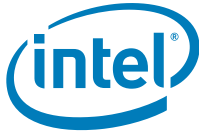


Table 10. Read Parameter Data Structure (Continued)

Byte	O/M	Description	MD332B Value
101	M	Number of address cycles Bit 4-7: Column address cycles Bit 0-3: Row address cycles	23h
102	M	Number of bits per cell MLC	02h
103-104	M	Bad blocks maximum per logical unit (LUN) 160	A0h, 00h
105-106	M	Block endurance 5,000	05h, 03h
107	M	Guaranteed valid blocks at beginning of target 1 (block 0)	01h
108-109	M	Block endurance for guaranteed valid blocks	Contact factory
110	M	Number of programs per page 1	01h
111	M	Partial programming attributes Bit 5-7: Reserved Bit 4:1 = partial page layout is partial page data followed by partial page spare Bit 1-3: Reserved Bit 0:1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability 12	0Ch
113	M	Number of interleaved address bits Bit 4-7: Reserved (0) Bit 0-3: Number of interleaved address bits	01h
114	O	Interleaved operation attributes Bit 4-7: Reserved (0) Bit 3:1 = Address restrictions for program cache Bit 2:1 = Program cache supported Bit 1:1 = No block address restrictions Bit 0: Overlapped/concurrent interleaving support	0Eh
115-127		Reserved (0)	00h
Electrical Parameters Block			
128	M	I/O pin capacitance 10 pF	0Ah
129-130	M	Timing mode support Bit 6-15Reserved (0) Bit 5:1 = supports timing mode 5 Bit 4:1 = supports timing mode 4 Bit 3:1 = supports timing mode 3 Bit 2:1 = supports timing mode 2 Bit 1:1 = supports timing mode 1 Bit 0:1 = supports timing mode 0, shall be 1	3Fh, 00h

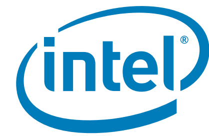


Table 10. Read Parameter Data Structure (Continued)

Byte	O/M	Description	MD332B Value
131-132	O	Program cache timing mode support Bit 6-15: Reserved (0) Bit 5:1 = supports timing mode 5 Bit 4:1 = supports timing mode 4 Bit 3:1 = supports timing mode 3 Bit 2:1 = supports timing mode 2 Bit 1:1 = supports timing mode 1 Bit 0:1 = supports timing mode 0	3Fh, 00h
133-134	M	^{t}PROG Maximum page program time (µs) 2200 µs	98h, 08h
135-136	M	^{t}BERS Maximum block erase time 10 ms	10h, 27h
137-138	M	^{t}R Maximum page read time (µs) 50 µs	32h, 00h
139-140	M	^{t}CCS Minimum change column setup time (ns) 200 ns	C8h, 00h
141-142		Source synch timing mode support	00h, 00h
143		Source synch features	00h
144-145		CLK input pin capacity (TYP)	00h, 00h
146-147		I/O pin capacity (TYP)	00h, 00h
148-149		Input pin capacity (TYP)	00h, 00h
150		Input pin capacity (MAX)	00h
151		Driver strength support	00h
152-163		Reserved (0)	00h
164-179		Reserved (0)	00h
180-253		Reserved (0)	00h
254-255		Integrity CRC 32 Gb 64 Gb 128 Gb	 TBD TBD TBD
Redundant Parameter Pages			
256-511	M	Value of bytes 0-255	
512-767	M	Value of bytes 0-255	
768+	O	Additional redundant parameter pages	

7.2.3 READ UNIQUE ID EDh

Intel offers the READ UNIQUE ID command feature to provide a method for uniquely identifying a NAND Flash device. The READ UNIQUE ID operation uses standard command and address timing. The format of the ID is arbitrary; however, this ID is guaranteed to be unique for every NAND Flash device manufactured.

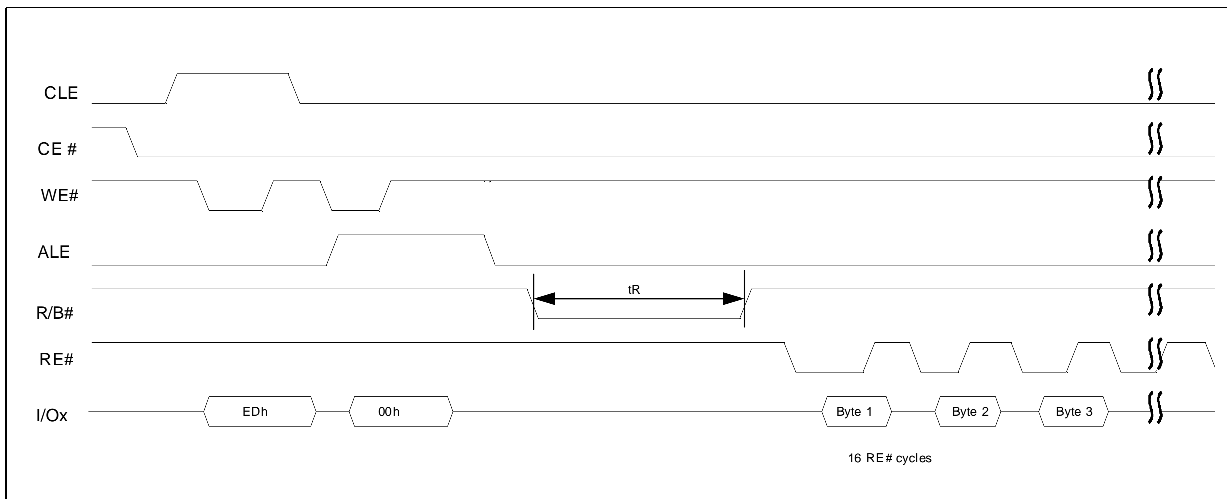
Many controllers use proprietary error correction code (ECC) schemes; thus, it is not possible for Intel to protect unique ID data with factory-programmed ECC. However, to ensure data integrity, Intel programs the noted NAND Flash devices with a 16-byte unique ID, beginning at byte 0 of the page, then follows with 16 bytes of complement ID. These 32 bytes of data are then repeated a total of 16 times, such that the last byte

of the last copy of complement unique ID resides at byte 511 in the page. The user can simply XOR the first copy of the unique ID and its complement. If the result is 0, the unique ID is good. In the unlikely event that the result is non-zero, the user can repeat the XOR operation on a subsequent copy of the unique ID data.

The figure below shows timing for the READ UNIQUE ID command. Unique ID data is simply stored on consecutive bytes for X8 devices. Normal page read timings apply for READ UNIQUE ID operations. To exit READ UNIQUE ID, cycle power on the NAND Flash device or issue a RESET command.

READ STATUS (70h) is valid. After reading status, issue 00h to resume READ UNIQUE ID. CHANGE READ COLUMN (05h-E0h) is also supported. Reading bytes beyond the final Unique ID copy returns indeterminate values.

Figure 18. Read Unique ID



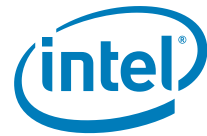
7.3 One Time Programmable (OTP) Commands

This Intel NAND Flash device offers a protected, one-time programmable Flash memory area. Thirty full pages of OTP data is available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Intel NAND Flash devices, the OTP area leaves the factory in an erased state (all bits are “1”s). Programming or partial-page programming enables the user to program only “0” bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as “one-time programmable,” Intel provides a unique way to program and verify data—before permanently protecting it and preventing future changes.

The OTP area is only accessible while in OTP-operation mode. To set the device to OTP-operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2 through P4.



When the device is in OTP-operation mode, all subsequent READ (00h-30h) and PAGE PROGRAM (80h-10h) commands are applied to the OTP area. The OTP area is assigned to 02h through 1Fh in block 0.

OTP programming and protection are achieved in two discrete operations. Each page in the OTP area is programmed using the PAGE PROGRAM operation. The pages in the OTP area (02h-1Fh) must be programmed in ascending order.

To protect the OTP area, issue the 80h command followed by five address cycles (00h-00h-01h-00h-00h), followed by one data cycle of 00h, followed by the 10h command. R/B# goes LOW for ^{t}PROG.

To read pages in the OTP area, whether or not it is protected, issue the READ (00h-30h) command. Erase commands are not valid while the device is in OTP-operation mode.

To exit OTP-operation mode, write 00h to P1 at feature address 90h. At power-on P1 is 00h by default.

To determine whether or not the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the READ STATUS ENHANCED (78h) command is prohibited during and following OTP operations.

7.3.1 OTP DATA PROGRAM

The OTP DATA PROGRAM command is used to write data to the pages within the OTP area. An entire page is programmed at one time.To program data in the OTP area, the device must be in OTP-operation mode. To set the device to OTP-operation mode, issue the SET FEATURES (EFh) command, followed by feature address 90h. Then write 01h-00h-00h-00h to P1 through P4, respectively. When the device is in OTP-operation mode, use the PAGE PROGRAM (80h-10h) command to write data to the pages within the OTP area. There is no ERASE operation for the OTP pages.

PAGE PROGRAM enables programming into an offset of an OTP page, using the two bytes of column address (CA[12:0]). The command is compatible with the CHANGE WRITE COLUMN (85h) command. The PAGE PROGRAM command will not execute if the OTP area has been protected.

To use the PAGE PROGRAM command, issue the 80h command. Issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 1Fh-00h-00h. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification. Program verification only detects “1s” that are not successfully written to “0s.”

R/B# goes LOW for the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only valid command for reading status in OTP-operation mode. Bit 5 of the status register will reflect the state of R/B#.

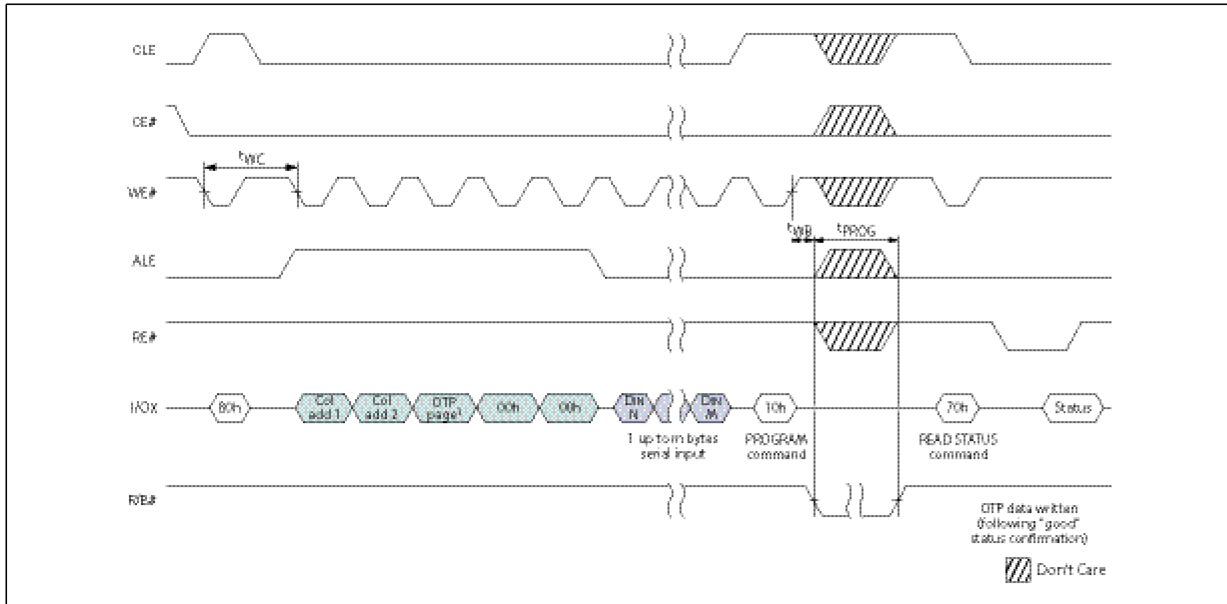
When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 15, “Status Register Bit Definition” on page 38).

It is possible to program each OTP page a maximum of eight times.

The PAGE PROGRAM command also accepts the CHANGE WRITE COLUMN (85h) command (see Figure 28 on page 40).

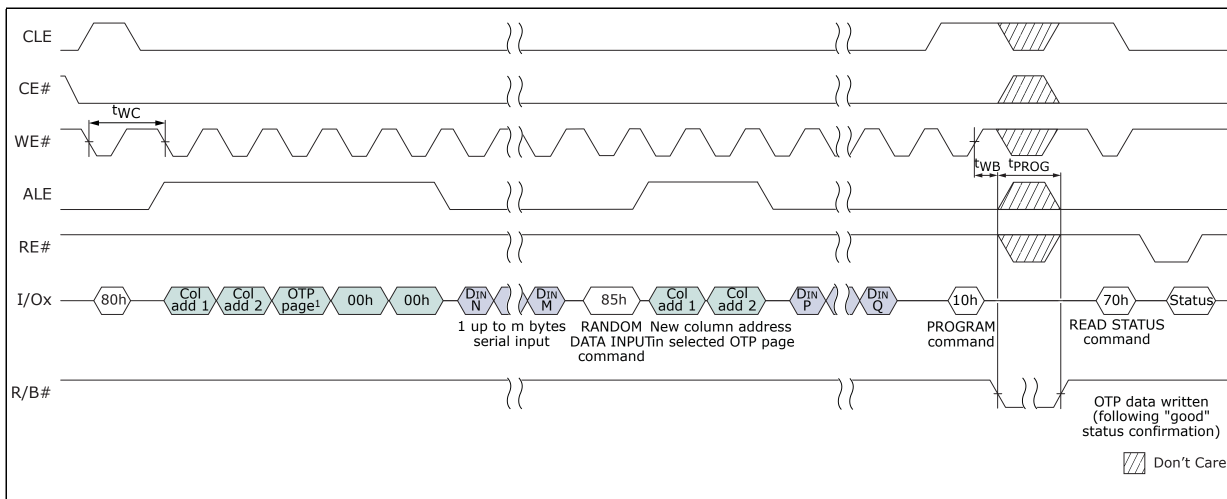
If a PAGE PROGRAM command is issued to the OTP area after the area has been protected, R/B# will go LOW for ᵗOBSY.

Figure 19. OTP DATA PROGRAM

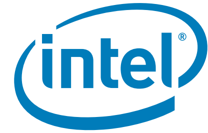


Note: The OTP page must be within the 02h-1Fh range.

Figure 20. OTP DATA PROGRAM with RANDOM DATA INPUT (After entering OTP-Operation Mode)



Note: The OTP page must be within the 02h-1Fh range.



7.3.2 OTP DATA PROTECT

To protect all data in the OTP area, set the device to OTP-operation mode, then issue the PAGE PROGRAM (80h-10h) command and write "00h" to column 0 of page 1 in block 0.

After the data is protected it can no longer be programmed. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

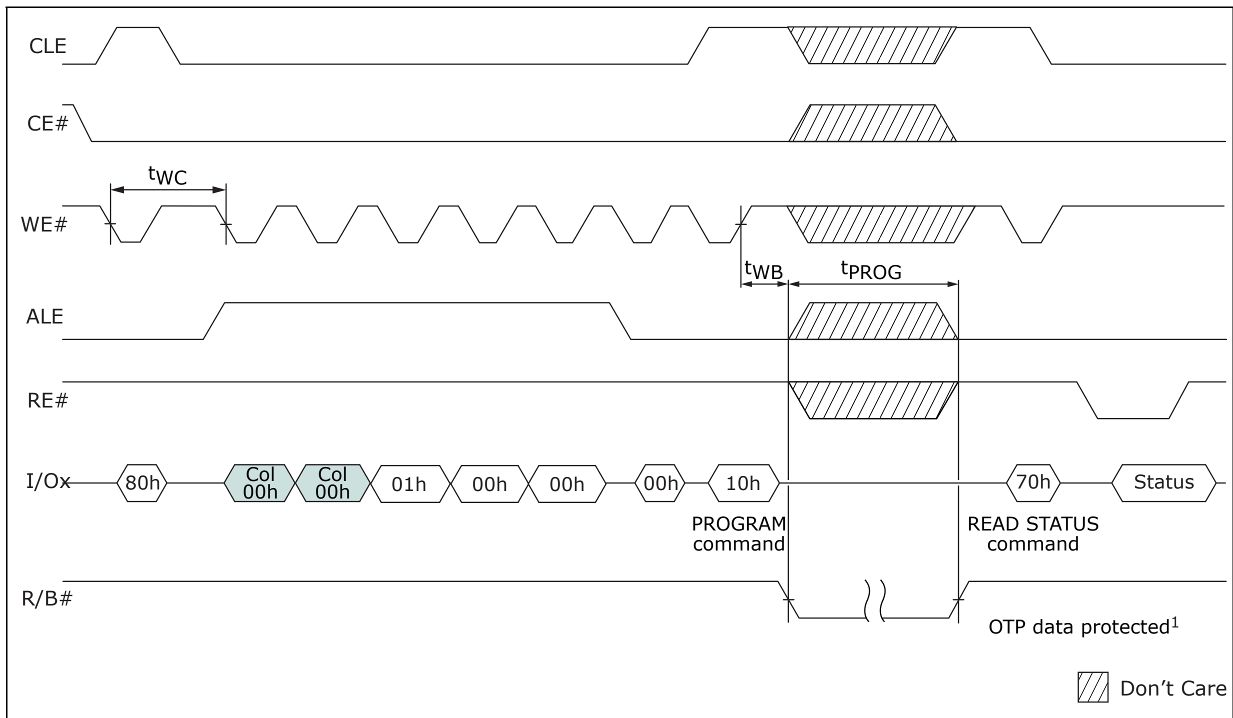
To use the PAGE PROGRAM command to protect the OTP area, issue the 80h command. Next, issue the following five address cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for ^{t}OBSY.

The READ STATUS (70h) and READ STATUS ENHANCED (78h) command are the only valid commands for reading status in OTP operation mode.

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 15, "Status Register Bit Definition" on page 38).

Figure 21. OTP DATA PROTECT (After entering OTP-Operation Mode)



Note: OTP data is protected following "good" status confirmation.

7.3.3 OTP DATA READ

To read data from the OTP area, set the device to OTP-operation mode, then issue the READ (00h-30h) command. Data can be read from OTP pages within the OTP area whether or not the area is protected.

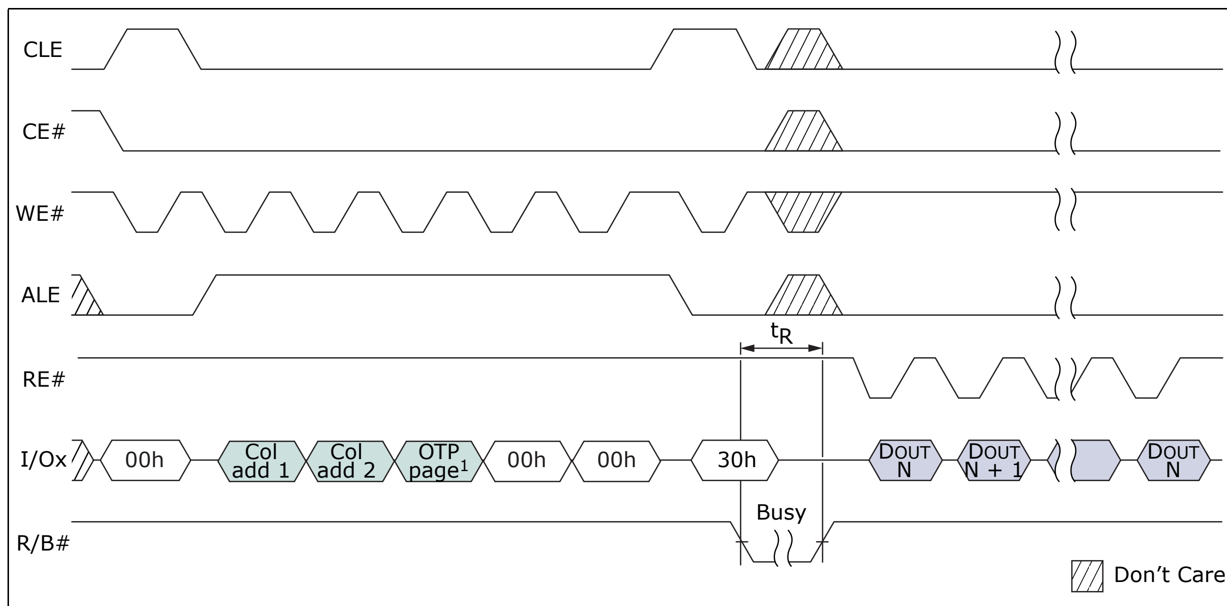
To use the READ command for reading data from the OTP area, issue the 00h command. Next, issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 1Fh-00h-00h. Finally, issue the 30h command.

R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command is the only valid command for reading status in OTP- operation mode. Bit 5 of the status register will reflect the state of R/B#. For details, refer to Table 15, “Status Register Bit Definition” on page 38.

Normal READ operation timings apply to OTP read accesses (see Figure 22). Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

The READ command is compatible with the CHANGE READ COLUMN (05h-E0h) command.

Figure 22. OTP DATA READ (After Entering OTP-Operation Mode)



Note: The OTP page must be within the 02h-1Fh range.

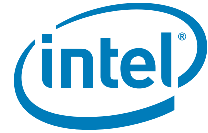
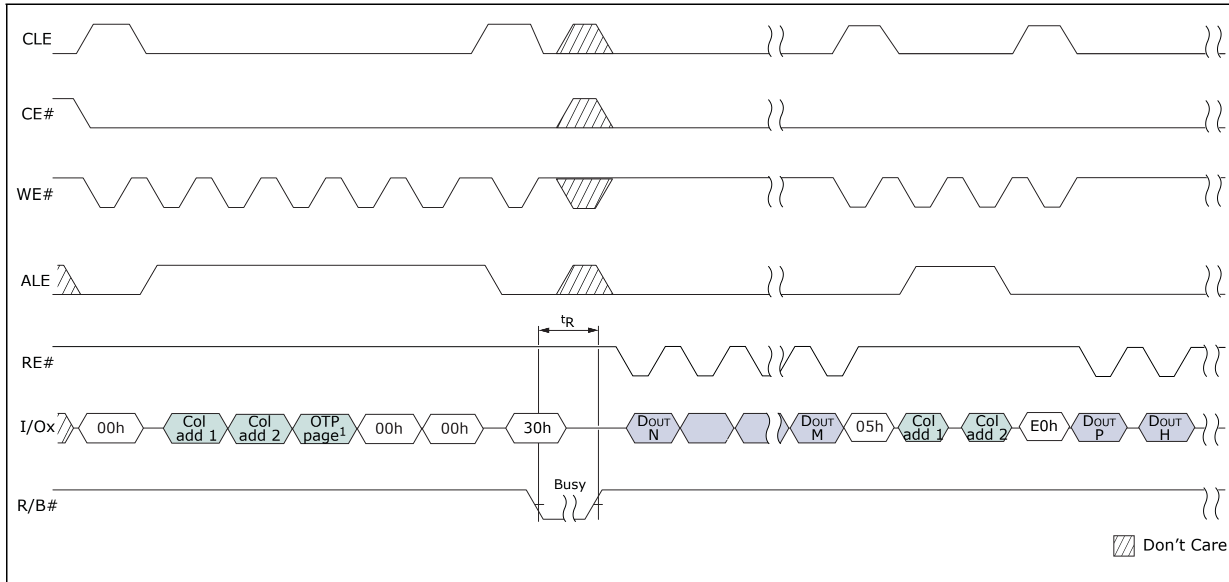


Figure 23. OTP DATA READ with RANDOM DATA READ (After Entering OTP-Operation Mode)



Note: The OTP page must be within the 02h-1Fh range.

7.4 Configuration Commands

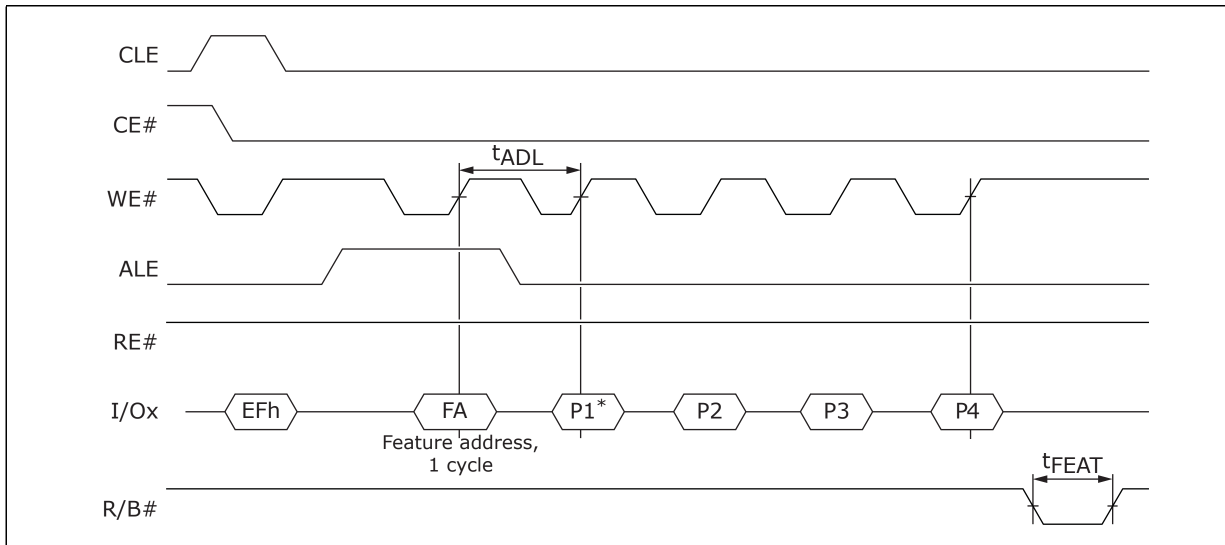
The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to alter NAND Flash device default power-on behaviors. These commands use a one-byte feature address to determine which sub-feature parameters are to be read or modified. Each feature address (in the range of 00h to FFh) is defined in Table 11 on page 34. The GET FEATURES command reads the sub-feature parameters (P1-P4) at the specified feature address. The SET FEATURES (EFh) command places sub-feature parameters (P1-P4) at the specified feature address. When a feature is set, by default it lasts until the device is power-cycled. It is volatile. Unless otherwise specified in the Features table, once a device feature is set the feature remains set, even if a RESET (FFh) command is issued.

7.4.1 SET FEATURES EFh

The SET FEATURES command is used to set the sub-feature parameters at a specified feature address. These parameters are stored in the device until the device is powered down. The sub-feature parameters are applied to all die on the CE# to which this command is issued. Figure 24 on page 34 depicts SET FEATURES behavior and timing.

R/B# goes LOW for ^{t}FEAT while the sub-feature parameters are written to the specified feature address. All four sub-feature parameters must be issued to the device for the SET FEATURES command to work. The READ STATUS (70h) command and the RESET (FFh) command are the only valid commands during SET FEATURES operation. Bits 5 and 6 of the status register will reflect the state of R/B#.

Figure 24. SET FEATURES



Note: P1-P4 are the sub-feature parameters to be written to the specified feature address (FA).

Table 11. Features

Feature Address	Description
00h	Reserved
01h	Timing mode
02h–0Fh	Reserved
10h	Programmable Output drive strength
11h-7Fh	Reserved
80h	Programmable Output drive strength
81h	Programmable R/B# pull-down strength
82h-8Fh	Reserved
90h	Array Operation mode
91h-94h	Reserved
95h	Reserved
96h-FFh	Reserved

7.4.1.1 Timing Mode

The timing-mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands, address and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the part is power cycled. Supported timing modes are reported in the parameter page.

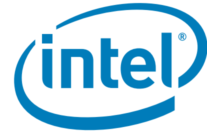


Table 12. Feature Address 01h: Timing Mode

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
P1										
Timing Mode	Mode 0 (default)	Reserved (0)					0	0	0	00h
	Mode 1	Reserved (0)					0	0	1	01h
	Mode 2	Reserved (0)					0	1	0	02h
	Mode 3	Reserved (0)					0	1	1	03h
	Mode 4	Reserved (0)					1	0	0	04h
	Mode 5	Reserved (0)					1	0	1	05h
P2										
Reserved		Reserved (0)								00h
P3										
Reserved		Reserved (0)								00h
P4										
Reserved		Reserved (0)								00h

7.4.1.2 Programmable I/O Drive Strength

Use the PROGRAMMABLE DRIVE STRENGTH feature to change the default I/O strength. Drive strength should be selected based on the expected loading of the memory bus. This table shows the four supported output drive-strength settings. The default drive-strength is full strength. The device returns to the default setting when power cycled. AC timing parameters need to be relaxed if the I/O drive strength is not set to full.

Table 13. Feature Address 10h and 80h: Programmable I/O Drive Strength

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
P1										
Output drive strength	Overdrive 2							0	0	00h
	Overdrive 1							0	1	01h
	Nominal (default)							1	0	02h
	Underdrive							**1**	1	03h
Reserved		0	0	0	0	0	0			00h
P2										
Reserved		Reserved (0)								00h
P3										
Reserved		Reserved (0)								00h
P4										
Reserved		Reserved (0)								00h

7.4.1.3 Programmable R/B# Pull-Down Strength

You can use the PROGRAMMABLE R/B# PULL-DOWN STRENGTH feature to change the R/B# pull-down strength. Pull-down strength should be selected based on the expected loading of R/B#. This table shows the four supported pull-down settings. The default setting is full strength. The device returns to the default setting when power cycled.

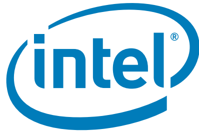


Table 14. Feature Address 90h: Array Operation Mode

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
P1										
Array Operation Mode	Normal (default)*								0	00h
	OTP								1	01h
Reserved		Reserved (0)								00h
P2										
Reserved		Reserved (0)								00h
P3										
Reserved		Reserved (0)								00h
P4										
Reserved		Reserved (0)								00h

Note: See Section 7.3, "One Time Programmable (OTP) Commands" on page 28 for details.

7.4.2 GET FEATURES EEh

Use this command to retrieve a stored feature. P1-P4 are the parameters for the specified Feature Address (FA). If a parameter, P1 through P4, has values defined as "reserved," the device must return a "0" for all bits in the parameter defined as reserved.

R/B# goes LOW (^{t}FEAT) while the sub-feature parameters are being loaded from the specified feature address. The READ STATUS (70h) and RESET (FFh) commands are available during the busy time and before data output. Bits 5 and 6 of the status register will reflect the state of R/B#. After reading the status, issue the 00h command to resume reading from the Feature address. The 70h command is not allowed when reading sub-feature parameters. The device will repeatedly output the same four bytes of data if the host continues to toggle RE#.

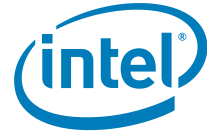
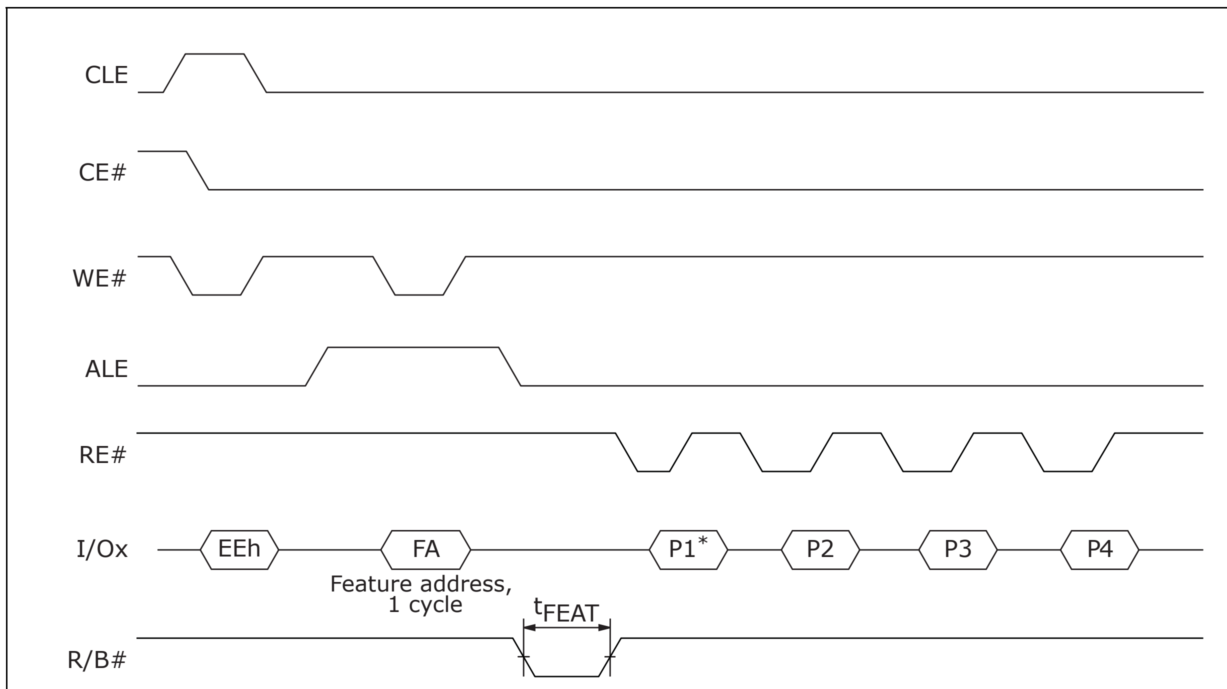


Figure 25. GET FEATURES



Note: P1-P4 are the sub-feature parameters to be read from the specified feature address (FA).

7.5 Status Commands

7.5.1 READ STATUS 70h

These NAND Flash devices have an 8-bit status register that the software can read during device operation. Table 15, "Status Register Bit Definition" on page 38 describes the status register.

After a READ STATUS command, all READ cycles will be from the status register until a new command is given. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ STATUS cycle to see these changes.

In devices that have more than one die sharing a common CE# pin, the READ STATUS (70h) command reports the status of the die that was last addressed. If concurrent operations are started on both die, then the TREAD STATUS ENHANCED (78h) command must be used to select the die that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as both die will respond until the next operation is issued.

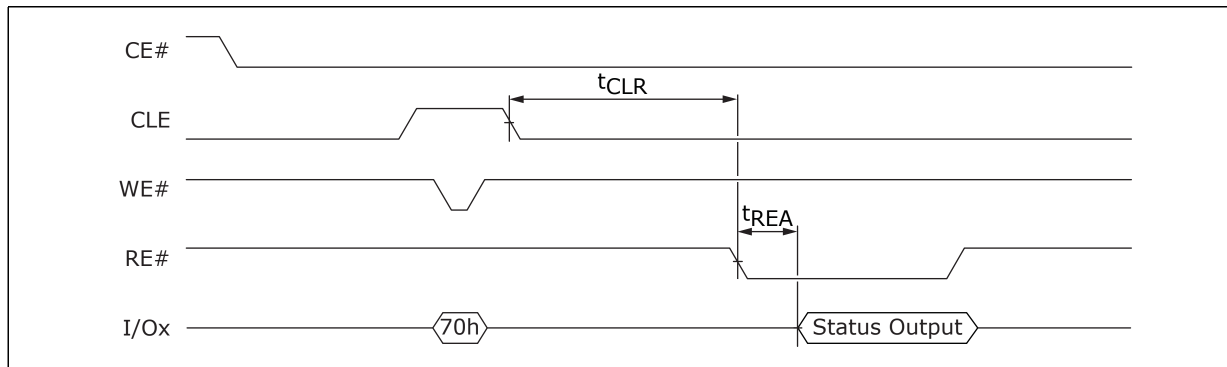
While monitoring the status register to determine when the ^{t}R (transfer from Flash array to data register) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

Table 15. Status Register Bit Definition

SR Bit	Page Program	Page Cache Program	Read	Read Cache	Block Erase	Definition
0[1]	Pass/fail	Pass/fail (N)	–	–	Pass/fail	"0" = Successful PROGRAM/ERASE "1" = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	"0" = Successful PROGRAM "1" = Error in PROGRAM
2	–	–	–	–	–	"0"
3	–	–	–	–	–	"0"
4	–	–	–	–	–	"0"
5	Ready/busy	Ready/busy[2]	Ready/busy	Ready/busy[2]	Ready/busy	"0" = Busy "1" = Ready
6	Ready/busy	Ready/busy cache[3]	Ready/busy	Ready/busy cache[3]	Ready/busy	"0" = Busy "1" = Ready
7[4]	Write protect	Write protect	Write protect	Write protect	Write protect	"0" = Protected "1" = Not protected
[15:8]	–	–	–	–	–	"0"

Notes:
1. Status register bit 0 reports a "1" if a PROGRAM/ERASE MULTI-PLANE operation fails on one or both planes. Status register bit 1 reports a "1" if a PAGE CACHE PROGRAM MULTI-PLANE operation fails on one or both planes. Use READ STATUS ENHANCED (78h) to determine the plane to which the operation failed.
2. Status register bit 5 is "0" during the actual programming operation. If cache mode is used, this bit will be "1" when all internal operations are complete.
3. Status register bit 6 is "1" when the cache register is ready to accept new data. R/B# follows bit 6. See Figure 30 on page 44, and Figure 32 on page 47.
4. Status register bit 7 typically mirrors the status of the WP# pin.

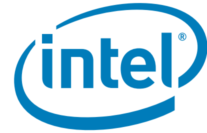
Figure 26. Status Register Operation



7.6 Column Address Commands

7.6.1 CHANGE READ COLUMN 05h-E0h

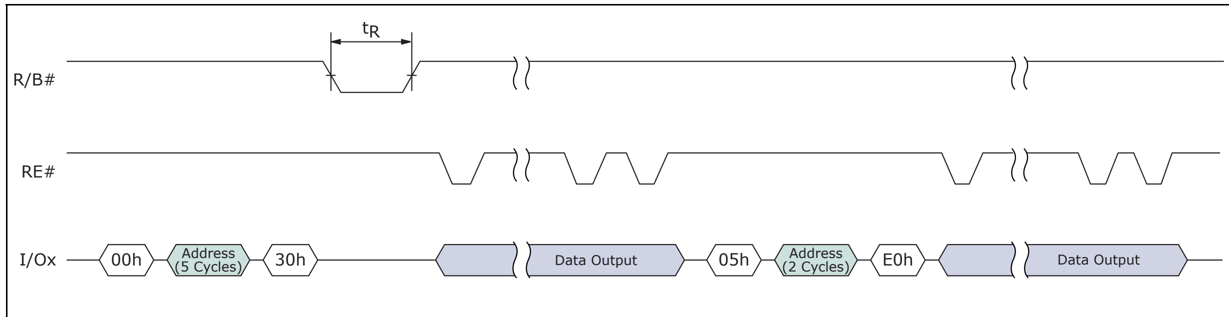
The CHANGE READ COLUMN command enables the user to specify a new column address so the data at single or multiple addresses can be read. The change read column mode is enabled after a normal READ (00h-30h sequence). When the Synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to "0") since data is transferred on DQ[7:0] in two-byte units.



Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (two cycles).

The CHANGE READ COLUMN command can be issued without limit within the page. Only data on the current page can be read. In asynchronous interface, pulsing the RE# pin outputs data sequentially (see figure below).

Figure 27. CHANGE READ COLUM Operation



7.6.2 CHANGE WRITE COLUMN 85h

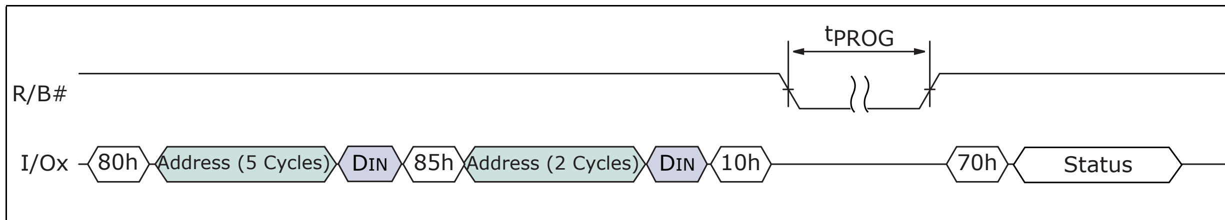
After the initial data set is input, additional data can be written with the CHANGE WRITE COLUMN (85h) command. The CHANGE WRITE COLUMN command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command. See Figure 28 for the proper command sequence.

When the Synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to “0”) since data is transferred on DQ[7:0] in two-byte units.

The CHANGE WRITE COLUMN command supposes two and five address cycles. Changing the plane address or the LUN address from the initial address is not allowed. The NAND device has the following behavior:

- If there are only two address input cycles, those are identified as column address.
- If there are only three address input cycles, the first two cycles are identified as column address and the last is ignored.
- If there are only four address input cycles, the first two cycles are identified as column address and the last two are ignored.
- If there are only five address input cycles, the first two cycles are identified as column address and the last three as row address.
- If there are more than five address input cycles, the extra cycles are ignored.

Figure 28. CHANGE WRITE COLUMN (Asynchronous Interface)



Note: This waveform only shows two address cycles, but the 85h command does support five address cycles.

7.7 Read Commands

7.7.1 READ 00h–30h

On power-on the device defaults to READ mode. To enter READ mode while in operation, write the 00h command to the command register, then write five ADDRESS cycles, and conclude with the 30h command.

To determine the progress of the data transfer from the Flash array to the data register (^{t}R), monitor the R/B# signal; or alternately, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must re-issue the READ (00h) command to receive data output from the data register. See Figure 92 on page 95 and Figure 93 on page 95 for examples. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate (see Figure 29).

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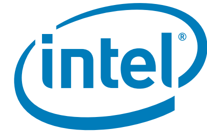
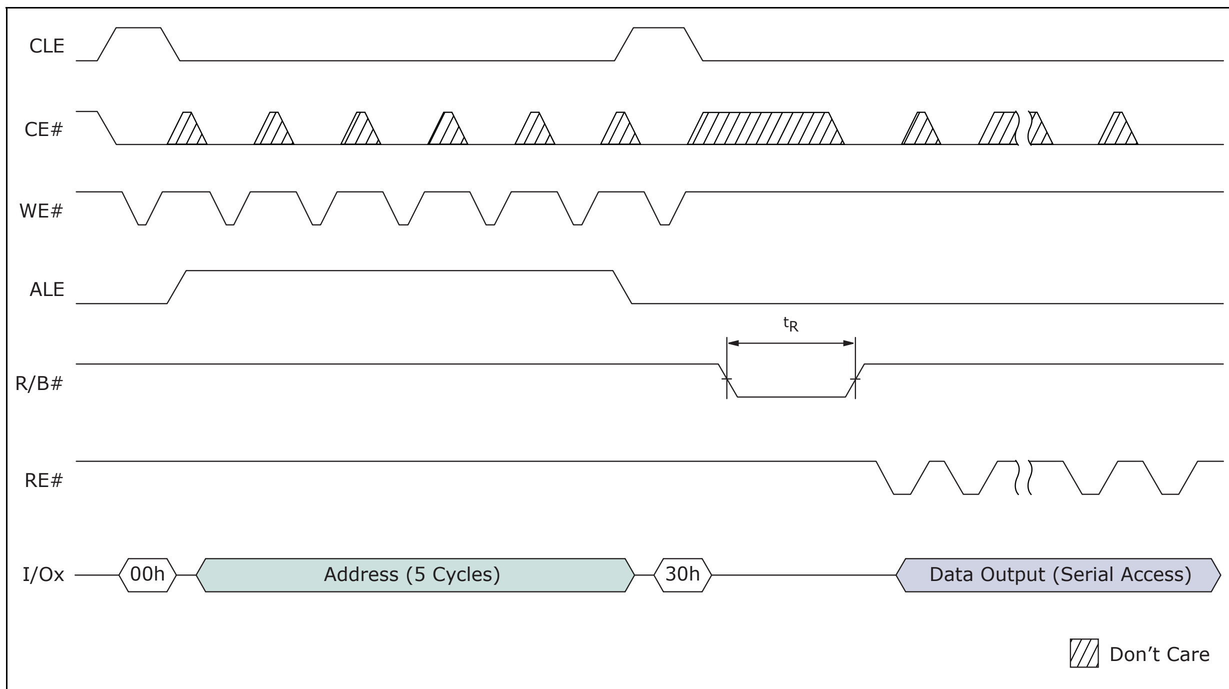


Figure 29. READ Operation



7.7.2 READ CACHE Operations

Intel NAND Flash devices have a cache register that can be used to increase READ operation speed. Data can be output from the device's cache register while concurrently moving a page from the NAND Flash array to the data register.

To begin a READ CACHE mode sequence, begin by reading a page from the NAND Flash array to the cache register using the READ (00h-30h) command (see "READ 00h–30h" on page 40). R/B# goes LOW during ^{t}R (status register bits 6 and 5 = 00). After ^{t}R (R/B# is HIGH and status register bits 6 and 5 = 11), issue either of these commands:

- READ CACHE SEQUENTIAL (31h) command to begin copying the next sequential page from the NAND Flash array to the data register
- READ CACHE RANDOM (00h-31h) command to begin copying the page specified in this command from the NAND Flash array to the data register.
- READ CACHE RANDOM (00h-31h) can cross block and plane address boundaries, but not die address boundary.

After the READ CACHE SEQUENTIAL or READ CACHE RANDOM command has been issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSY while the next page begins copying into the data register. After ^{t}RCBSY, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that a page is being copied from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the device.

After outputting the desired number of bytes from the cache register, it is possible to either begin an additional READ CACHE SEQUENTIAL (31h) or READ CACHE RANDOM (00h-31h) operation or issue the READ CACHE END (3Fh) command.

If an additional READ CACHE SEQUENTIAL (31h) or READ CACHE RANDOM (00h-31h) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSY while the data register is copied to the cache register, then the next page begins copying into the data register. After ^{t}RCBSY, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the device.

If the READ CACHE END (3Fh) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSY while the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH and status register bits 6 and 5 = 11, indicating that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the device.

During device busy times, ^{t}RCBSY, the only valid commands are READ STATUS (70h), READ STATUS EHANCED (78h), and RESET (FFh). Until status register bit 5 = 1, the only valid commands during READ CACHE mode operations are READ STATUS EHANCED (78h), READ (00h), READ CACHE SEQUNTIAL (31h), READ CACHE RANDOM (00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh).

7.7.3 READ CACHE SEQUENTIAL 31h

The READ CACHE SEQUENTIAL (31h) command reads the next sequential page into the data register while the previous page is output from the cache register. To issue this command, write 31h to the command register.

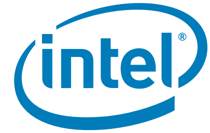
After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register by toggling RE# beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the device.

Do not issue the 31h command after reading the last page of the block into the data register. Instead, issue the 3Fh command. Crossing block boundaries with the READ CACHE SEQUENTIAL (31h) command is prohibited.

7.7.4 READ CACHE RANDOM 00h-31h

The READ CACHE RANDOM (00h-31h) command reads the specified page into the data register while the previous page is output from the cache register. To issue this command, write 00h to the command register, then write five address cycles to the address register. Conclude the sequence by writing 31h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from



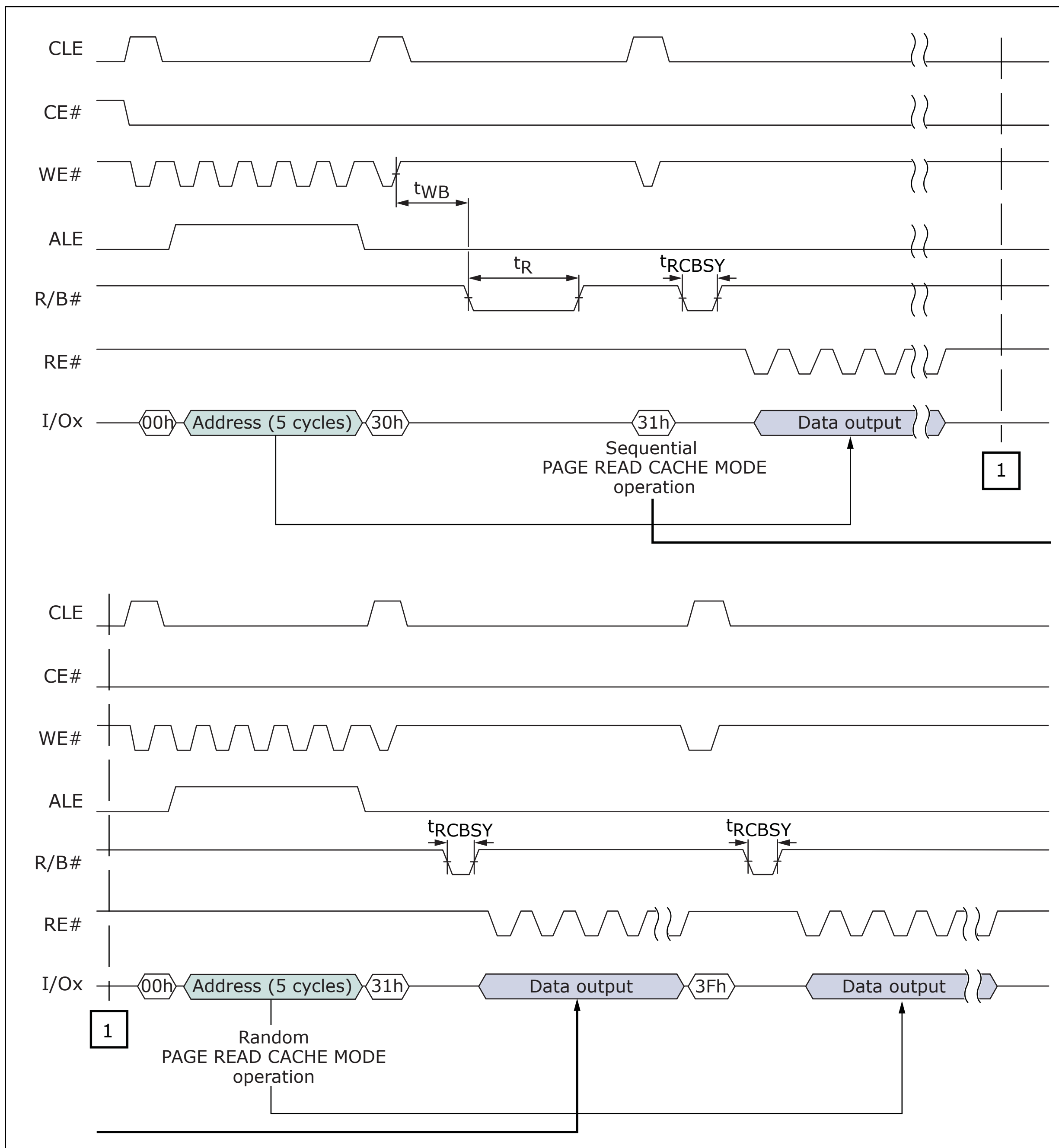
the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the device.

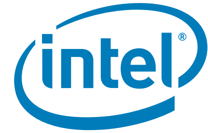
7.7.5 READ CACHE END 3Fh

The READ CACHE END (3Fh) command copies a page from the data register to the cache register without beginning a new READ CACHE mode operation. To issue the READ CACHE END command, write 3Fh to the command register.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and status register bits 6 and 5 = 11 to indicate that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the device.

Figure 30. READ CACHE Mode Operations





7.8 Program Commands

7.8.1 PAGE PROGRAM 80h-10h

Intel NAND Flash devices are inherently page-programmed devices. Pages must be programmed consecutively within a block, the from the least significant page address to the most significant page address (i.e., 0, 1, 2, ...255). Random page address programming is prohibited.

This Intel NAND Flash device does not support partial-page programming operations.

If a RESET (FFh) command is issued during a PAGE PROGRAM operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

7.8.1.1 SERIAL DATA INPUT 80h

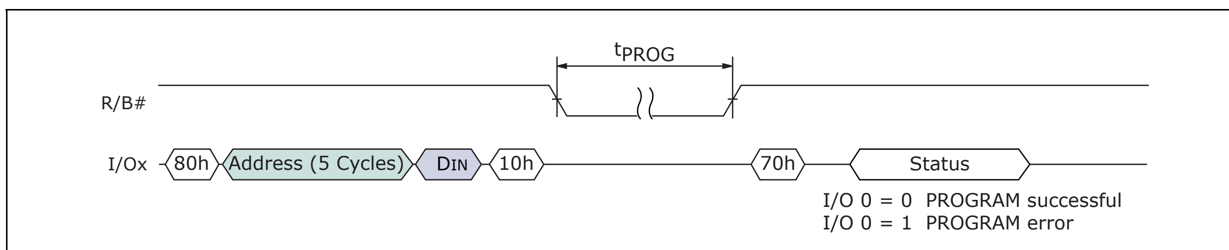
PAGE PROGRAM operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by five ADDRESS cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address.

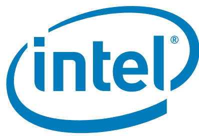
7.8.1.2 PROGRAM 10h

The PROGRAM (10h) command is written after the data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of array programming time, ^{t}PROG. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the programming operation. Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the program operation passed or failed (see figure below). The command register stays in read status register mode until another valid command is written to it.

Figure 31. PROGRAM and READ STATUS Operation





7.8.2 PAGE CACHE PROGRAM 80h-15h

Cache programming is actually a buffered programming mode of the standard PAGE PROGRAM command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by five cycles of address, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE WRITE (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array.

CHANGE WRITE COLUMN commands are allowed during PAGE CACHE PROGRAM operations.

Bit 6 (Cache R/B#) of the status register can be read by issuing the READ STATUS (70h) and READ STATUS ENHANCED (78h) command to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6.

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

If just the R/B# pin is used to determine programming completion, the last page of the program sequence must use the PAGE PROGRAM (80h-10h) command instead of the PAGE CACHE PROGRAM (80h-15h) command. If the PAGE CACHE PROGRAM (80h-15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete (see Figure 32).

Bit 1of the status register returns the pass/fail for the previous page when bit 6 of the status register is a “1” (ready state). The pass/fail status of the current program operation is returned with bit 0 of the status register when bit 5 of the status register is a “1” (ready state) (see Figure 32.)

If a RESET (FFh) command is issued during a PAGE CACHE PROGRAM operation while R/B# or bit 5 or bit 6 of the status register is LOW, the data in the shared memory cells being programmed will become invalid. Interruption of a program operation on one page could corrupt the data in another page within the block being programmed.

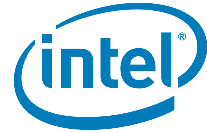
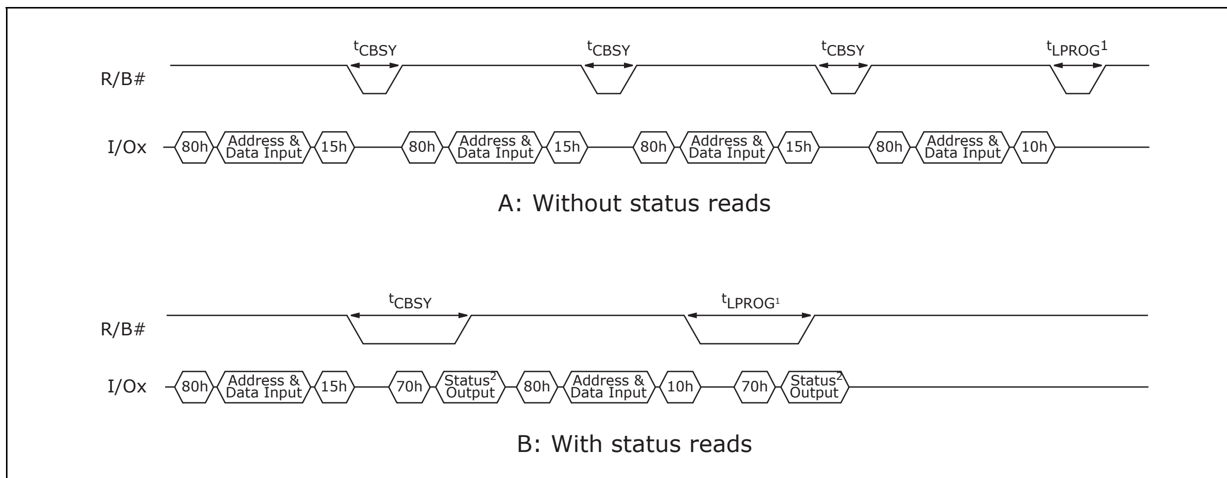


Figure 32. PAGE CACHE PROGRAM Example



Notes:
1. Command can be 70h or 78h.
2. Check I/O[6:5] for internal ready/busy. Check I/O[1:0] for pass fail. RE# can stay LOW or pulse multiple times after a 70h or 78h command.

7.9 Erase Commands

7.9.1 BLOCK ERASE 60h-D0h

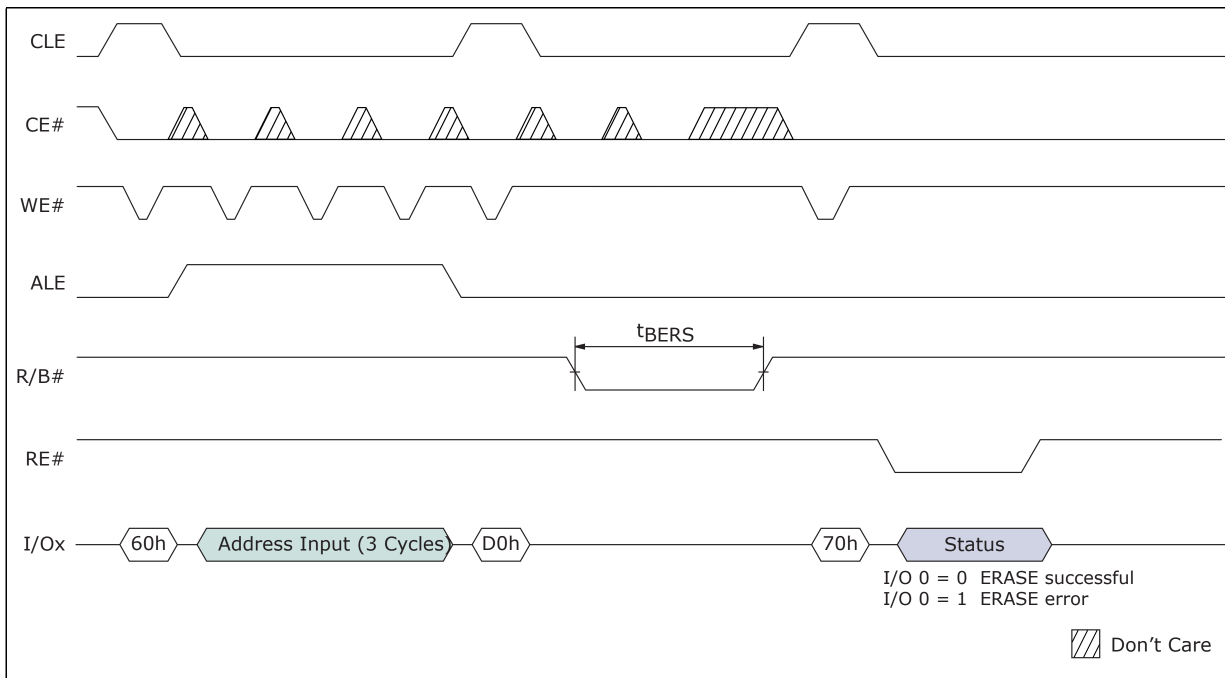
Erasing occurs at the block level. For example, the JS29F32G08AAMDB device has 4,096 erase blocks, organized into 256 pages per block, 4,320 bytes per page (4,096 + 224 bytes). Each block is 1,080 K bytes (1,024K + 56K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 33).

The last three cycles of addresses of the five-cycle addressing sequence are required for a BLOCK ERASE operation. The first two cycles must not be used. Although the page addresses are loaded, they are a “Don’t Care” and are ignored for BLOCK ERASE operations. See Figure 8, “Memory Map (x8)” on page 13 for addressing details.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then three cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS (70h) command can be used to check the status of the error. When bit 6 = “1” the ERASE operation is complete. Bit 0 indicates a pass/fail condition where “0” = pass (see Figure 33, and Table 15 on page 38).

Figure 33. BLOCK ERASE Operation



7.10 Copyback Commands

An internal data move requires two command sequences. Issue a COPYBACK READ (00h-35h) command first, then the COPYBACK PROGRAM (85h-10h) command. Data moves are only supported within the plane from which data is read.

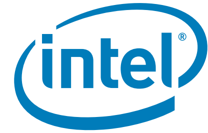
7.10.1 COPYBACK READ 00h-35h

The COPYBACK READ (00h-35h) command is used in conjunction with the COPYBACK PROGRAM (85h-10h) command. First, 00h is written to the command register, then the internal source address is written (five cycles). After the address is input, the COPYBACK READ (35h) command writes to the command register. This transfers a page from memory into the cache register.

All five address cycles are required when a COPYBACK READ command is issued.

After a COPYBACK READ (00h-35h) command is issued and R/B# returns HIGH, signifying operation completion, the data transferred from the source page into the cache register may be read out by toggling RE#. Data is output sequentially from the column address originally specified with the COPYBACK READ (00h-35h) command. CHANGE READ COLUMN (05h-E0h) commands can be issued without limit after the COPYBACK READ command.

The memory device is now ready to accept the COPYBACK PROGRAM command. Please refer to the description of this command in the following section.



7.10.2 COPYBACK PROGRAM 85h-10h

After the COPYBACK READ (00h-35h) command has been issued and R/B# goes HIGH, the COPYBACK PROGRAM (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register and programming of the new destination page begins. The sequence: 85h, destination address (five cycles), then 10h, is written to the device. After 10h is written, R/B# goes LOW while the control logic automatically programs the new page. The READ STATUS command and bit 6 of the status register can be used instead of the R/B# line to determine when the write is complete. Bit 0 of the status register indicates if the operation was successful.

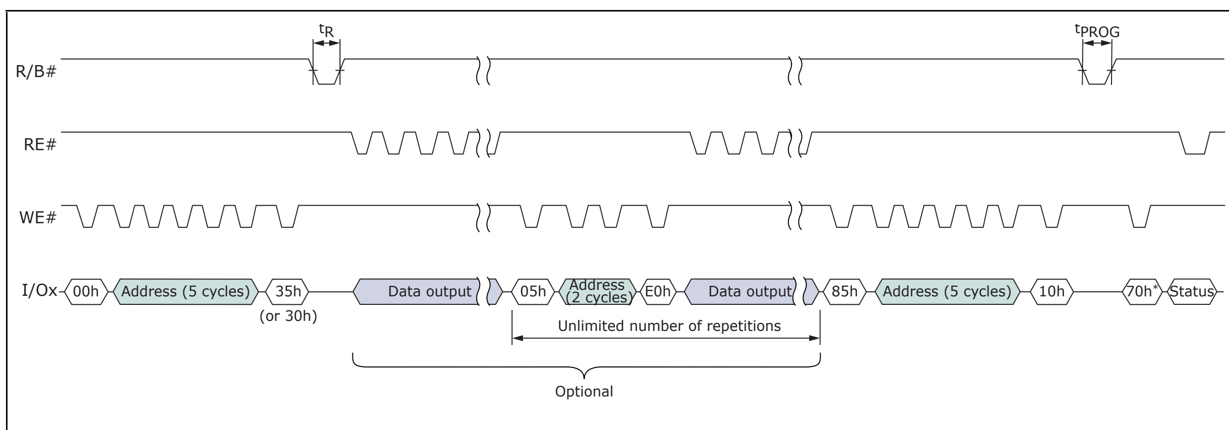
The CHANGE WRITE COLUMN (85h) command can be used during the COPYBACK PROGRAM command sequence to modify a word or multiple words of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the CHANGE WRITE COLUMN (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data is transferred to the data register, and programming of the new page is started. The CHANGE WRITE COLUMN command can be issued as many times as necessary before starting the programming sequence with 10h (see Figures 34 and 35).

Because COPYBACK operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple COPYBACK operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using COPYBACK operations also use a robust ECC scheme that exceeds the minimum required ECC.

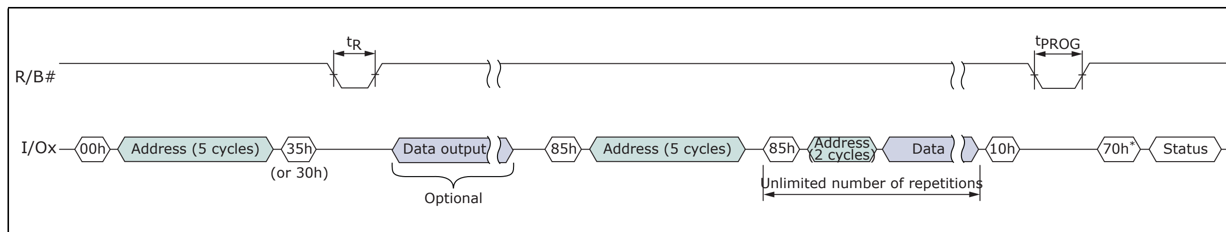
If a RESET (FFh) command is issued during a COPYBACK PROGRAM (85h-10h) operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

Figure 34. COPYBACK Operations



Note: Command can be 70h or 78h.

Figure 35. COPYBACK READ with Optional Data Output and COPYBACK PROGRAM



Notes:
1. Command can be 70h or 78h
2. This waveform only shows two address cycles, but 85h also supports five address cycles.

7.11 Multi-Plane Operations

This NAND Flash device is divided into two physical planes. Each plane contains a 4,320-byte data register, a 4,320-byte cache register, and a 2,048-block Flash array. Multi-plane commands make better use of the flash arrays on these physical planes by performing PROGRAM, READ, or ERASE operations simultaneously, significantly improving system performance.

Multi-plane commands require two addresses, one address per plane. These two addresses are subject to the following requirements:

- The least significant block address bit, BA8, must be different for both addresses.
- The page address bits, PA[7:0], must be identical for both addresses.

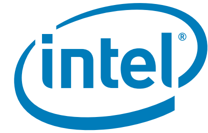
7.11.1 READ MULTI-PLANE 00h-32h-00h-30h

The READ MULTI-PLANE (00h-32h-00h-30h) operation is similar to the READ (00h-30h) operation. It transfers two pages of data from the Flash array to the data registers. Each page must be from a different plane on the same die.

To enter the READ MULTI-PLANE mode, write the 00h command to the command register, then write five ADDRESS cycles for plane 0 (BA8 = “0”). Next, write the 00h command to the command register, then write five ADDRESS cycles for plane 1 (BA8 = “1”). Finally, issue the 30h command. The first plane and second plane addresses must meet the multi-plane addressing requirements, and, in addition, they must have identical column addresses.

After the 30h command is written, page data is transferred from both planes to their respective data registers in ^{t}R. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# returns HIGH. To read out the data from the plane 0 data register, pulse RE# repeatedly. After the data cycle from the plane 0 address completes, issue a SELECT CACHE REGISTER (06h-E0h) command to select the plane 1 address, then repeatedly pulse RE# to read out the data from the plane 1 data register.

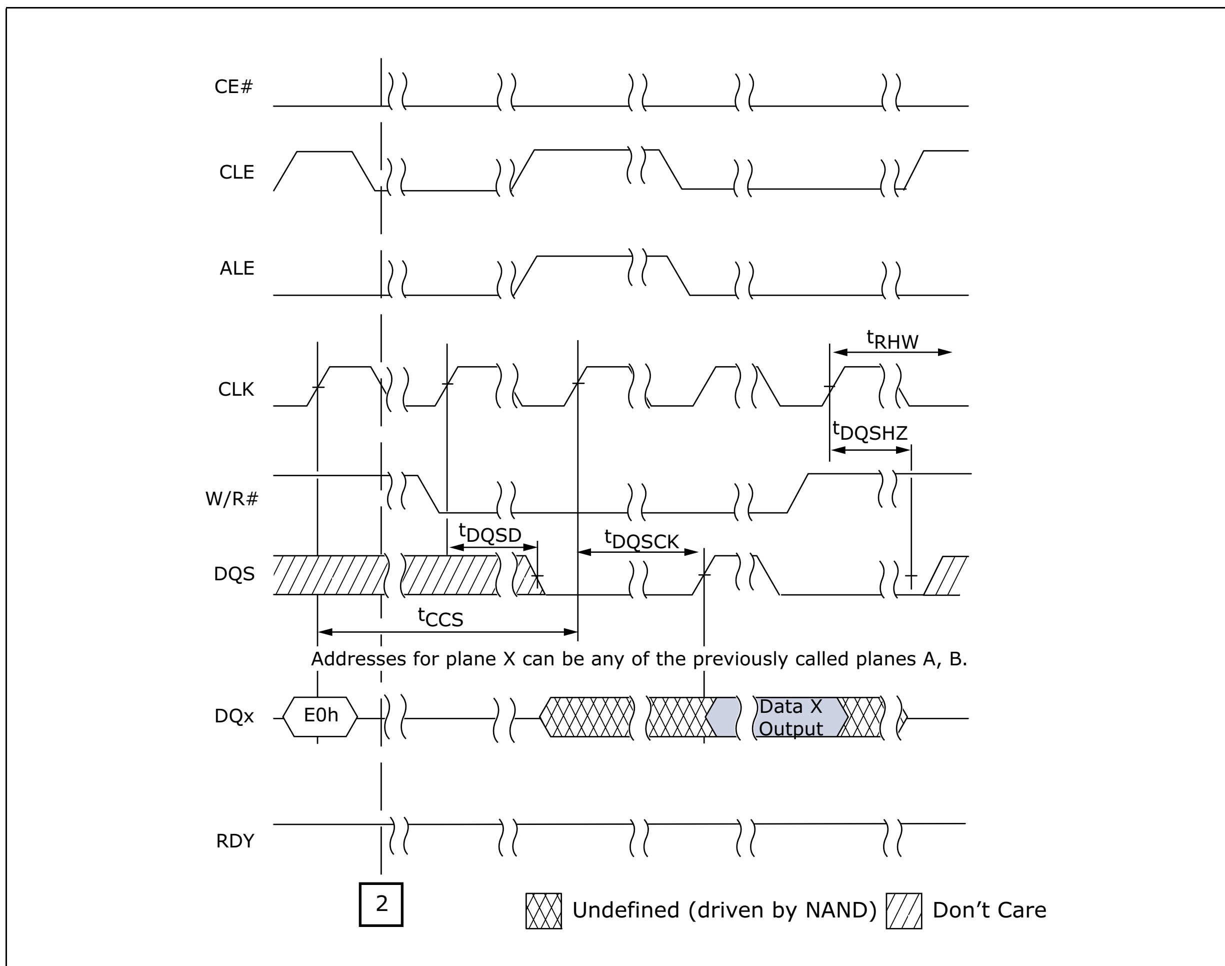
Alternately, the READ STATUS (70h) command can monitor the data transfers. When the data cycle is complete, status register bit 6 is set to “1.” To read data from one of the two planes, the user must first issue the SELECT CACHE REGISTER (06h-E0h) command and pulse RE# repeatedly. When the data cycle is complete, issue a SELECT CACHE REGISTER (06h-E0h) command to select the other plane. To output the data beginning at the specified column address, pulse RE# repeatedly.



Use of the READ STATUS ENHANCED (78h) command is supported during and following a READ MULTI-PLANE operation.

Figure 36. READ MULTI-PLANE 1 of 2

Figure 37. READ MULTI-PLANE 2 of 2



7.11.2 SELECT CACHE REGISTER 06h-E0h

The SELECT CACHE REGISTER (06h-E0h) command selects a plane and column address from which to read data after a READ MULTI-PLANE (00h-00h-30h) command.

To issue a SELECT CACHE REGISTER command, issue the 06h command, then five ADDRESS cycles, and follow with the E0h command. Pulse RE# repeatedly to read data from the new plane beginning at the specified column address.

The primary purpose of the SELECT CACHE REGISTER command is to select a new plane and column address within that plane. If a new plane does not need to be selected, then it is possible to use the CHANGE READ COLUMN (05h-E0h) command instead. For details, see page 38.

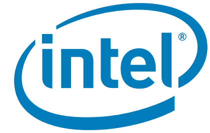
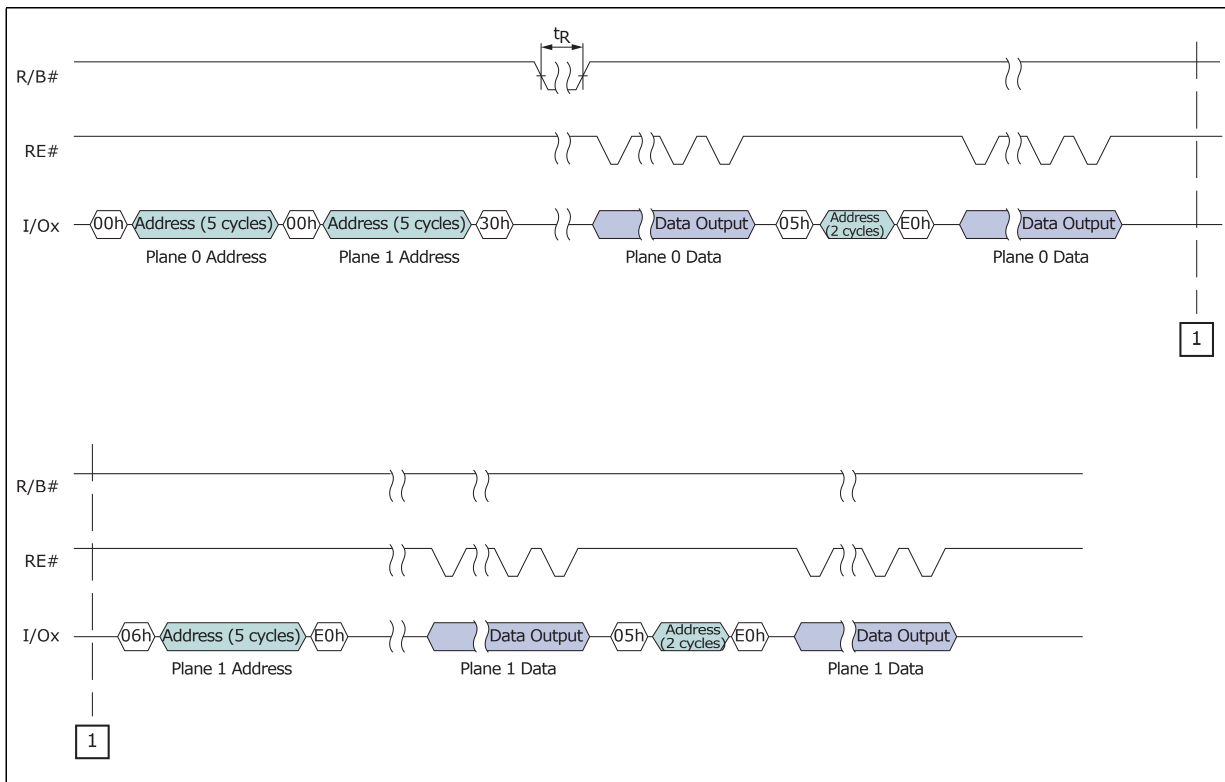


Figure 38. READ MULTI-PLANE

Notes:

1. Column and page addresses must be the same.
2. The least-significant block address bit, BA8, must not be the same for the first and second plane addresses.

Figure 39. READ MULTI-PLANE with SELECT CACHE REGISTER



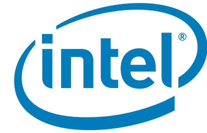
7.11.3 READ STATUS ENHANCED 78h

In Intel NAND Flash devices that have two planes and possible more than one die in a package that share the same CE# pin, it is possible to independently poll the status register of a particular plane and die using the READ STATUS ENHANCED (78h) command. This feature operates regardless of device size, organization, or status. This command can be used to check the status during and after multi-plane operations, and also to check the status of PROGRAM and ERASE operations interleaved between two die sharing the same CE# pin.

After the 78h command is issued, the device requires three ADDRESS cycles containing the block and page addresses, BA[19:8] and PA[7:0]. The most significant block address bit in the third ADDRESS cycle, BA20, selects the proper die, and the least significant block address bit in the first ADDRESS cycle, BA8, selects the proper plane within that die.

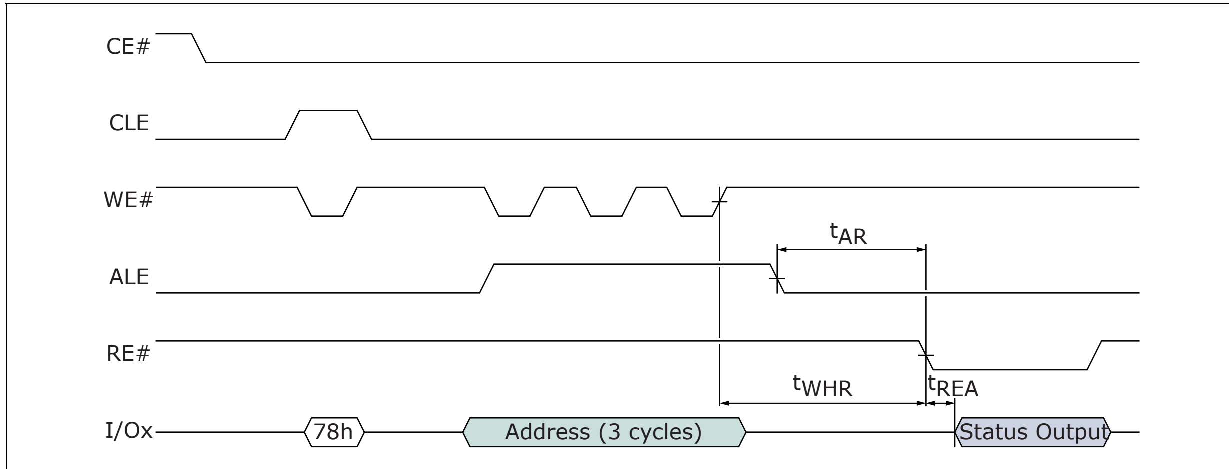
After the 78h command and the three ADDRESS cycles, the status register is output on I/O[7:0] when RE# is LOW. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to issue a new READ STATUS command to see these changes. The status register bit definitions are identical to those reported by the READ STATUS command (see Table 15 on page 38).

In devices that have more than one die sharing a common CE# pin, when one die is not busy (status register bit 5 is “1”), it is possible to initiate a new operation to that die even if the other die is busy. Operations can overlap and occur concurrently on the two



die. Multiple-die operations are limited to PROGRAM and ERASE operations, like PAGE PROGRAM, BLOCK ERASE, PAGE PROGRAM MULTI-PLANE and BLOCK ERASE MULTI-PLANE.

Figure 40. READ STATUS ENHANCED Cycle



7.11.4 PAGE PROGRAM MULTI-PLANE 80h-11h-80h-10h

The PAGE PROGRAM MULT-PLANE (80h-11h-80h-10h) operation is similar to the PAGE PROGRAM (80h-10h) operation. It programs two pages of data from the data registers to the Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to most significant page address. Random page programming within a block is prohibited. The first plane address and the second plane address must meet the multi-plane addressing requirements (see Section 7.11, "Multi-Plane Operations" on page 50 for details).

To begin the PAGE PROGRAM MULTI-PLANE operation, write the 80h command to the command register; write five ADDRESS cycles for the first plane; then write the data. Serial data is loaded on consecutive WE# cycles starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h), READ STATUS ENHANCED (78h), and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register; write five ADDRESS cycles for the second plane; then write the data. The PROGRAM (10h) command is written after the second-plane data input is complete.

After the 10h command is written, the control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operations to both planes. WRITE verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of the array programming time (^{t}PROG). When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}PROG are READ STATUS (70h), READ STATUS ENHANCED (78h), and RESET (FFh).

If a RESET (FFh) command is issued during a PAGE PROGRAM MULT-PLANE (80h-11h-80h-10h) operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

When the device is ready, if the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = "1"), use the READ STATUS ENHANCED (78h) command twice—once for each plane—to determine which plane operation failed.

During serial data input for either plane, the CHANGE WRITE COLUMN (85h) command can be used any number of times to change the column address within that plane. Figure 41 shows PAGE PROGRAM MULTI-PLANE operation.

Figure 41. PAGE PROGRAM MULTI-PLANE

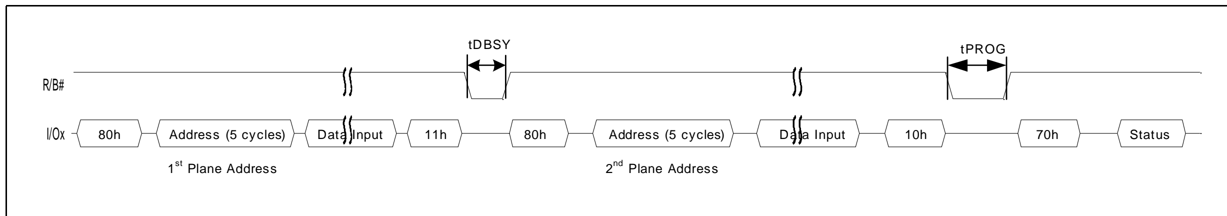
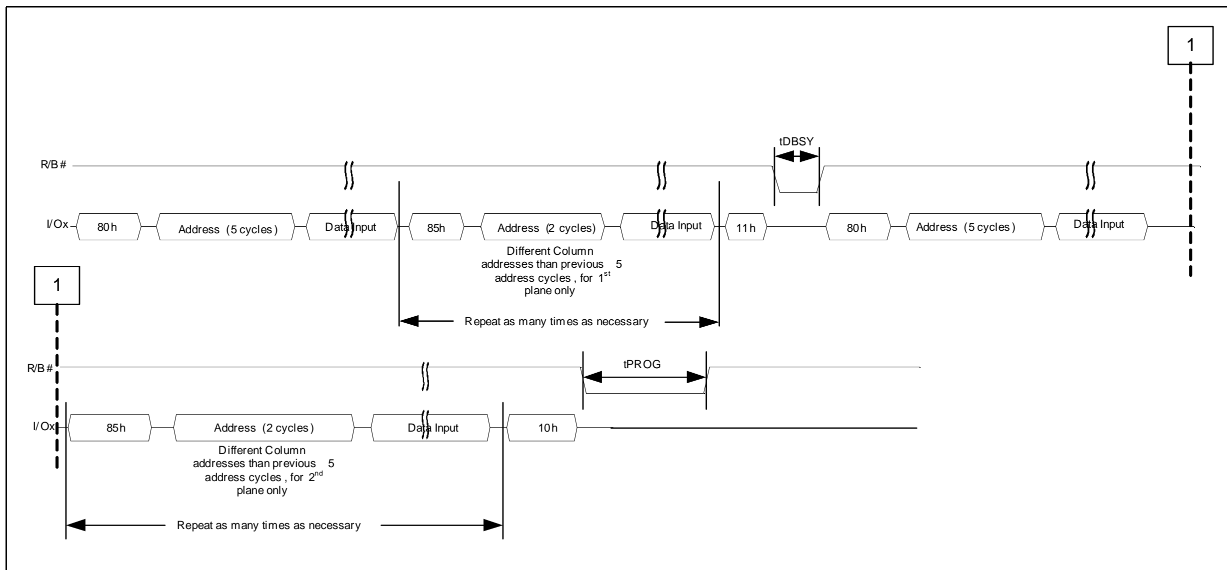
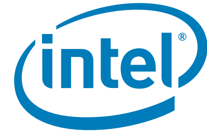


Figure 42. PAGE PROGRAM MULTI-PLANE with CHANGE WRITE COLUMN





7.11.5 PAGE CACHE PROGRAM MULTI-PLANE 80h-11h-80h-15h

The PAGE CACHE PROGRAM MULTI-PLANE (80h-11h-80h-15h) operation is similar to the PAGE CACHE PROGRAM (80h-15h) operation. It cache programs two pages of data from the data registers to the Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to the most significant page address. Random page programming within a block is prohibited. The first plane and second plane addresses must meet the multi-plane addressing requirements (see Section 7.11, "Multi-Plane Operations" on page 50).

To enter the PAGE CACHE PROGRAM MULTI-PLANE, write the 80h command to the command register, write five ADDRESS cycles for the first plane, then write the data. Serial data is loaded on consecutive WE# cycles starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h) READ STATUS ENHANCED (78h), and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register, write five ADDRESS cycles for the second plane, then write the data. The CACHE WRITE (15h) command is written after the second-plane data input is complete. Data is transferred from the cache registers to the data registers on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data registers and R/B# returns HIGH, memory array programming to both planes begins.

When R/B# returns HIGH, new data can be written to the cache registers by issuing another PAGE CACHE PROGRAM MULTI-PLANE (80h-11h-80h-15h) sequence. The time that R/B# stays LOW (^{t}CBSY) is determined by the actual programming time of the previous operation. For the first cache operation, the duration of ^{t}CBSY is the time it takes for the data to be copied from the cache registers to the data registers. On the second and subsequent PAGE CACHE PROGRAM MULTI-PLANE operations, transfer from the cache registers to the data registers is delayed until the current data registers' contents have been programmed into the arrays.

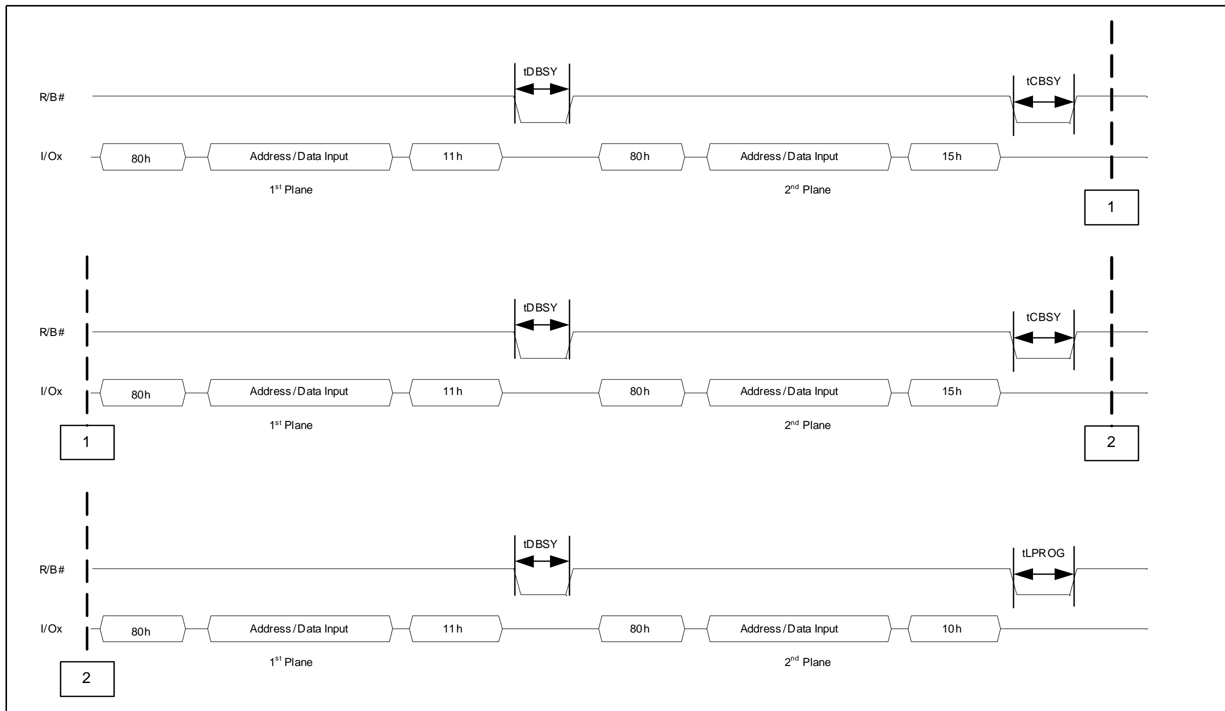
If the R/B# pin is used to determine programming completion, the last operation of the program sequence must use the PROGRAM PAGE MULTI-PLANE (80h-11h-80h-10h) command instead of the PAGE CACHE PROGRAM MULTI-PLANE (80h-11h-80h-15h) command. If the PAGE CACHE PROGRAM MULTI-PLANE (80h-11h-80h-15h) command is used for the last operation, then use READ STATUS (70h) to monitor the operation's progress; status register bit 5 indicates when programming is complete. See Table 7 on page 22 for details of the status register.

To determine when the current PAGE CACHE PROGRAM MULTI-PLANE (80h-11h-80h-15h) operation has completed, issue the READ STATUS (70h) command and check status register bits 5 and 6. When the device is ready, use status register bit 0 to determine if the current operation passed and status register bit 1 to determine if the previous operation passed. If either bit 0 or bit 1 = "1," indicating a failed operation, then use the READ STATUS Enhanced (78h) command twice—once for each plane—to determine which current or previous plane operation failed. For more information on status register bit definitions, see Table 15 on page 38.

During the serial data input for either plane, the CHANGE WRITE COLUMN (85h) command may be used any number of times to change the column address within that plane.

If a RESET (FFh) command is issued during a PAGE CACHE PROGRAM MULTI-PLANE operation while R/B# is LOW or bit 5 or bit 6 of the status register is LOW, the data in the shared memory cells being programmed will become invalid. Interruption of a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.

Figure 43. PAGE CACHE PROGRAM MULTI-PLANE

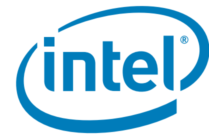


7.11.6 COPYBACK MULTI-PLANE Operations

A COPYBACK MULTI-PLANE operation is similar to a COPYBACK operation, and requires two sequences. Issue a COPYBACK READ MULTI-PLANE (00h-00h-35h) command first, then the COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) command. Data moves are only supported within the planes from which data is read. The first plane and second plane addresses must meet the multi-plane addressing requirements for both the COPYBACK READ MULTI-PLANE (00h-00h-35h) and COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) commands (see Section 7.11, “Multi-Plane Operations” on page 50).

7.11.6.1 COPYBACK READ MULTI-PLANE 00h-00h-35h

The COPYBACK READ MULTI-PLANE (00h-00h-35h) command is used in conjunction with the COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) command. First, write 00h to the command register, then write the first plane internal source address (five cycles). Again, write 00h to the command register, followed by the second-plane



internal source address (five cycles). Finally, write 35h to the command register. After the 35h command, R/B# goes LOW for ^{t}R while two pages are read into their respective cache registers.

After a COPYBACK READ MULTI-PLANE (00h-00h-35h) command is issued, the data transferred from the source pages into the cache registers may be read out by toggling RE#. Data is output sequentially from the column address originally specified by the COPYBACK READ MULTI-PLANE (00h-00h-35h) command, starting with plane 0.

A SELECT CACHE REGISTER (06h-E0h) command can be used to select the data transferred from the source pages of each plane. This command will change the starting column address on only the plane being selected. The column address on the plane moved from will remain unchanged from its previous location.

To read out data after the COPYBACK READ MULTI-PLANE command, either SELECT CACHE REGISTER (06h-E0h) commands without limit or a combination of READ STATUS ENHANCED (78) and CHANGE READ COLUMN (05h-E0h) commands can be issued.

The memory device is now ready to accept the COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) command.

Alternatively, two COPYBACK READ (00h-35h) commands may be issued, each addressing different planes on the same die, prior to issuing the COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) command.

Alternatively, a READ MULTI-PLANE (00h-00h-30h) command may be issued, prior to issuing the COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) command.

7.11.6.2 COPYBACK PROGRAM MULTI-PLANE 85h-11h-85h-10h

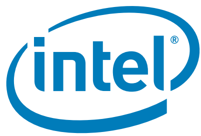
After the COPYBACK READ MULTI-PLANE (00h-00h-35h) command has been issued and R/B# goes HIGH (or the status register bit 6 is "1"), the COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) command is used. Pages must be read from and programmed to the same plane.

First, write 85h to the command register, then write the first plane destination address (five cycles), then write 11h to the command register. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h), READ STATUS ENHANCED (78h), and RESET (FFh).

After ^{t}DBSY, write the 85h command to the command register, then write the second plane destination address (five cycles), then write 10h to the command register. Data is transferred from the cache registers to the data registers on the rising edge of WE#, and programming begins on both planes.

R/B# goes LOW for the duration of array programming time, ^{t}PROG. When programming and verification is complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}PROG are READ STATUS (70h), READ STATUS ENHANCED (78h), and RESET (FFh).

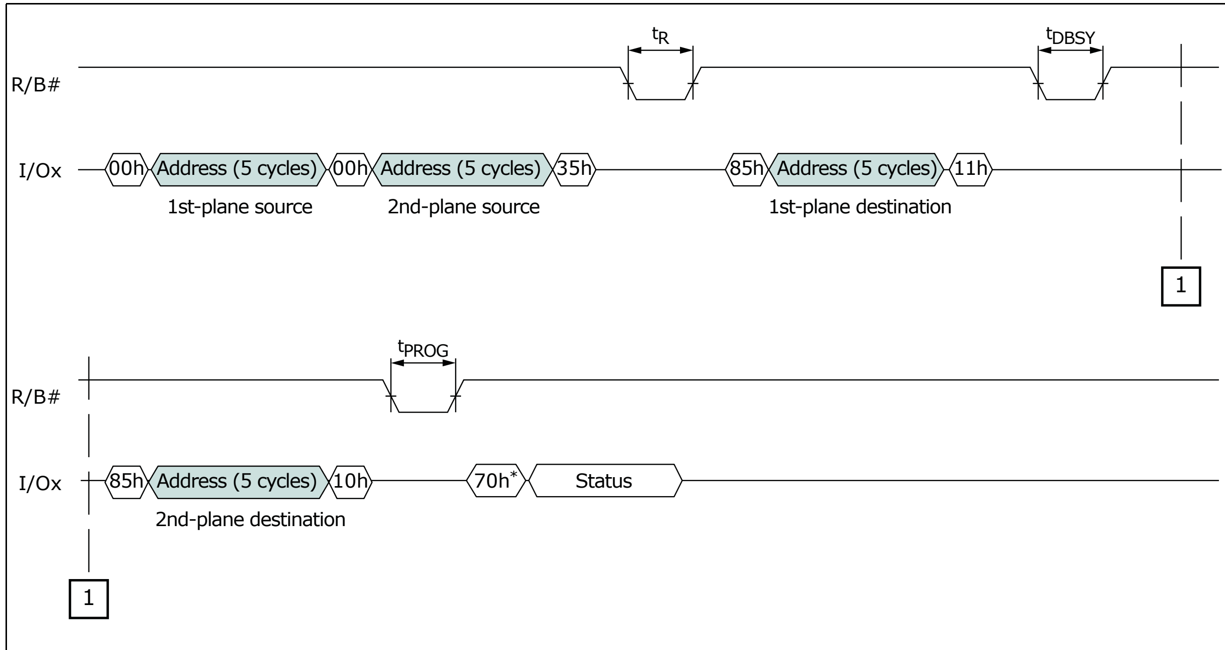
If a RESET (FFh) command is issued during a COPYBACK PROGRAM MULTI-PLANE (85h-11h-85h-10h) operation while R/B# is LOW, the data in the shared-memory cells being programmed becomes invalid. Interrupting a PROGRAM operation on one page could corrupt the data in another page within the block being programmed.



If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = “1”), use the READ STATUS ENHANCED (78h) command twice—once for each plane—to determine which plane operation failed.

During the serial data input for either plane, the CHANGE WRITE COLUMN (85h) command may be used any number of times to change the column address within that plane. See Figure 46, “COPYBACK READ MULTI-PLANE with CHANGE WRITE COLUMN” on page 62 for an example.

Figure 44. COPYBACK READ MULTI-PLANE Operations



Note: Command can be 70h or 78h.

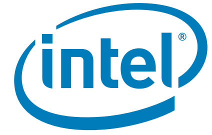


Figure 45. COPYBACK READ MULTI-PLANE with SELECT CACHE REGISTER

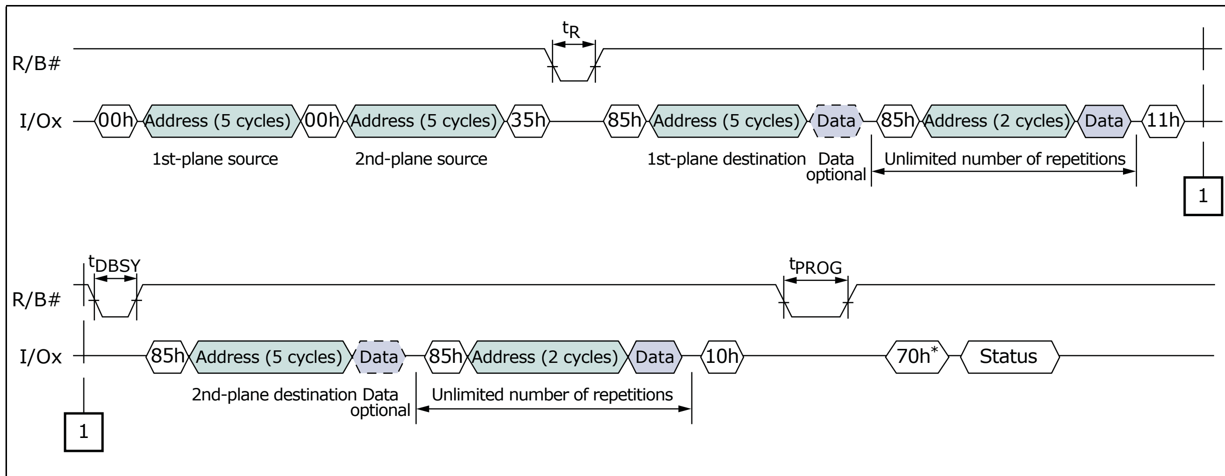
R/B#
tR
RE#
I/Ox
00h Address (5 cycles) 00h Address (5 cycles) 35h Data output 06h Address (5 cycles) E0h
1st-plane source
2nd-plane source (or 30h)
Data from 1st-plane source
2nd-plane source address
1

R/B#
RE#
I/Ox
1
Data output 05h Address (2 cycles) E0h Data output
Data from 2nd-plane source
2nd-plane source column address
Data from 2nd-plane source from new column address
Optional
2

R/B#
tDBSY
tPROG
RE#
I/Ox
85h Address (5 cycles) 11h 85h Address (5 cycles) 10h 70h* Status
2
1st-plane destination
2nd-plane destination

Note: Command can be 70h or 78h.

Figure 46. COPYBACK READ MULTI-PLANE with CHANGE WRITE COLUMN



Note: Command can be 70h or 78h.

7.11.7 BLOCK ERASE MULTI-PLANE 60h-D1h-60h-D0h

The BLOCK ERASE MULTI-PLANE (60h-D1h-60h-D0h) operation is similar to the BLOCK ERASE (60h-D0h) operation. It erases two blocks instead of one. The blocks to be erased must be on different planes on the same die. The first plane and second plane addresses must meet the multi-plane addressing requirements (see Section 7.11, "Multi-Plane Operations" on page 50).

Begin a BLOCK ERASE MULTI-PLANE operation by writing 60h to the command register, followed by three ADDRESS cycles of the first plane block address. Next, write the D1h command. The D1h command is a "dummy" command. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when the status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h), READ STAUS ENHANCED (78h), and RESET (FFh).

After ^{t}DBSY, write the 60h command to the command register followed by three address cycles for the second plane. Finally, issue the D0h command.

R/B# goes LOW for the duration of block erase time, ^{t}BERS. When block erasure is complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}BERS are READ STATUS (70h), READ STATUS ENHANCED (78h), and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 = "1"), then use the READ STATUS ENHANCED (78h) command twice—once for each plane—to determine which plane operation failed.

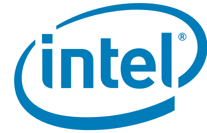
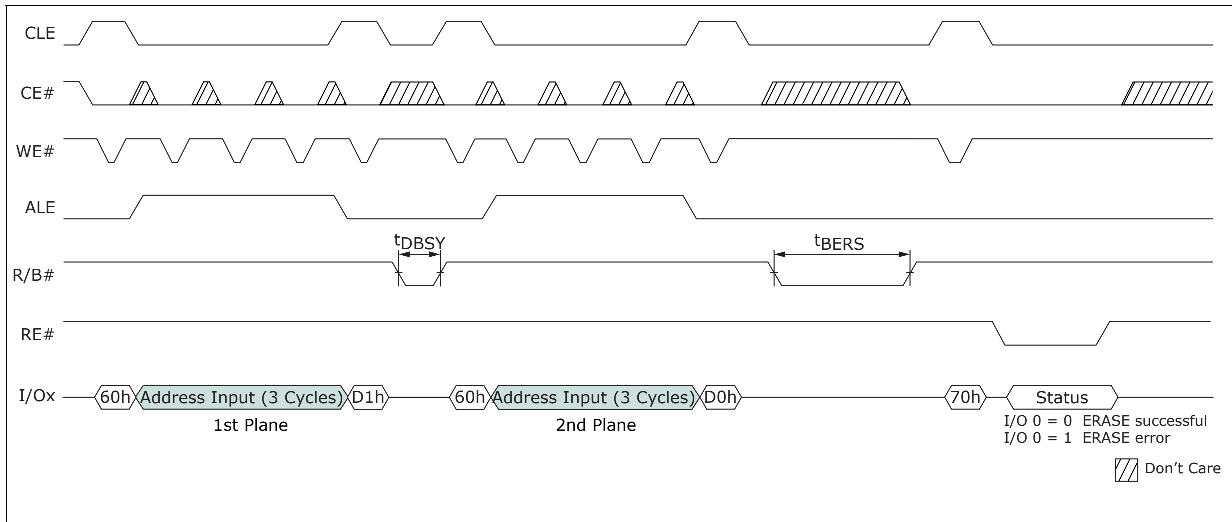


Figure 47. BLOCK ERASE MULTI-PLANE Operation



7.12 Interleaved Die Operations

In devices that have more than one die sharing a common CE# pin, it is possible to significantly improve performance by interleaving operations between the die. When both die are idle (R/B# is HIGH or status register bit 5 is "1"), issue a command to the first die. Then, while the first die is busy (R/B# is LOW), issue a command to the other die.

There are two methods to determine operation completion. The R/B# signal indicates when both die have finished their operations. R/B# remains LOW while either die is busy. When R/B# goes HIGH, then both die are idle and the operations are complete. Alternatively, the command can report the status of each die individually. If a die is performing a cache operation, like PAGE CACHE PROGRAM (80h-15h) or PAGE CACHE PROGRAM MULITI_PLANE (80h-11h-80h-15h), then the die is able to accept the data for another cache operation when status register bit 6 is "1." All operations, including cache operations, are complete on a die when status register bit 5 is "1."

During and following interleaved die operations, the commands prohibited. Instead, use the READ STATUS ENHANCED (78h) command to monitor status. These commands select which die will report status. Interleaved multi-plane commands must also meet the requirements in Section 7.11, "Multi-Plane Operations" on page 50.

READ, PAGE PROGRAM, PAGE CACHE PROGRAM, COPYBACK PROGRAM, PAGE PROGRAM MULTI-PLANE, PGE CACHE PROGRAM MULTI-PLANE, BLOCK ERASE and BLOCK ERASE MULTI-PLANE can be used in any combination as interleaved operations on separate die that share a common CE#.

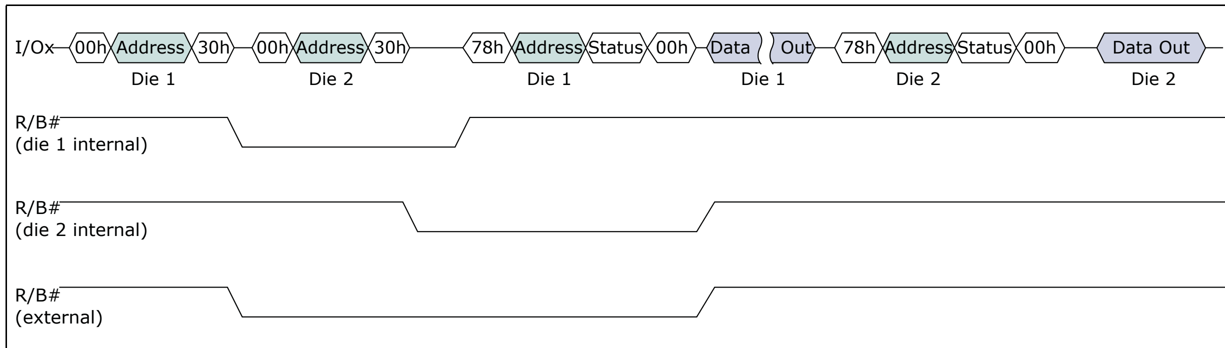
In interleaved PROGRAM and READ operations, the PROGRAM operation must be issued before the READ operation. The data from the READ operation must be read out before the next PROGRAM operation.

7.12.1 Interleaved READ Operations

Figure 48 on page 64 shows how to perform interleaved page read operations. In Figure 48, the status register is monitored for operation completion with the READ STATUS ENHANCED (78h) command. When the host has issued READ commands to multiple die at the same time, the host shall issue READ STATUS ENHANCED (78h) command before reading data from either die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h or SELECT CACHE REGISTER (06h-E0h) command, and thus avoiding bus contention. The host can use the SELECT CACHE REGISTER (06h-E0h) or READ STATUS ENHANCED (78h) commands to read out data from another die.

CHANGE READ COLUMN (05h-E0h) commands are permitted during interleaved page read operations.

Figure 48. Interleaved READ with Status Register Monitoring



7.12.2 Interleaved READ MULTI-PLANE Operation

Figure 49 on page 65 shows how to perform interleaved READ MULTI-PLANE operations using the READ STATUS ENHANCED (78h) command to monitor the status register for operation completion. When the host has issued READ MULTI-PLANE commands to multiple die at the same time, the host shall issue READ STATUS ENHANCED (78h) command before reading data from either die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h or SELECT CACHE REGISTER (06h-E0h) command, and thus avoiding bus contention.

The interleaved READ MULTI-PLANE operation must meet multi-plane addressing requirements. See Section 7.11, "Multi-Plane Operations" on page 50 for details.

CHANGE READ COLUMN (05h-E0h) is permitted during interleaved READ MULTI-PLANE operations to change the column address within a plane. SELECT CACHE REGISTER (06h-E0h) is permitted during interleaved READ MULTI-PLANE operations to change planes and column addresses between the planes.

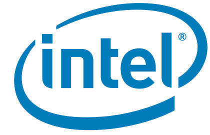


Figure 49. Interleaved READ MULTI-PLANE with Status Register Monitoring

I/Ox: 00h, Address (Die 1), 00h, Address (Die 1), 30h, 00h, Address (Die 2), 00h, Address (Die 2), 30h, 78h, Address, Status (Die 1)

R/B# (die 1 internal)

R/B# (die 2 internal)

R/B# (external)

1

I/Ox: 06h, Address, E0h (Die 1, Plane 0), Data output (Die 1, Plane 0), 06h, Address, E0h (Die 1, Plane 1), Data output (Die 1, Plane 1), 78h, Address, Status (Die 2)

R/B# (die 1 internal)

R/B# (die 2 internal)

R/B# (external)

1 2

I/Ox: 06h, Address, E0h (Die 2, Plane 0), Data output (Die 2, Plane 0), 06h, Address, E0h (Die 2, Plane 1), Data output (Die 2, Plane 1), 05h, Address, E0h (2 cycles), Data output (Die 2, Plane 1)

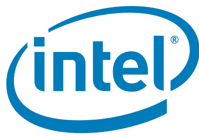
R/B# (die 1 internal)

R/B# (die 2 internal)

R/B# (external)

2

Note: Multi-plane addressing requirements apply.



7.12.3 Interleaved PAGE PROGRAM Operations

Figures 50 and 51 show how to perform two types of interleaved PAGE PROGRAM operations. In Figure 50, the R/B# signal is monitored for operation completion. In Figure 51, the status register is monitored for operation completion with the command.

CHANGE WRITE COLUMN (85h) is permitted during interleaved PAGE PROGRAM operations.

Figure 50. Interleaved PAGE PROGRAM with R/B# Monitoring

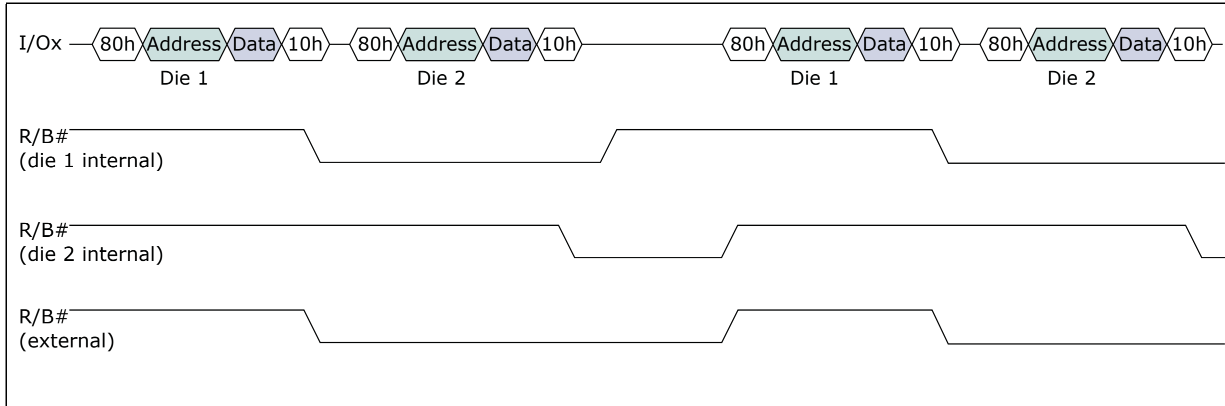
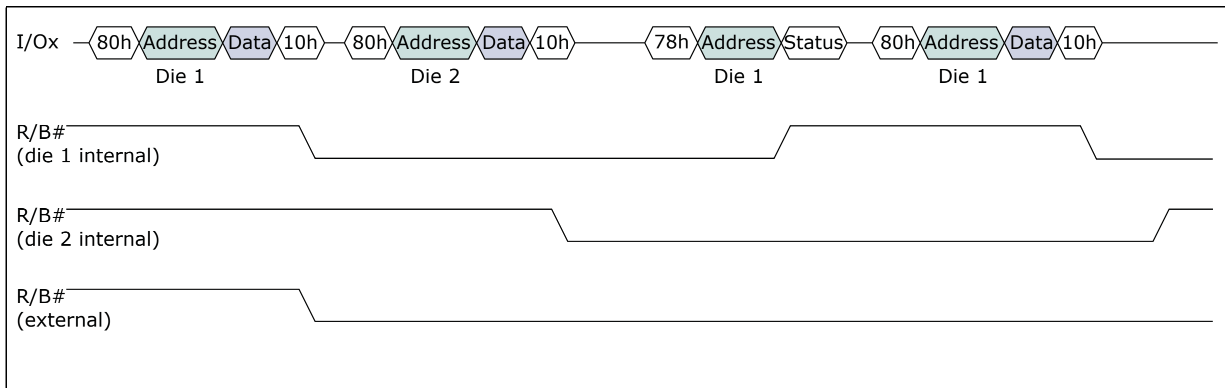


Figure 51. Interleaved PAGE PROGRAM with Status Register Monitoring



7.12.4 Interleaved PAGE CACHE PROGRAM Operations

Figures 52 and 53 show how to perform two types of interleaved PAGE CACHE PROGRAM operations. In Figure 52, the R/B# signal is monitored. In Figure 53, the status register is monitored with the READ STATUS ENHANCED (78h) command.

CHANGE WRITE COLUMN (85h) is permitted during interleaved PAGE CACHE PROGRAM operations.

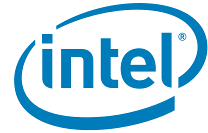


Figure 52. Interleaved PAGE CACHE PROGRAM with R/B# Monitoring

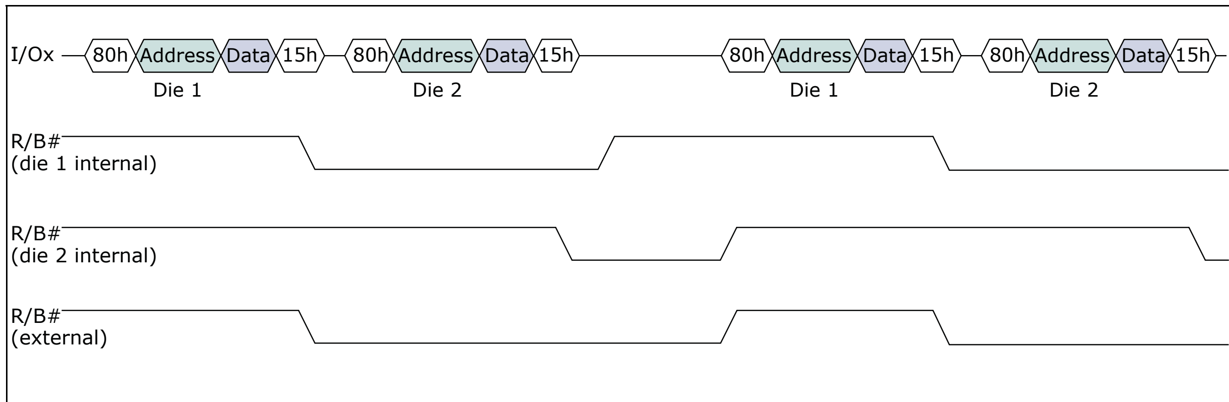
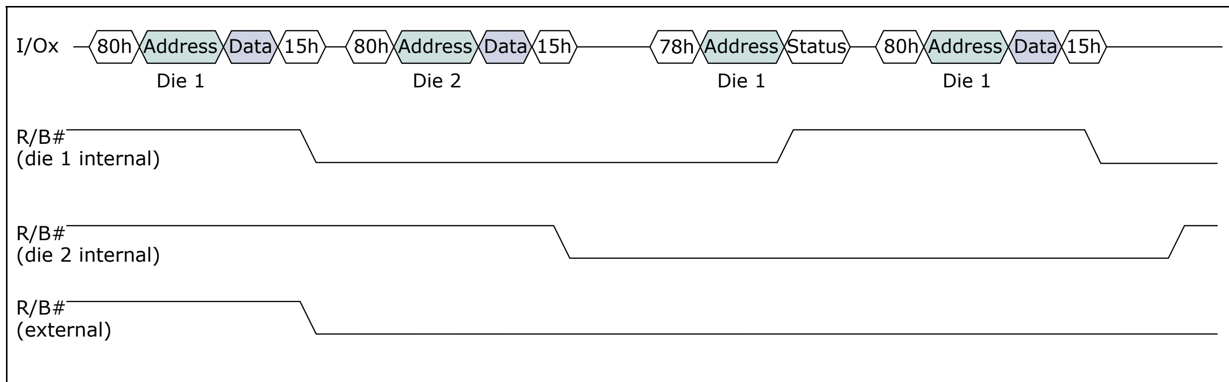


Figure 53. Interleaved PAGE CACHE PROGRAM with Status Register Monitoring



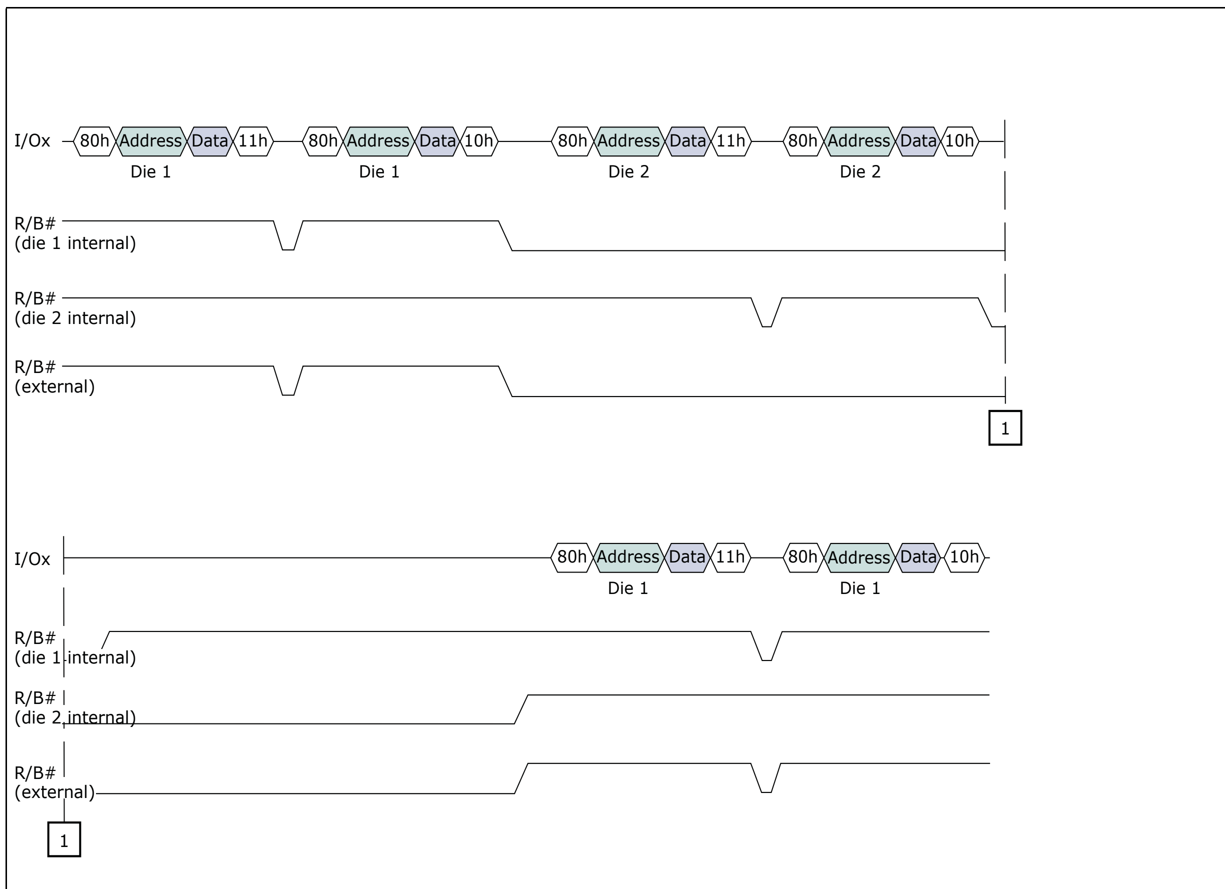
7.12.5 Interleaved PAGE PROGRAM MULTI-PLANE Operation

Figure 54 on page 68 and Figure 55 on page 69 show how to perform two types of interleaved PAGE PROGRAM MULTI-PLANE operations. In Figure 54, the R/B# signal is monitored for operation completion. In Figure 55, the READ STATUS ENHANCED (78h) command is used to monitor the status register for operation completion.

The interleaved PAGE PROGRAM MULTI-PLANE operation must meet multi-plane addressing requirements. See Section 7.11, "Multi-Plane Operations" on page 50 for details.

CHANGE WRITE COLUMN (85h) is permitted during interleaved PAGE PROGRAM MULTI-PLANE operations.

Figure 54. Interleaved PAGE PROGRAM MULTI-PLANE with R/B# Monitoring



Note: Multi-plane addressing requirements apply.

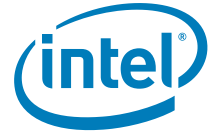
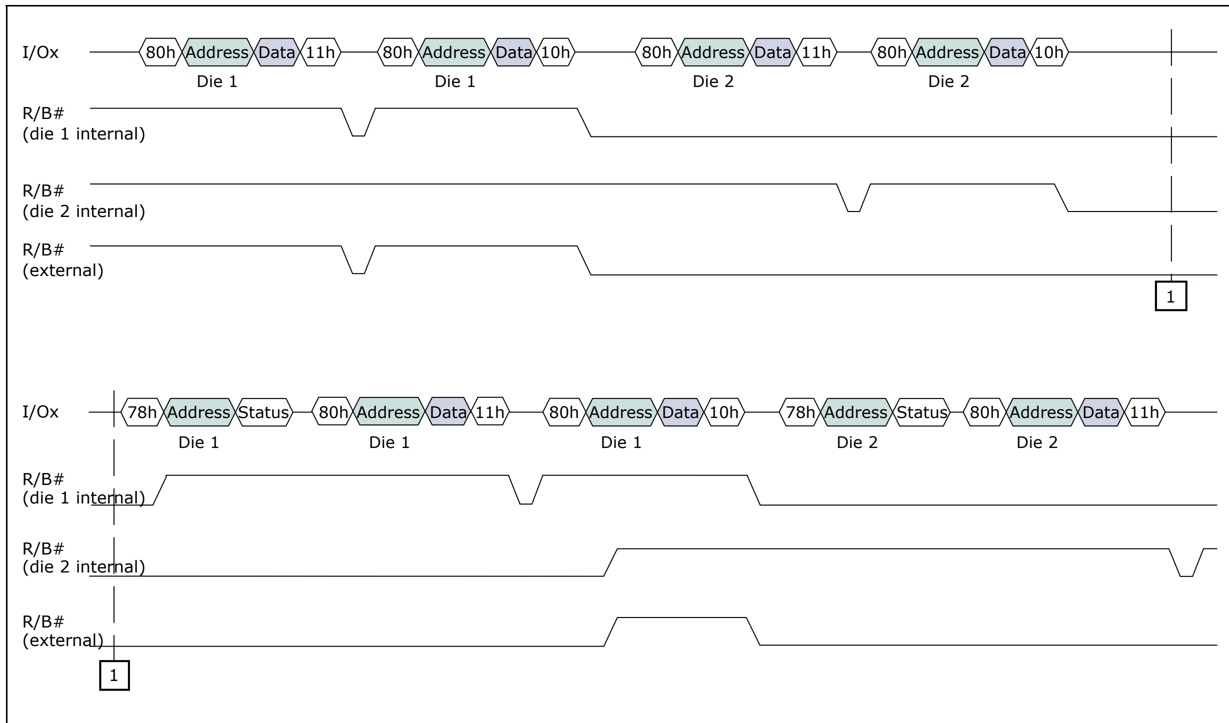


Figure 55. Interleaved PAGE PROGRAM MULTI-PLANE with Status Register Monitoring



Note: Multi-plane addressing requirements apply.

7.12.6 Interleaved PAGE CACHE PROGRAM MULTI-PLANE Operations

Figure 56 on page 70 and Figure 57 on page 71 show how to perform two types of interleaved PAGE CACHE PROGRAM MULTI-PLANE operations. In Figure 56, the R/B# signal is monitored. In Figure 57, the status register is monitored with the command.

The interleaved PAGE CACHE PROGRAM MULTI-PLANE operation must meet multi-plane addressing requirements. See Section 7.11, "Multi-Plane Operations" on page 50 for details.

CHANGE WRITE COLUMN (85h) is permitted during interleaved PAGE CACHE PROGRAM MULTI-PLANE operations.

A CHANGE WRITE COLUMN command will change the starting column address on only the plane and die currently being programmed. The column addresses from any other planes will remain unchanged from their previous locations.

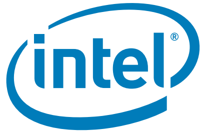
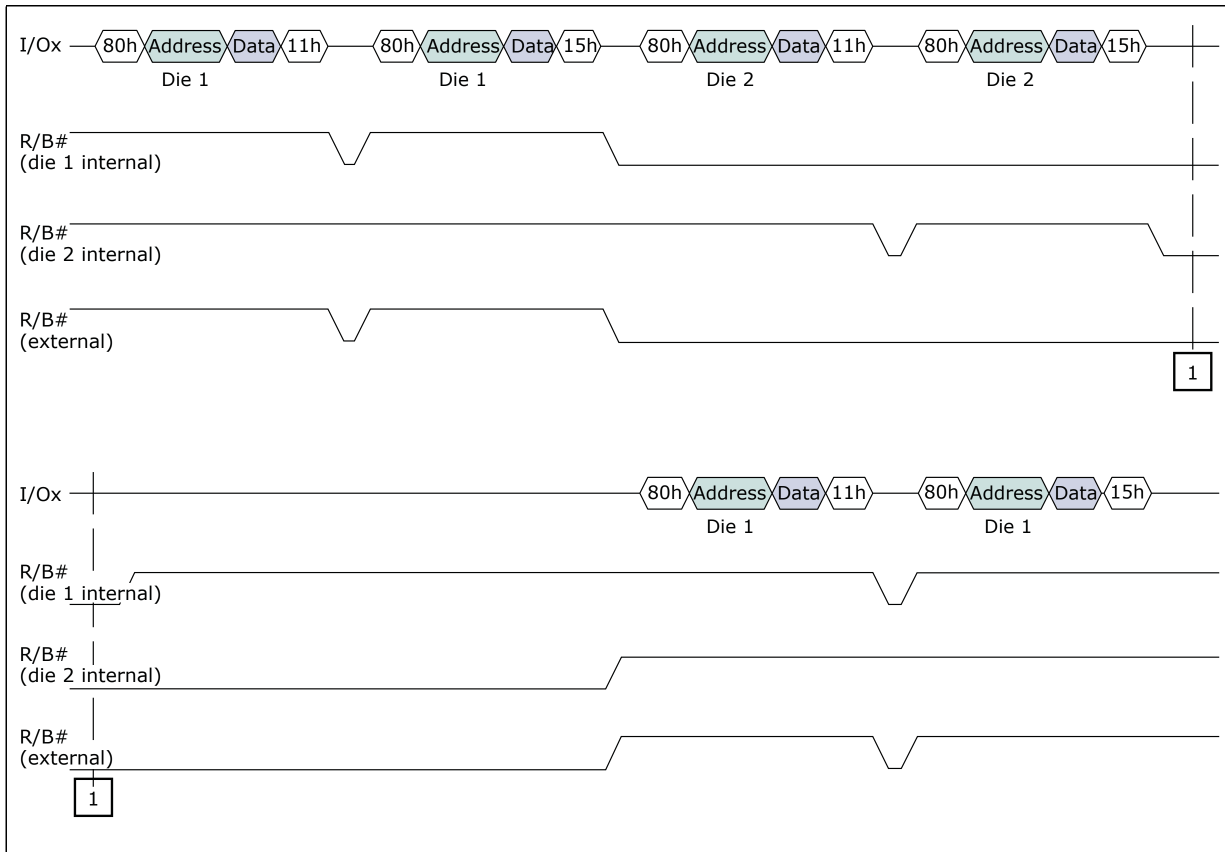


Figure 56. Interleaved PAGE CACHE PROGRAM MULTI-PLANE with R/B# Monitoring



Note: Multi-plane addressing requirements apply.

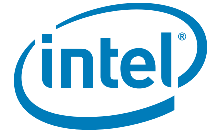
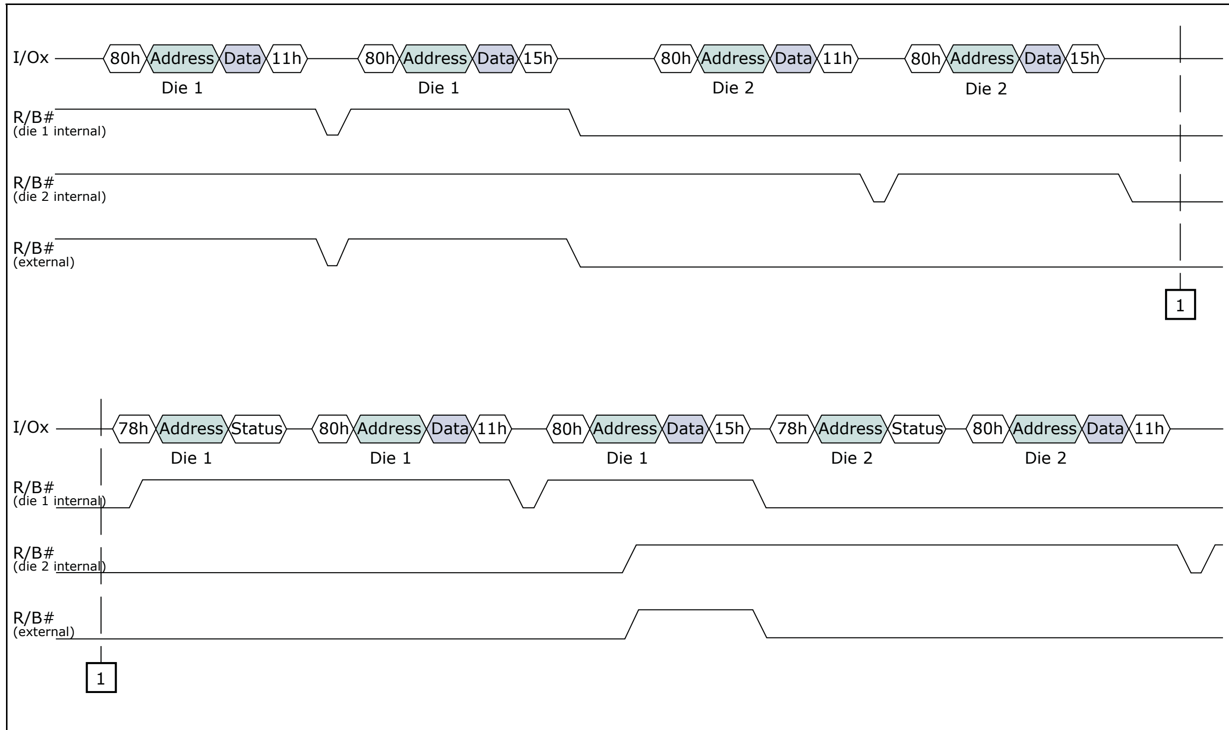


Figure 57. Interleaved PAGE CACHE PROGRAM MULTI-PLANE with Status Register Monitoring



Note: Multi-plane addressing requirements apply.

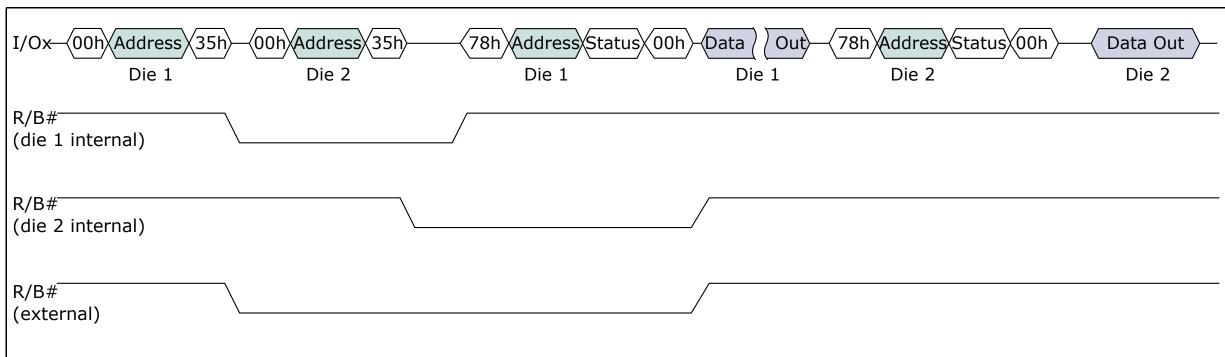
7.12.7 Interleaved COPYBACK READ Operations

Figure 58 on page 72 shows how to perform interleaved COPYBACK READ operations. In Figure 58, the status register is monitored for operation completion with the READ STATUS ENHANCED (78h) command. When the host has issued READ commands to multiple die at the same time, the host shall issue READ STATUS ENHANCED (78h) command before reading data from either die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h or SELECT CACHE REGISTER (06h-E0h) command, and thus avoiding bus contention.

The COPYBACK READ operations must operate within the same plane.

CHANGE READ COLUMN (05h-E0h) commands are permitted during interleaved COPYBACK READ operations.

Figure 58. Interleaved COPYBACK READ with Status Register Monitoring



7.12.8 Interleaved COPYBACK READ MULTI-PLANE Operations

Figure 59 on page 73 shows how to perform interleaved COPYBACK READ MULTI-PLANE operations. In Figure 59, the READ STATUS ENHANCED (78h) command is used to monitor the status register for operation completion. When the host has issued READ commands to multiple die at the same time, the host shall issue READ STATUS ENHANCED (78h) command before reading data from either die. This ensures that only the die selected by the 78h command responds to a data output cycle after being put in data output mode with a 00h or SELECT CACHE REGISTER (06h-E0h) command, and thus avoiding bus contention.

The interleaved COPYBACK READ MULTI-PLANE operation must meet multi-plane addressing requirements. See Section 7.11, "Multi-Plane Operations" on page 50 for details. The COPYBACK READ MULTI-PLANE operations must operate within the same plane.

CHANGE READ COLUMN (05h-E0h) is permitted during interleaved COPYBACK READ MULTI-PLANE operations to change the column address within a plane. SELECT CACHE REGISTER (06h-E0h) is permitted during interleaved COPYBACK READ MULTI-PLANE operations to change planes and column addresses between the planes.

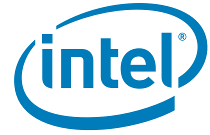


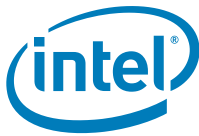
Figure 59. Interleaved COPYBACK READ MULTI-PLANE with Status Register Monitoring

I/Ox: 00h, Address (Die 1), 00h, Address (Die 1), 35h, 00h, Address (Die 2), 00h, Address (Die 2), 35h, 78h, Address, Status (Die 1)
R/B# (die 1 internal)
R/B# (die 2 internal)
R/B# (external)
1

I/Ox: 06h, Address, E0h (Die 1, Plane 0), Data output (Die 1, Plane 0), 06h, Address, E0h (Die 1, Plane 1), Data output (Die 1, Plane 1), 78h, Address, Status (Die 2)
R/B# (die 1 internal)
R/B# (die 2 internal)
R/B# (external)
1 2

I/Ox: 06h, Address, E0h (Die 2, Plane 0), Data output (Die 2, Plane 0), 06h, Address, E0h (Die 2, Plane 1), Data output (Die 2, Plane 1), 05h, Address, E0h (2 cycles), Data output (Die 2, Plane 1)
R/B# (die 1 internal)
R/B# (die 2 internal)
R/B# (external)
2

Note: Multi-plane addressing requirements apply.



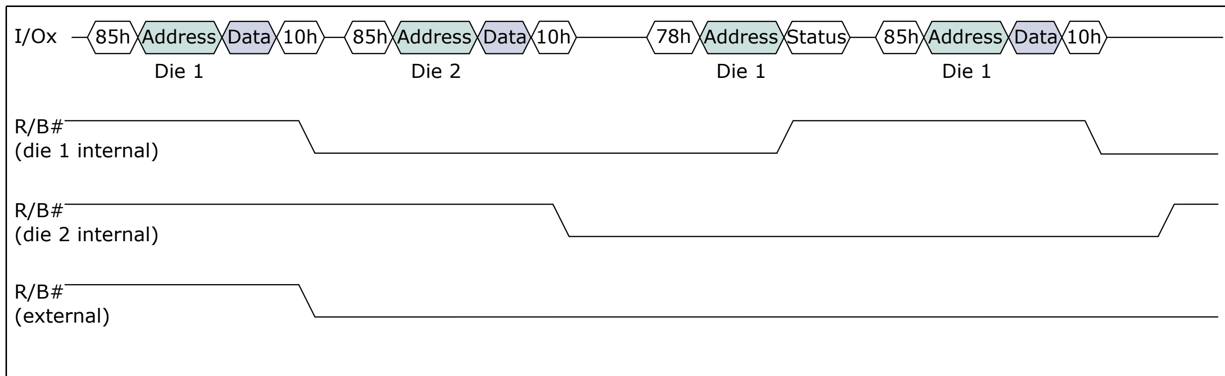
7.12.9 Interleaved COPYBACK PROGRAM Operations

Figure 60 shows how to perform interleaved COPYBACK PROGRAM operations. In Figure 60, the status register is monitored for operation completion with the READ STATUS ENHANCED (78h) command.

An interleaved COPYBACK READ operation is required before a COPYBACK PROGRAM operation can be started. See "Interleaved COPYBACK READ Operations" on page 71 for a description. The COPYBACK PROGRAM operations must operate within the same plane.

CHANGE WRITE COLUMN (85h) commands are permitted during interleaved COPYBACK PROGRAM operations.

Figure 60. Interleaved COPYBACK PROGRAM with Status Register Monitoring



Note: A previous interleaved COPYBACK READ operation is required.

7.12.10 Interleaved COPYBACK READ MULTI-PLANE Operations

Figure 61 on page 75 shows how to perform interleaved COPYBACK READ MULTI-PLANE operations. In Figure 61, the READ STATUS ENHANCED (78h) command is used to monitor the status register for operation completion.

The interleaved COPYBACK READ MULTI-PLANE operation must meet multi-plane addressing requirements. See Section 7.11, "Multi-Plane Operations" on page 50 for details. The COPYBACK READ MULTI-PLANE operations must operate within the same plane.

An interleaved COPYBACK READ MULTI-PLANE operation is required before a COPYBACK PROGRAM MULTI-PLANE operation can be started. See "Interleaved COPYBACK READ MULTI-PLANE Operations" on page 72 for a description.

CHANGE WRITE COLUMN (85h) is permitted during interleaved COPYBACK READ MULTI-PLANE operations.

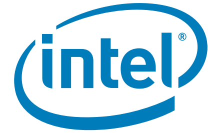
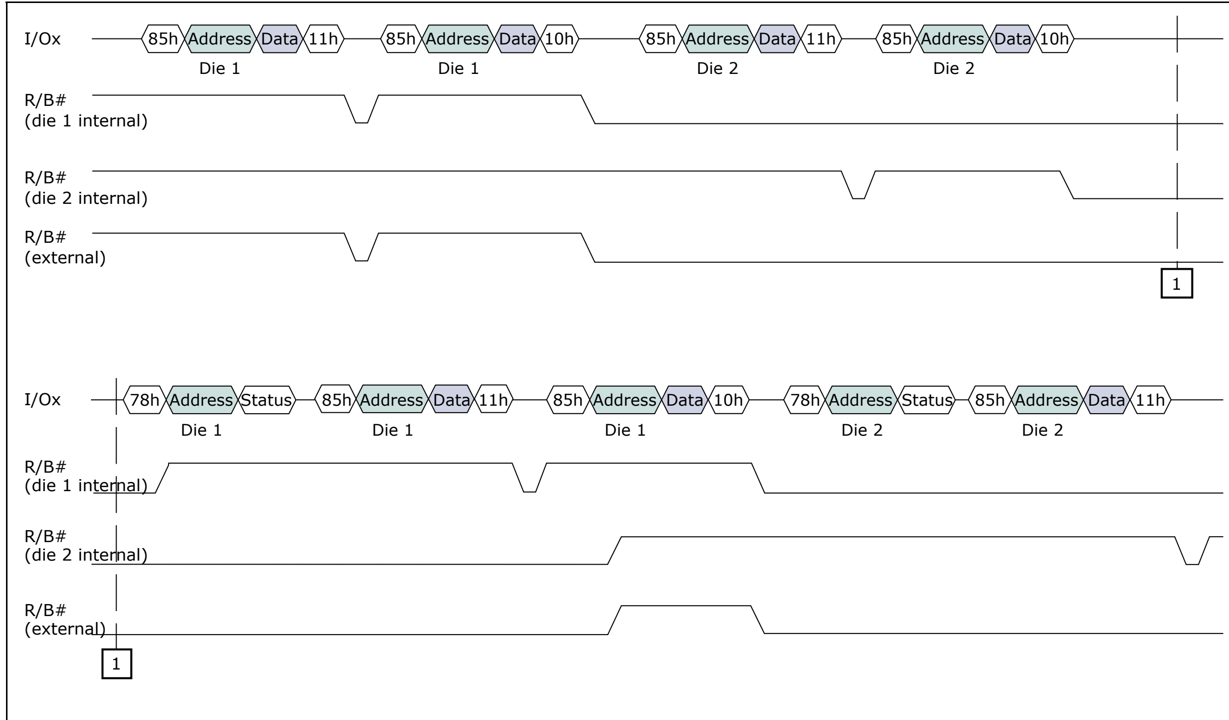


Figure 61. Interleaved COPYBACK PROGRAM MULTI-PLANE with Status Register Monitoring



Note: A previous interleaved COPYBACK READ MULTI-PLANE operation is required.

7.12.11 Interleaved BLOCK ERASE Operations

Figures 62 and 63 show how to perform two types of interleaved BLOCK ERASE operations. In Figure 62, the R/B# signal is monitored for operation completion. In Figure 62, the command is used to monitor the status register for operation completion.

Figure 62. Interleaved BLOCK ERASE with R/B# Monitoring

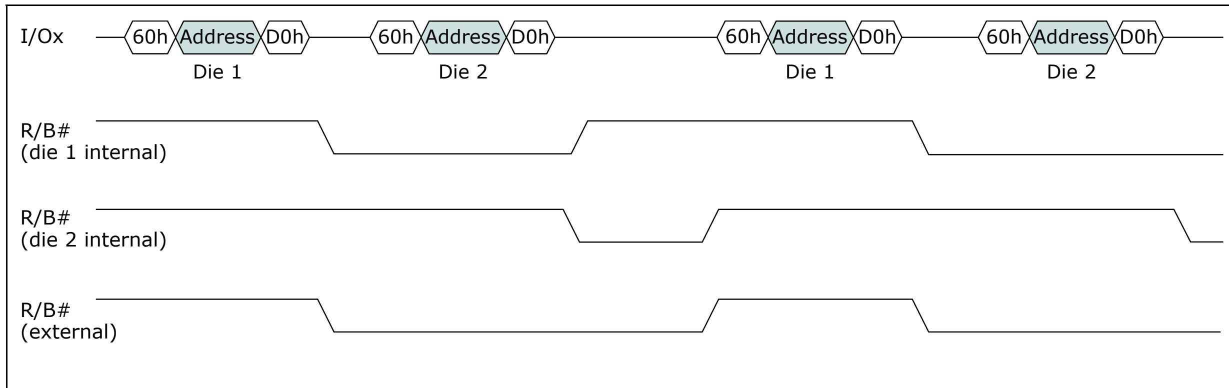
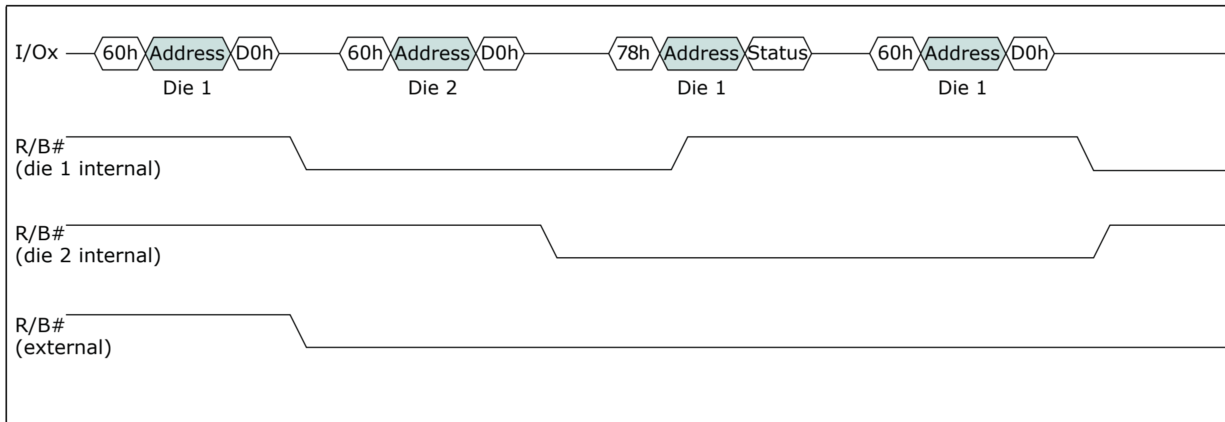


Figure 63. Interleaved BLOCK ERASE with Status Register Monitoring

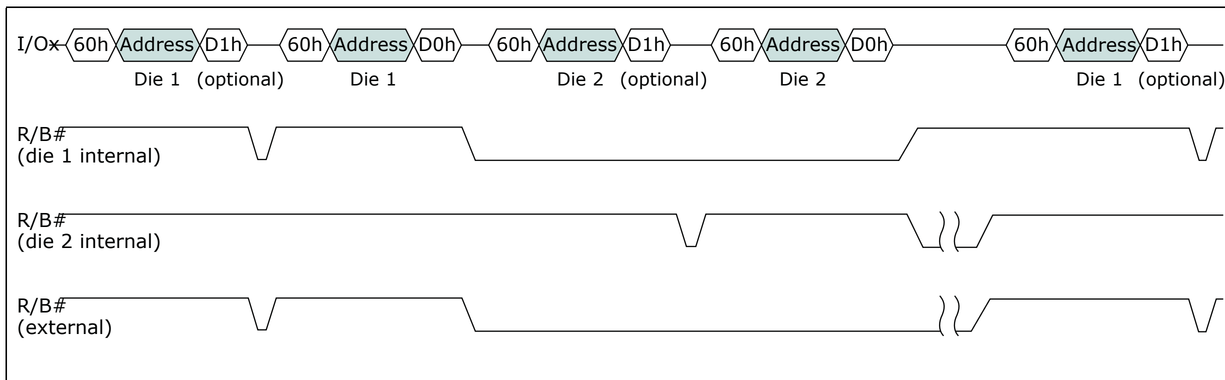


7.12.12 Interleaved BLOCK ERASE MULTI-PLANE Operations

Figure 64 and Figure 65 on page 77 show how to perform two types of interleaved BLOCK ERASE MULTI-PLANE operations. In Figure 64, the R/B# signal is monitored for operation completion. In Figure 65, the command is used to monitor the status register for operation completion.

The interleaved BLOCK ERASE MULTI-PLANE operation must meet two-plane addressing requirements. See Section 7.11, "Multi-Plane Operations" on page 50 for details.

Figure 64. Interleaved BLOCK ERASE MULTI-PLANE with R/B# Monitoring



Note: Multi-plane addressing requirements apply.

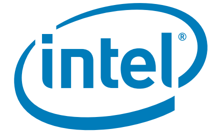
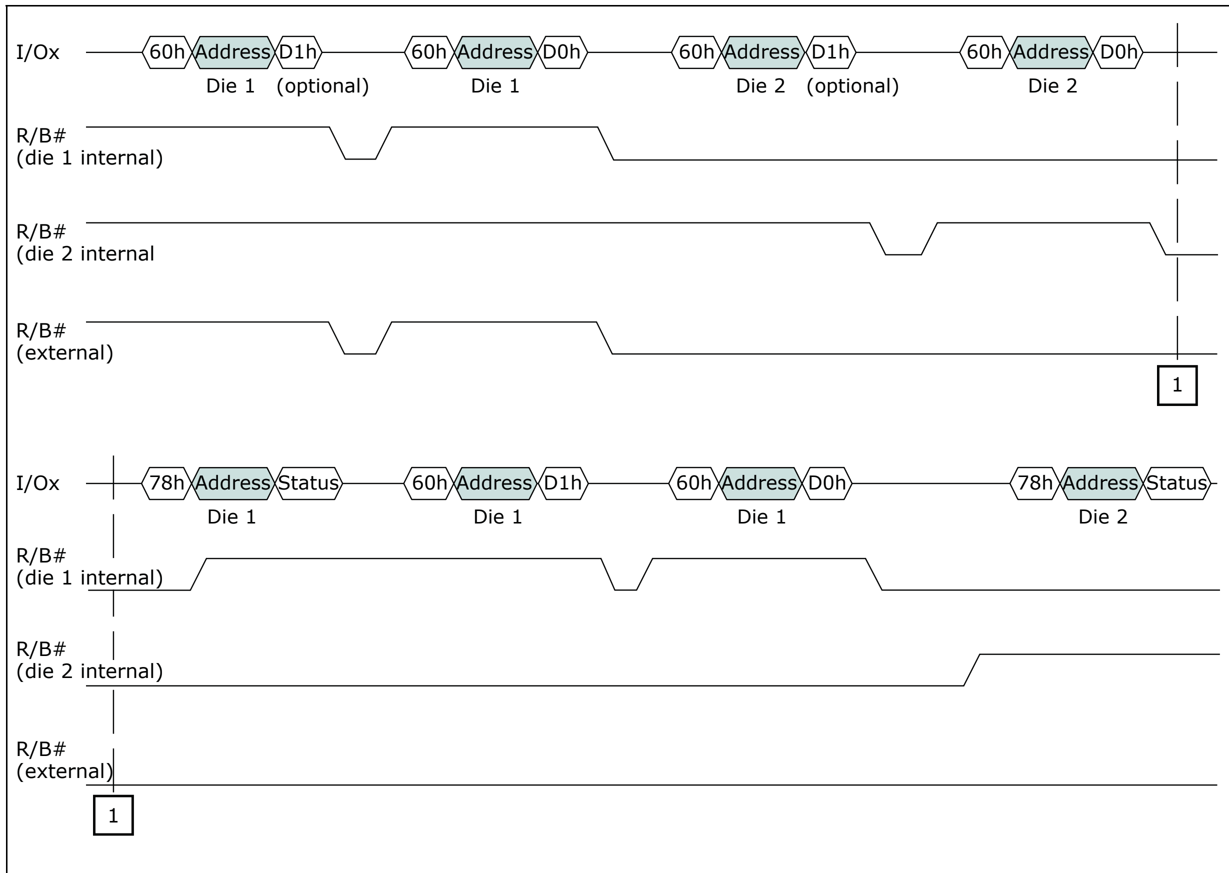


Figure 65. Interleaved BLOCK ERASE MULTI-PLANE with Status Register Monitoring



Note: Multi-plane addressing requirements apply.

7.13 WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using the WP# pin. Figures 66 through 77 illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, the WP# pin must not be toggled until the command is complete and the device is ready (status register bit 5 is “1”).

Figure 66. ERASE Enable

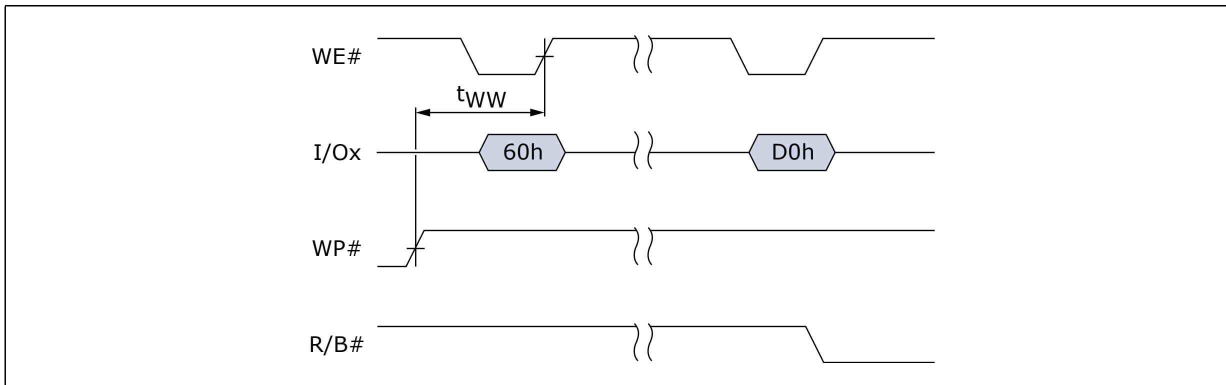


Figure 67. ERASE Disable

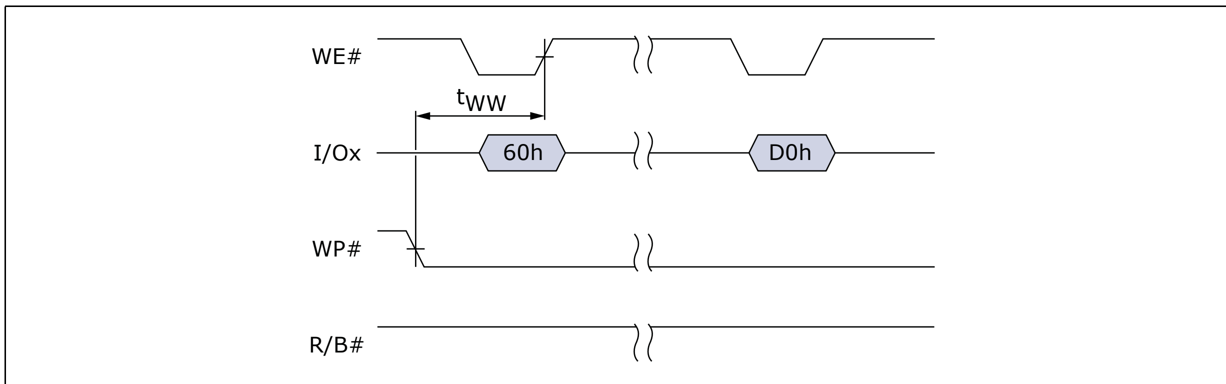
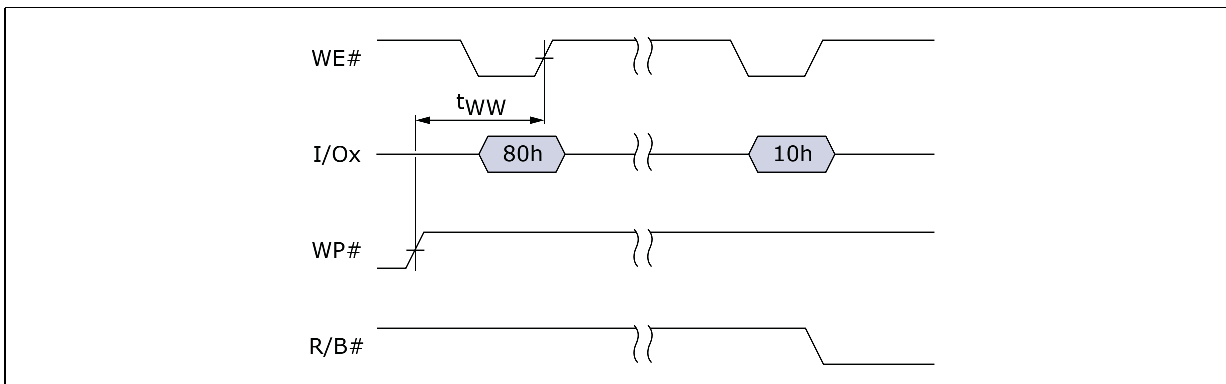


Figure 68. PROGRAM Enable



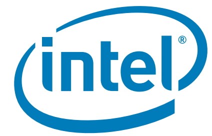


Figure 69. PROGRAM Disable

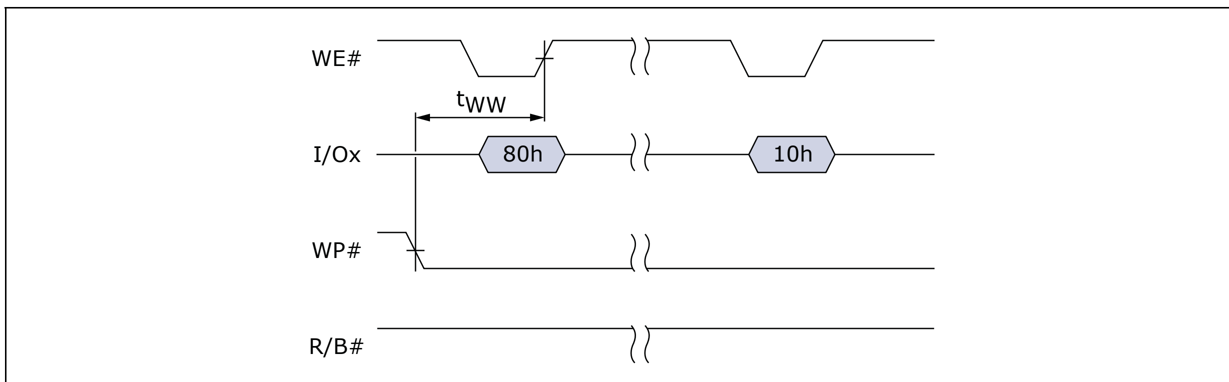


Figure 70. COPYBACK PROGRAM Enable

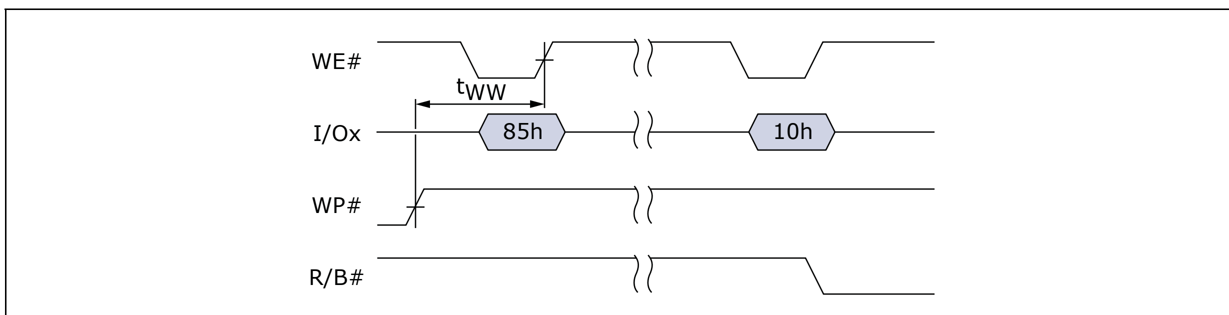


Figure 71. COPYBACK PROGRAM Disable

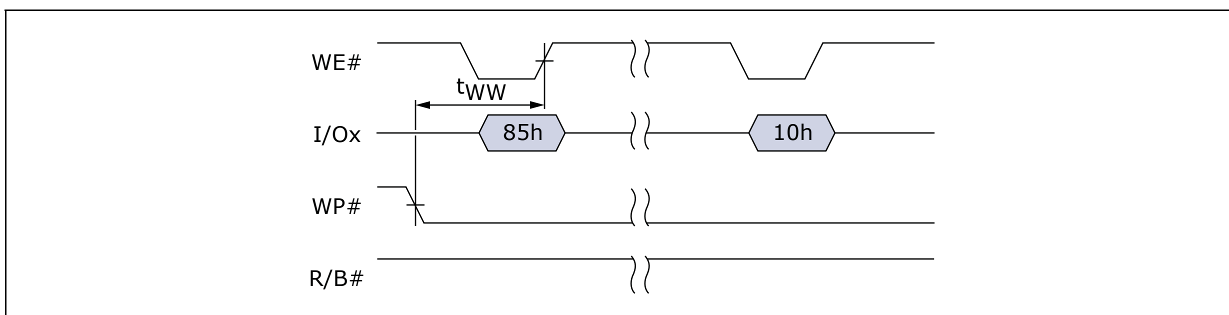


Figure 72. ERASE MULTI-PLANE Enable

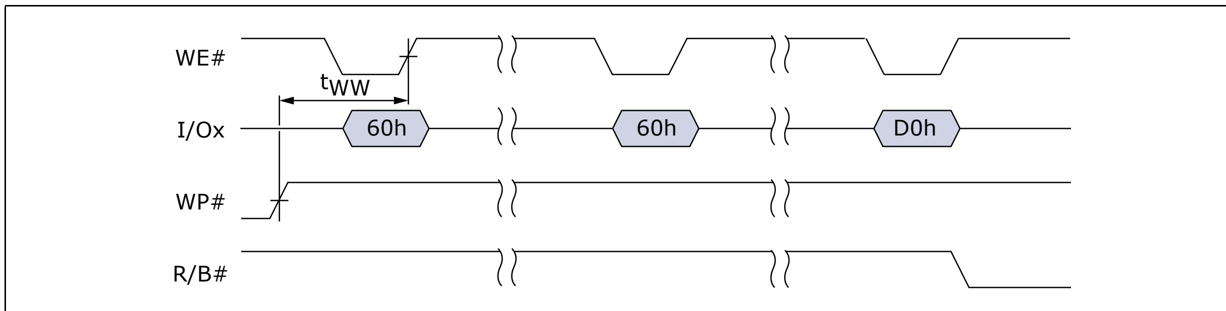


Figure 73. ERASE MULTI-PLANE Disable

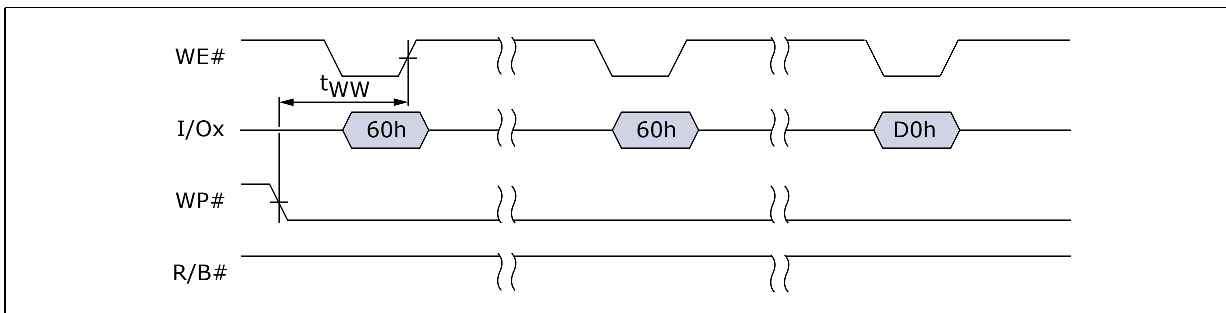
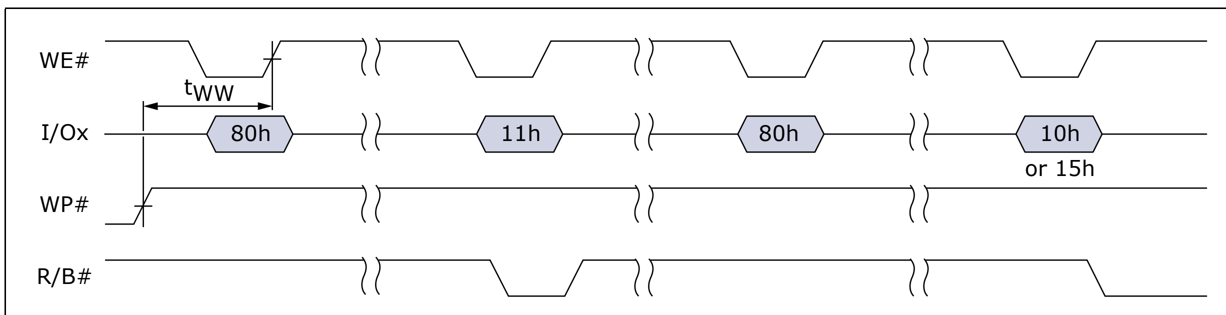


Figure 74. PROGRAM MULTI-PLANE Enable



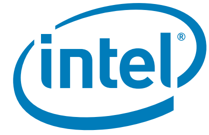


Figure 75. PROGRAM MULTI-PLANE Disable

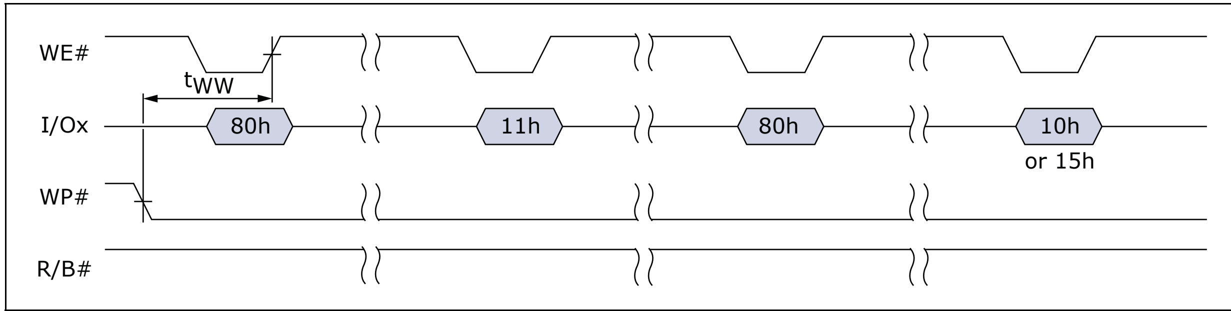


Figure 76. COPYBACK PROGRAM MULTI-PLANE Enable

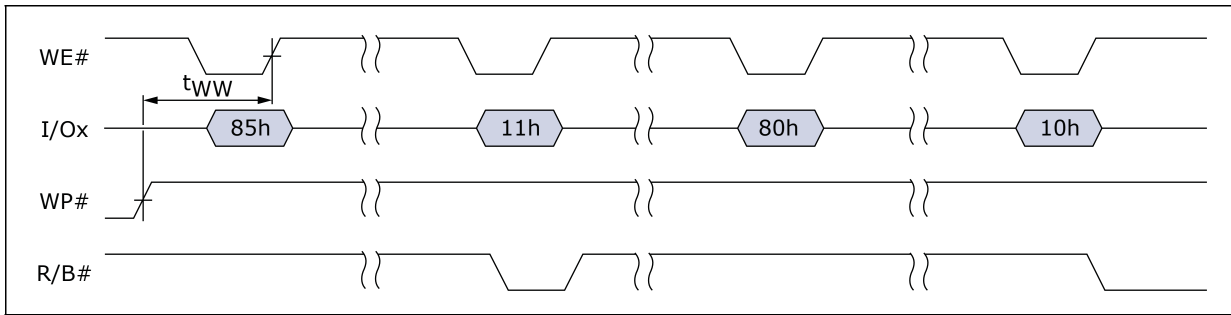
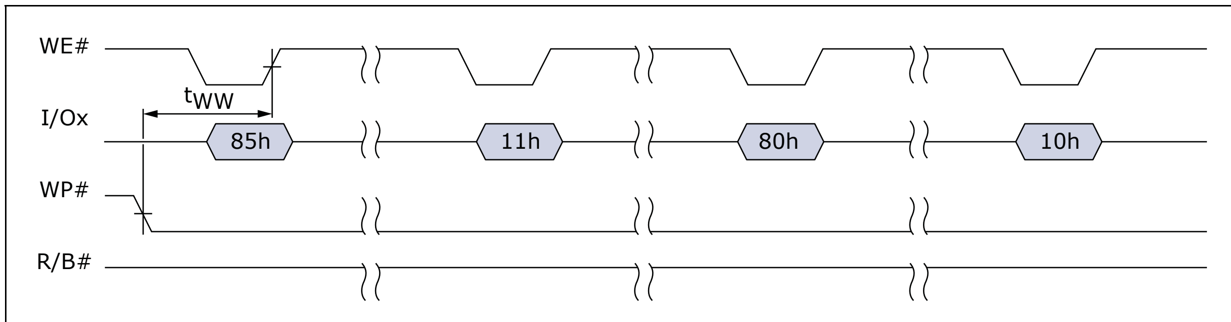
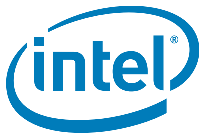


Figure 77. COPYBACK PROGRAM MULTI-PLANE Disable





8.0 Error Management

This NAND Flash device is specified to have a minimum of 3,936 MLC blocks (N_{VB}) out of 4,096 total available blocks. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains one or more bad bits. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below N_{VB} during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, the devices can be used quite reliably in systems that provide bad-block management and error correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare are location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements.

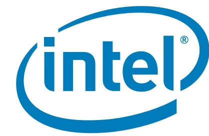
System software should check bytes 4,096 to 4,319 on the first page of each block for a 00h value prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad-block table can then be created, allowing system software to map around these areas. Factory testing is performed under worst-case conditions. Because blocks marked "bad" may be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Check status after a PROGRAM, ERASE, or COPYBACK operation.
- Under typical-use conditions, a minimum of 12-bit ECC for MLC devices is required per 540 bytes of data.
- Use bad block management and a wear-leveling algorithm.

Table 16. Error Management Details

Description	Requirement
Minimum number of valid blocks per LUN	3,936
Total available blocks per LUN	4,096
First spare area location	Byte 4,096
Bad-block mark	00h
Minimum required ECC	12-bit ECC per 540 bytes of data



9.0 Electrical Characteristics

Table 17. Absolute Maximum Ratings by Device.

Parameter/Condition	Symbol	Min	Max	Unit
Voltage input	V_{IN}	–0.6	+4.6	V
V_{CC} supply voltage	V_{CC}	–0.6	+4.6	V
VccQ supply voltage	VccQ	-0.6	+4.6	V
Storage temperature	T_{STG}	–65	+150	°C
Short circuit output current, I/Os		–	5	mA

Note: Voltage on any pin relative to Vss.

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating ***only***, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 18. Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	+70	°C
	Extended		–40	–	+85	°C
V_{CC} supply voltage		Vcc	2.7	3.3	3.6	V
VccQ supply voltage		VccQ	2.7	3.3	3.6	V
Vss ground voltage		Vss	0	0	0	V
VssQ ground voltage		VssQ	0	0	0	V

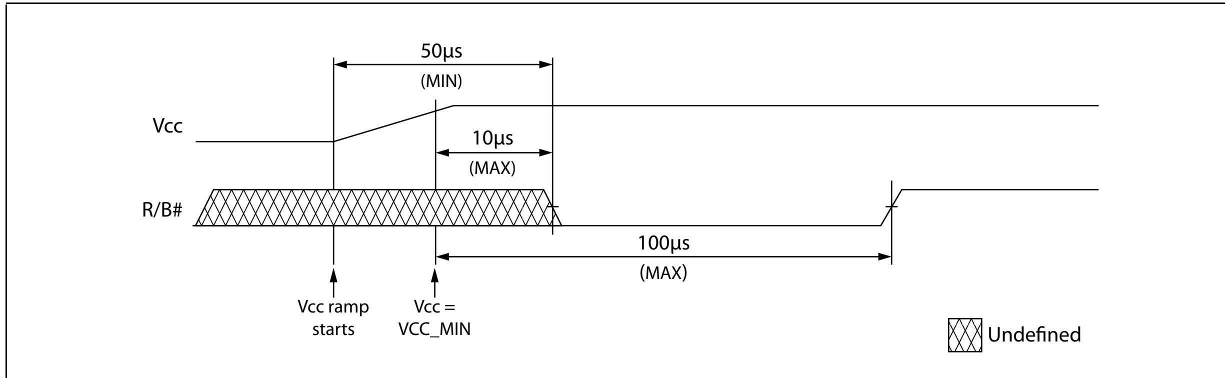
9.1 V_{CC} Power Cycling

Intel NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. The CLE and ALE signals should be kept at V_{IL} during V_{CC} ramp to avoid an inadvertent command latch. The WP# signal permits additional hardware protection during power transitions. When ramping Vcc and VccQ, use the following procedure to initialize the device:

1. Ramp Vcc to 2.7-3.6 V.
2. Ramp VccQ to 2.7-3.6 V not sooner than the Vcc ramp. VccQ must not exceed Vcc.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target. The R/B# signal becomes valid when
   - 50 µs has elapsed since the beginning the VccQ ramp, and
   - 10 µs has elapsed since VccQ reaches 2.7 V
4. If not monitoring R/B#, the host must wait at least 100 µs from VccQ reaching 2.7 V.
5. all of the targets on the device power-on with the asynchronous interface active. Each NAND LUN draws less than an average of 10 mA (IST) measured over intervals of 1 ms until the RESET (FFh) command is issued.

6. The RESET (FFh) command must be issued to all targets (CE#s) as the first command after the NAND Flash device is powered on. Each target will be busy for a maximum of 1 ms after the RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
7. The device is now initialized and ready for normal operations. At power-down, VccQ must go LOW before or simultaneously with Vcc going LOW.

Figure 78. R/B# Power-On Behavior



Notes:
1. If Vcc takes 40 µs or greater to reach Vcc_min from the start of the Vcc ramp, then R/B shall be valid 10 µs after reaching Vcc_min. If Vcc takes less than 40 µs to reach Vcc_min from the start of the Vcc ramp, then R/B shall be valid 50 µs from the start of the Vcc ramp.
2. When Vcc reaches Vss_min, R/B# will be valid HIGH within 100 µs. Then the host can issue the RESET (FFh) command.

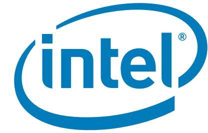
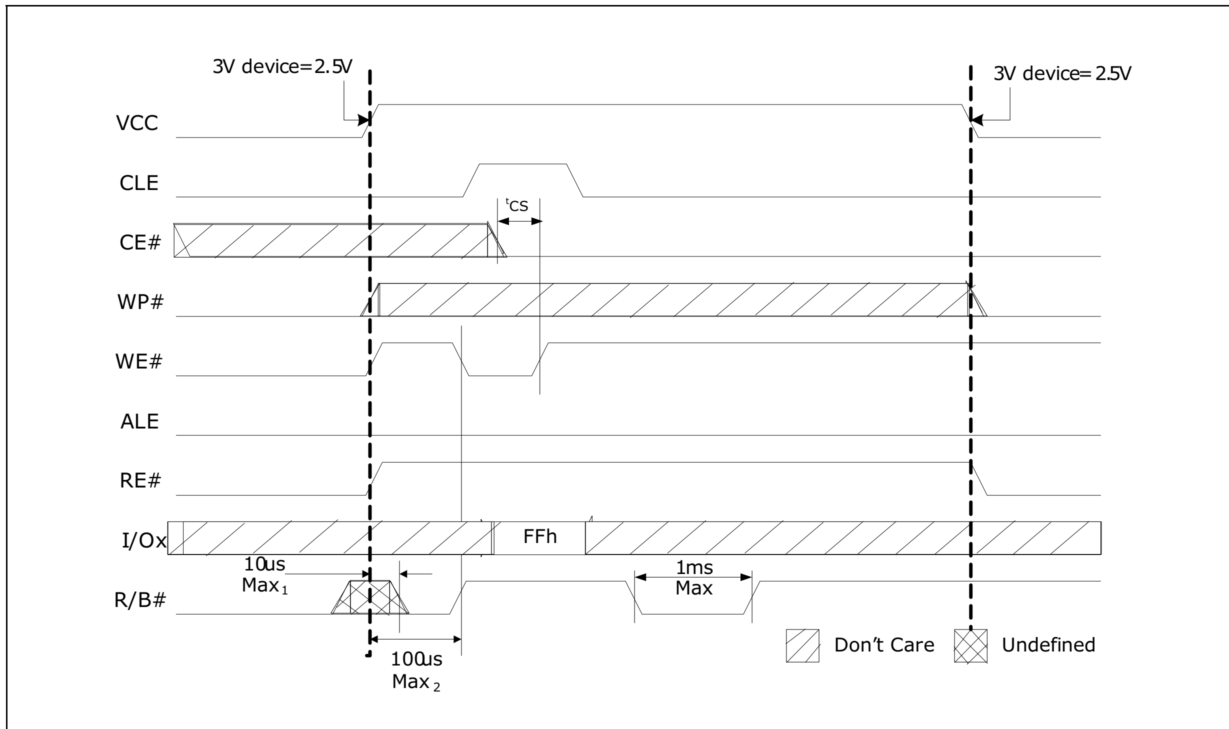


Figure 79. AC Waveforms During Power Transition



Notes:
1. If Vcc takes 40 µs or greater to reach Vcc_min from the start of the Vcc ramp, then R/B shall be valid 10 µs after reaching Vcc_min. If Vcc takes less than 40 µs to reach Vcc_min from the start of the Vcc ramp, then R/B shall be valid 50 µs from the start of the Vcc ramp.
2. When Vcc reaches 2.5 V, R/B# will be valid HIGH within 100 µs. Then the host can issue the RESET (FFh) command.

Table 19. Device DC and Operating Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Sequential read current	^{t}RC = ^{t}RC (MIN), CE# = V_{IL}, I_{OUT} = 0mA	$I_{CC}1$	–	20	40	mA
Program current	–	$I_{CC}2$	–	20	40	mA
Erase current	–	$I_{CC}3$	–	20	40	mA
Standby current (TTL)	CE# = V_{IH}, WP# = 0V/VCC	$I_{SB}1$	–	–	1	mA
Standby current (CMOS)	CE# = V_{CC} – 0.2V, WP# = 0V/V_{CC}	$I_{SB}2$	–	10	50	µA
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA
Input high voltage	I/Ox, CE#, CLE, ALE, WE#, RE#, WP#, R/B#	V_{IH}	0.8 x Vcc	–	V_{CC} + 0.3	V
Input low voltage (all inputs)	–	V_{IL}	–0.3	–	0.2 x Vcc	V
Output high voltage	I_{OH} = –400µA	V_{OH}	0.67 x Vcc	–	–	V
Output low voltage	I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V
Output low current (R/B#)	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA

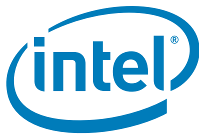


Table 19. Device DC and Operating Characteristics (Continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Staggered power-up current	^{t}Rise = 1ms, cLine = 0.1uF. Before Reset command is issued and after VCC reaches VCC_min = 2.5V.[1]	IST			10 per Die	mA

Notes:
1. Until a Reset command is received by the NAND package (SDP, DDP, QDP or ODP) after power-up, the NAND package (SDP, DDP, QDP or ODP) shall not draw more than 10 mA per die. IST is measured with a nominal rise time of 1 ms and a line capacitance of 0.1µF. The measurement shall be taken with 1ms averaging intervals and shall begin after VCC reaches VCC_min = 2.5 V.
2. All operating current ratings are specified per die for single plane operations. It can be greater for dual plane and interleaved die operations.

Table 20. Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	JS29F32G08AAMDB	3,936	4,096	Blocks	1, 2
		JS29F64G08CAMDB	7,872	8,192		1, 3
		JS29F16B08JAMDB	15,744	16,384		1, 4

Notes:
1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Each 32 Gb section has a maximum of 160 invalid blocks.
3. Each 64 GB section has a maximum of 320 invalid blocks.
4. Each 128 Gb section has a maximum of 640 invalid blocks.

Table 21. Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input capacitance	CIN	SDP	10	pF	1, 2
		DDP	20		
		QDP	40		
Input/output capacitance (I/O)	COUT	SDP	10	pF	1, 2
		DDP	20		
		QDP	40		

Notes:
1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_C = 25°C; f = 1 MHz; VIN = 0V.

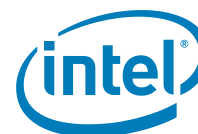


Table 22. Test Conditions

Parameter		Value	Notes
Input pulse levels	JS29FxxxxxxAMDB	0.0V to 3.3V	
Input rise and fall times		5ns	
Input and output timing levels		Vcc/2	
Output load	JS29Fxxx08xAMDB (Vcc = 2.5-3.3V)	1 TTL GATE and CL = 50pF	1
	JS29Fxxx08xAMDB (Vcc = 3.3V ± 10%)	1 TTL GATE and CL = 100pF	1

Note: Verified in device characterization; not 100 percent tested.

Table 23. AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	Standard Operating Modes		Unit
		Min	Max	
ALE to data start[1]	^{t}ADL	70	–	ns
ALE hold time	^{t}ALH	5	–	ns
ALE setup time	^{t}ALS	10	–	ns
CE# hold time	^{t}CH	5	–	ns
CLE hold time	^{t}CLH	5	–	ns
CLE setup time	^{t}CLS	10	–	ns
CE# setup time	^{t}CS	15	–	ns
Data hold time	^{t}DH	5	–	ns
Data setup time	^{t}DS	7	–	ns
WRITE cycle time	^{t}WC	20	–	ns
WE# pulse width HIGH	^{t}WH	7	–	ns
WE# pulse width	^{t}WP	10	–	ns
WP# setup time	^{t}WW	30	–	ns

Notes:
1. Timing for ^{t}ADL begins in the ADDRESS cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.
2. Standard operating-mode timings meet ONFI timing mode 5 parameters.

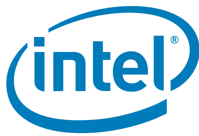


Table 24. AC Characteristics: Normal Operation

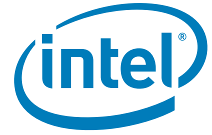
Parameter	Symbol	Standard Operating Modes		Unit	Notes
		Min	Max		
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	25	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	ns	1
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15		ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
Data transfer from Flash array to data register	^{t}R	–	50	µs	
READ cycle time	^{t}RC	20	–	ns	
RE# access time	^{t}REA	–	16	ns	2
RE# HIGH hold time	^{t}REH	7	–	ns	2
RE# HIGH to output hold	^{t}RHOH	15	–	ns	2
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	1, 2
RE# LOW to output hold	^{t}RLOH	5		ns	2
RE# pulse width	^{t}RP	10	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	60	–	ns	

Notes:
1. Transition is measured ±200 mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
2. AC characteristics may need to be relaxed if I/O drive strength is not set to "full."
3. The first RESET command after powering up will cause the device to stay busy for up to 1 ms. Subsequent RESET commands, while in the ready state mode, will drive the device busy for a maximum of 5 µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.
5. Standard operating-mode timings meet ONFI timing mode 5 parameters.

Table 25. PROGRAM/ERASE Characteristics

Symbol	Parameter	Typ	Max	Unit	Notes
NOP	Number of partial page programs	–	1	Cycle	1
^{t}BERS	BLOCK ERASE operation time	2	10	ms	
^{t}CBSY	Busy time for PROGRAM CACHE operation	3	2,200	µs	2
^{t}RCBSY	Busy time for READ CACHE operation	3	50	µs	3
^{t}DBSY	Dummy busy time	0.5	1	µs	
^{t}FEAT	Busy time for SET FEATURES and GET FEATURES operations		1	µs	
^{t}ITC	Busy time for interface change		1	µs	4
^{t}OBSY	Busy time for OTP DATA PROGRAM operation if OTP is protected		25	µs	
^{t}LPROG	LAST PAGE PROGRAM operation time	–	–	–	5
^{t}PROG	PAGE PROGRAM operation time	900	2,200	µs	
^{t}R	READ operation time		50	µs	
^{t}CCS	Change Column Setup time	200	–	ns	6

Notes:
1. One total to the same page. NOP for OTP pages is "8".
2. ^{t}CBSY MAX time depends on timing between internal program completion and data in.
3. ^{t}RCBSY MAX time depends on timing between internal read completion.
4. ^{t}ITC (MAX) is the busy time when the interface changes from asynchronous to synchronous using the SET FEATURES (EFh) command or synchronous to asynchronous using the RESET (FFh) command. During the ^{t}ITC time, the READ STATUS (70h) and READ STATUS ENHANCED (78h) commands are prohibited.
5. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last – 1 page) – command load time (last page) – address load time (last page) – data load time (last page).
6. ^{t}CCS is a min spec. The CHANGE WRITE/READ COLUMN command would use this spec.



10.0 Timing Diagrams

Figure 80. COMMAND LATCH Cycle

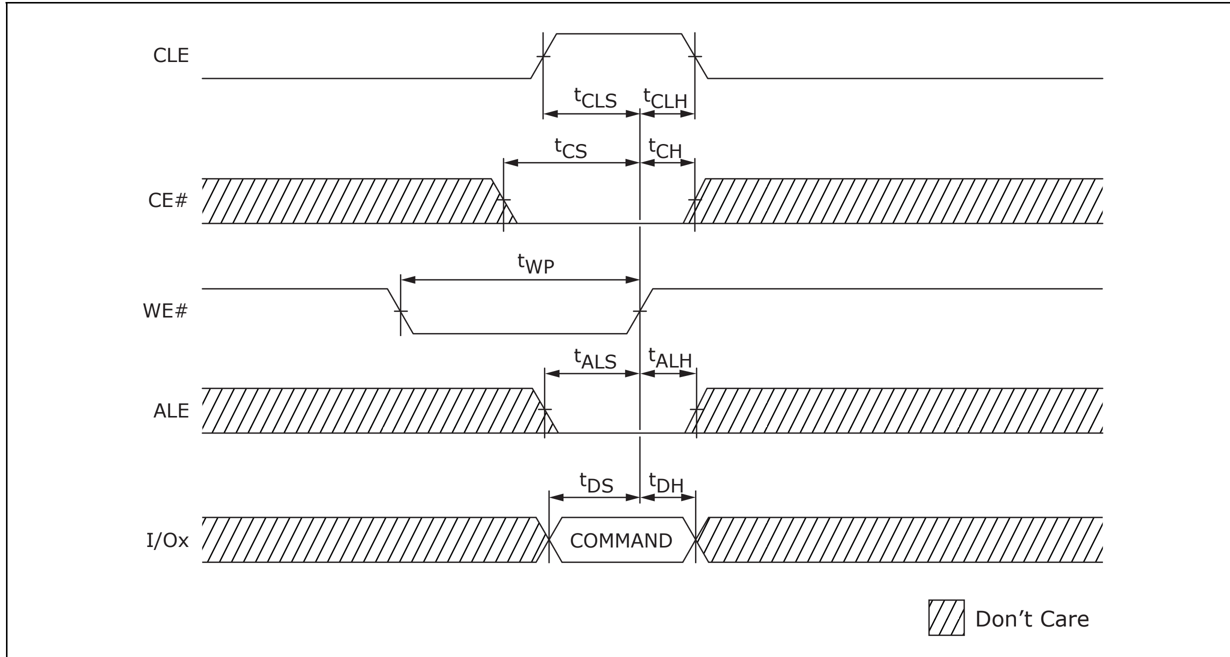


Figure 81. ADDRESS LATCH Cycle

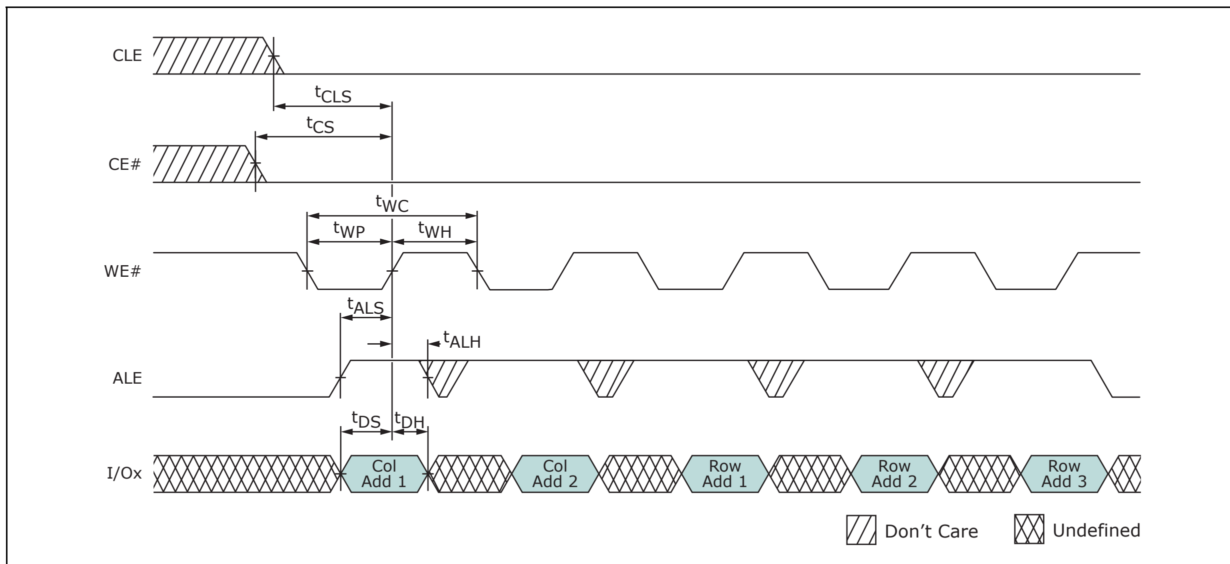


Figure 82. INPUT DATA LATCH

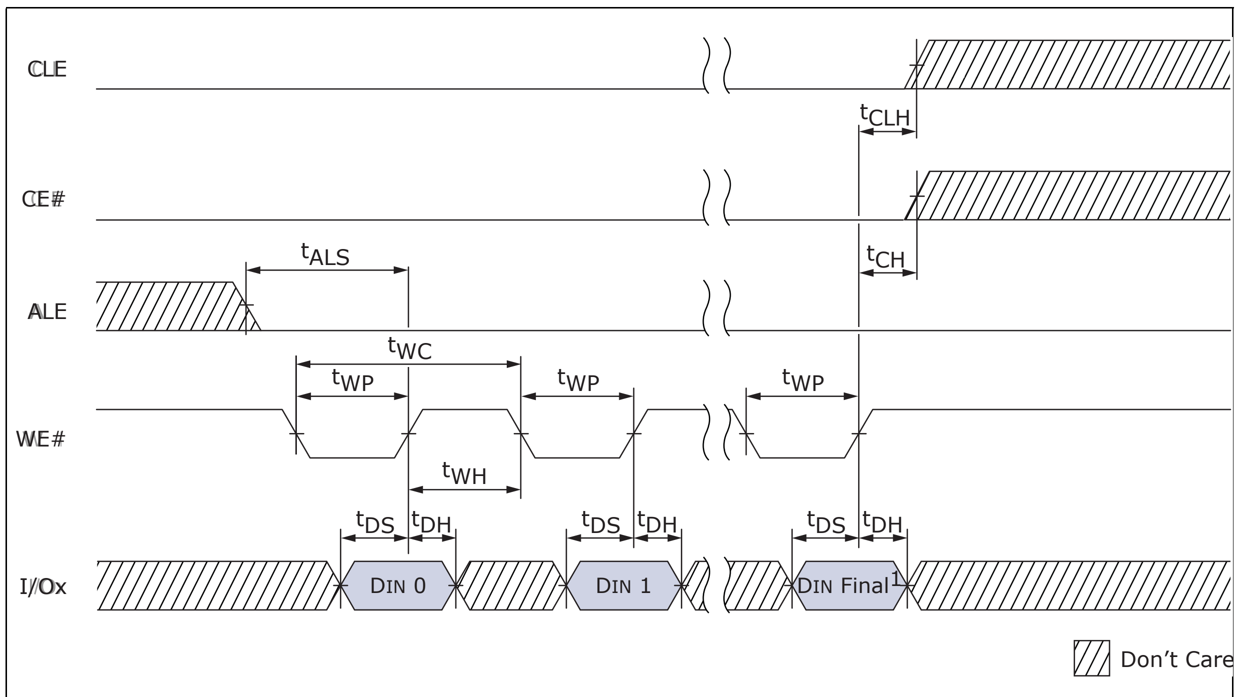
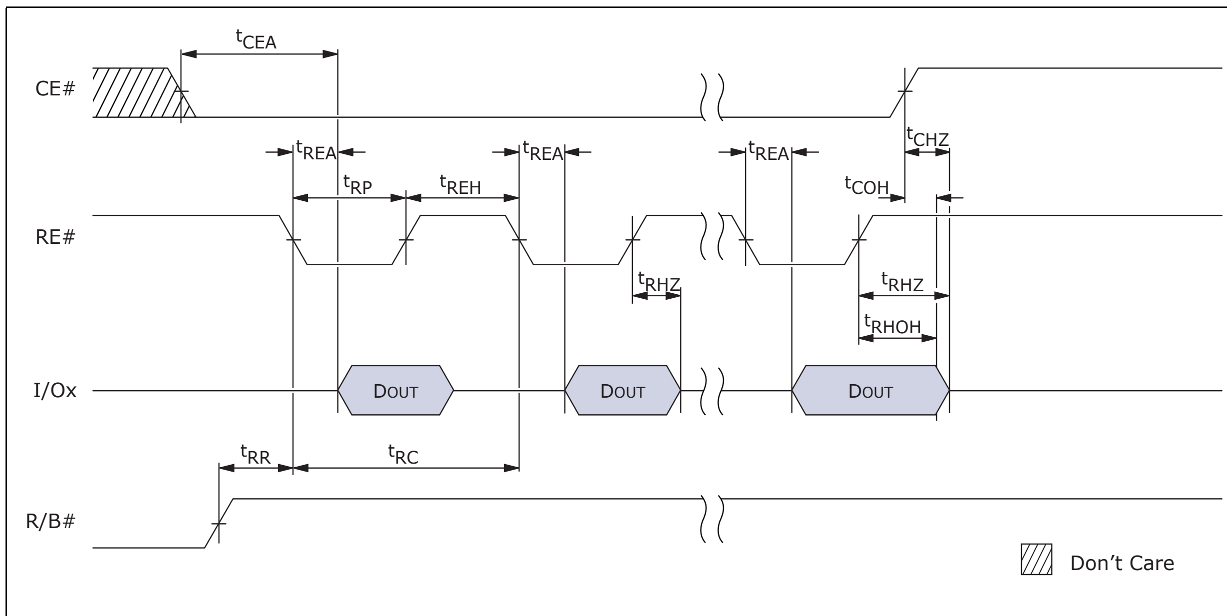


Figure 83. SERIAL ACCESS Cycle After READ



Note: Use this timing diagram for $^{t}RC \geq 30$ ns.

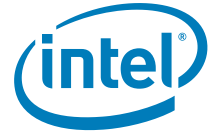
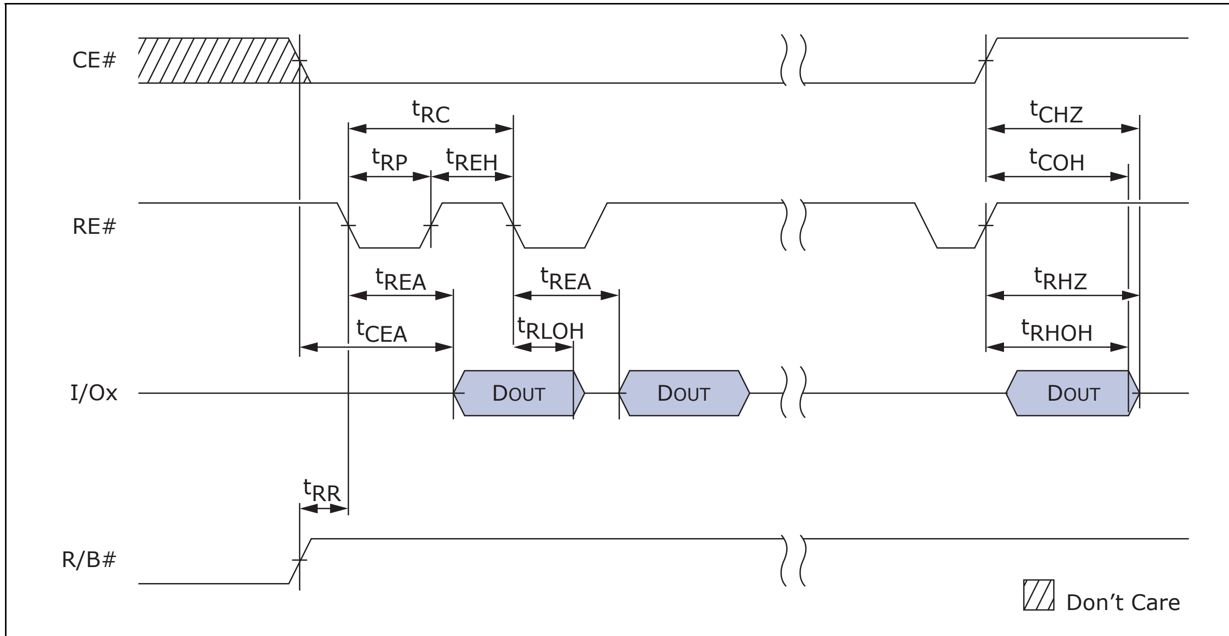


Figure 84. SERIAL ACCESS Cycle After READ (EDO Mode)



Note: Use this timing diagram for ^{t}RC < 30 ns.

Figure 85. READ STATUS Cycle

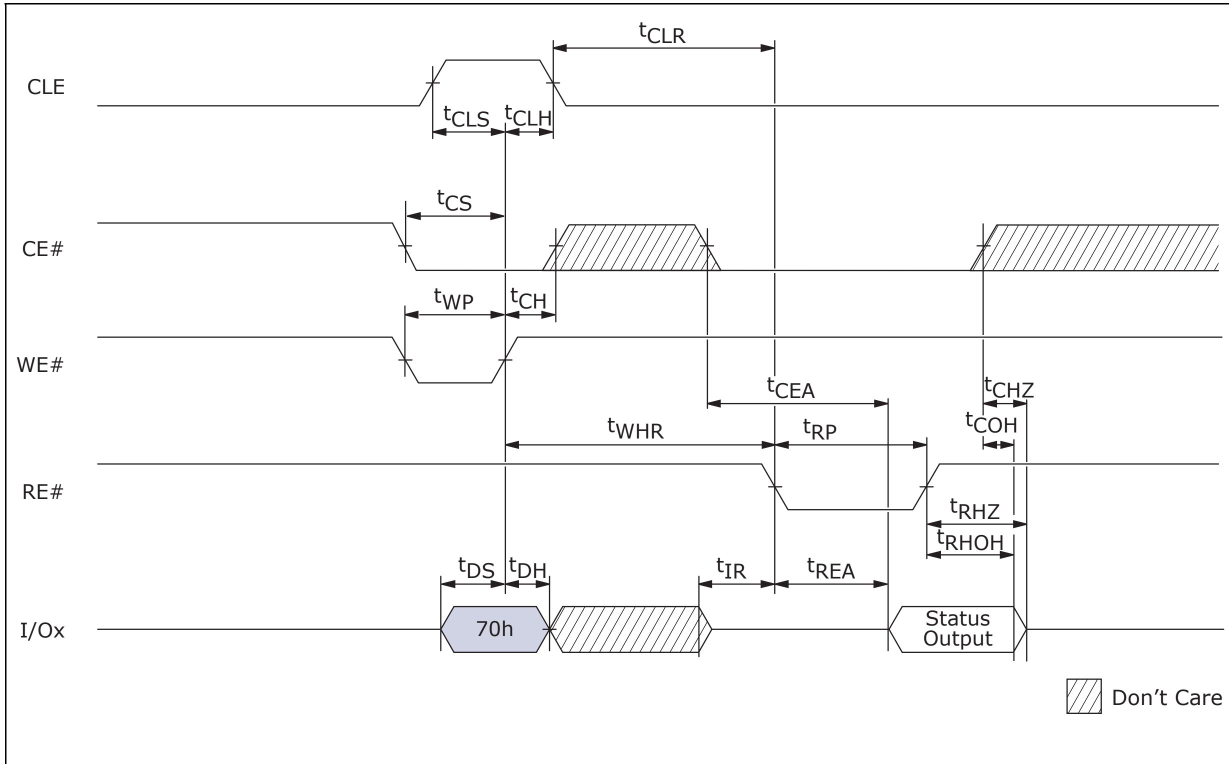


Figure 86. READ STATUS ENHANCED Operation

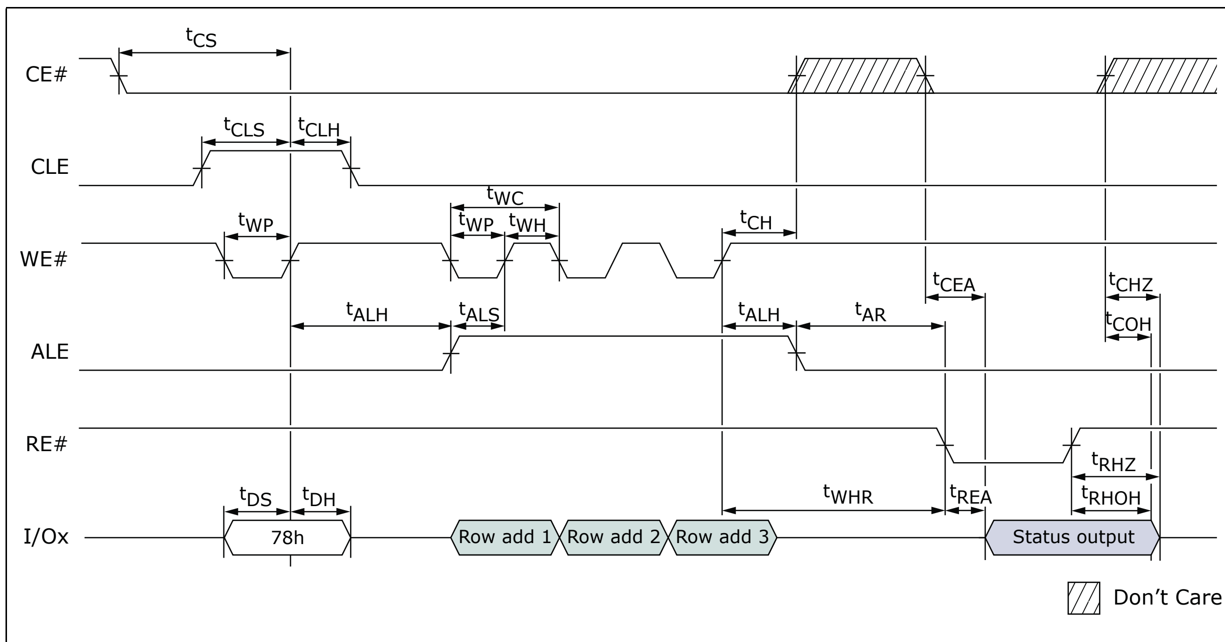
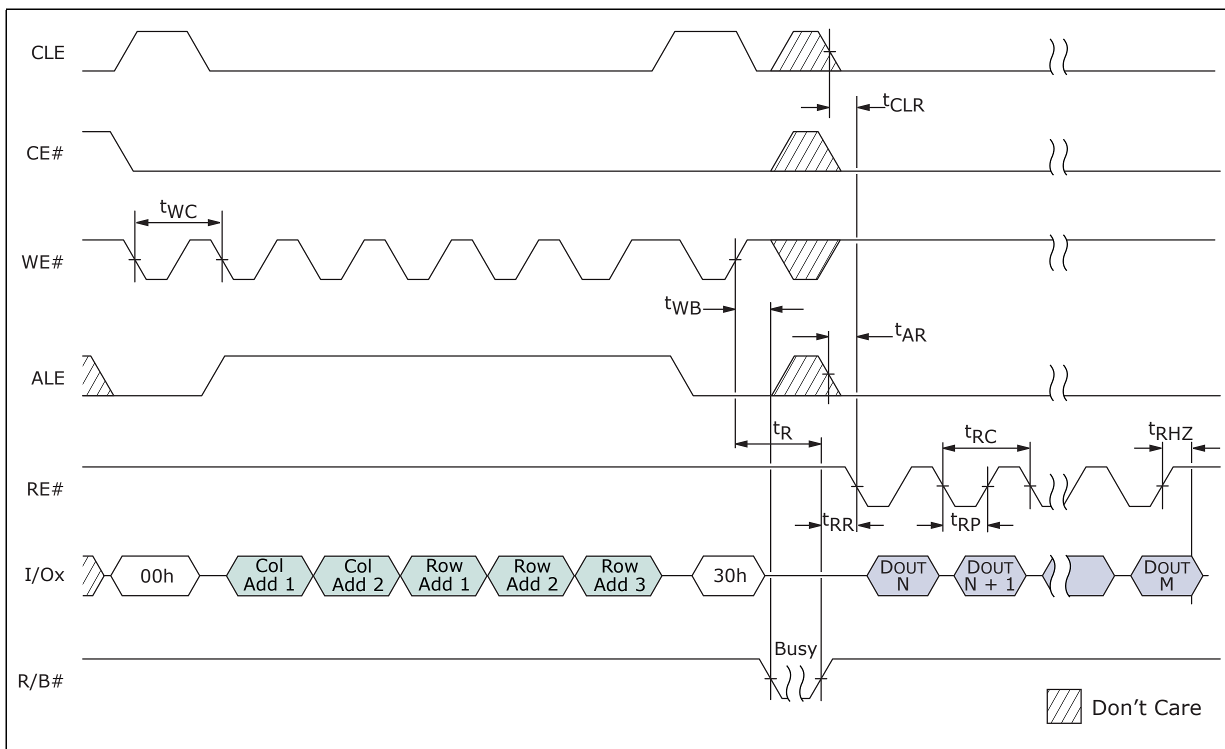


Figure 87. READ



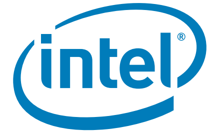


Figure 88. READ Operation with CE# "Don't Care"

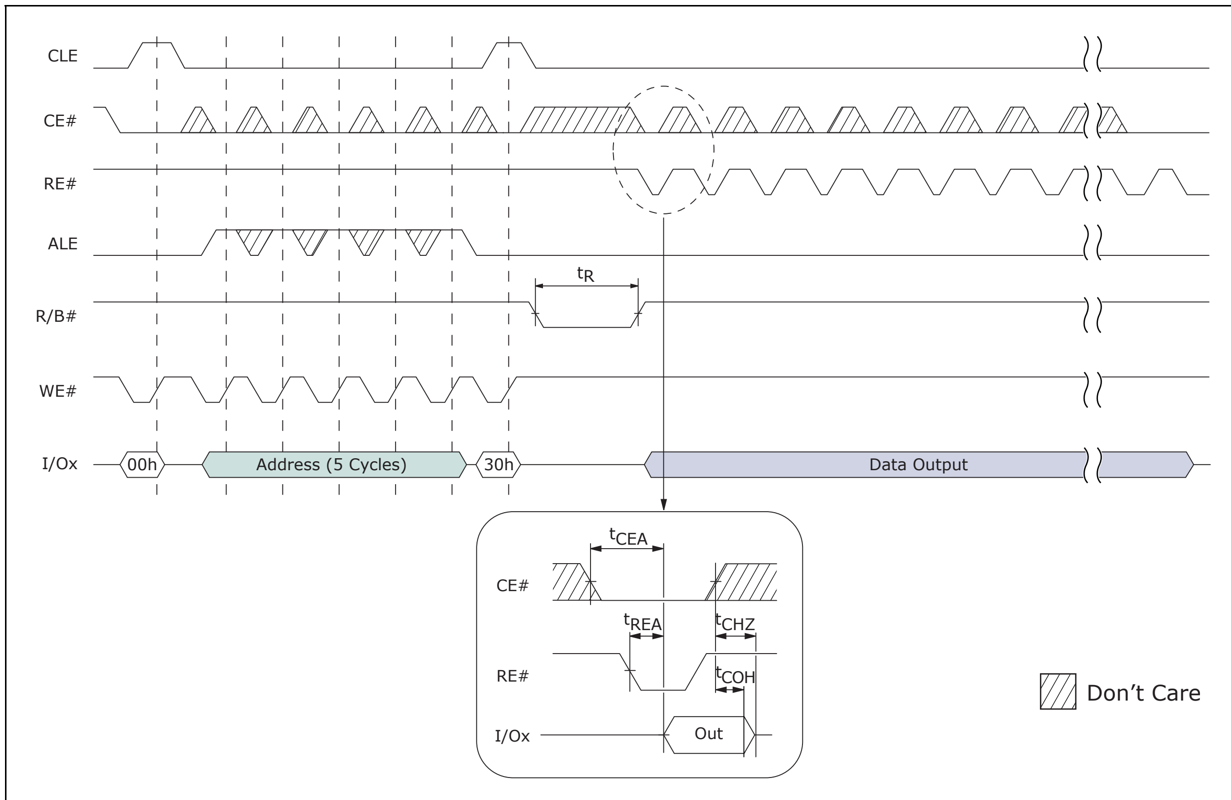


Figure 89. CHANGE READ COLUMN

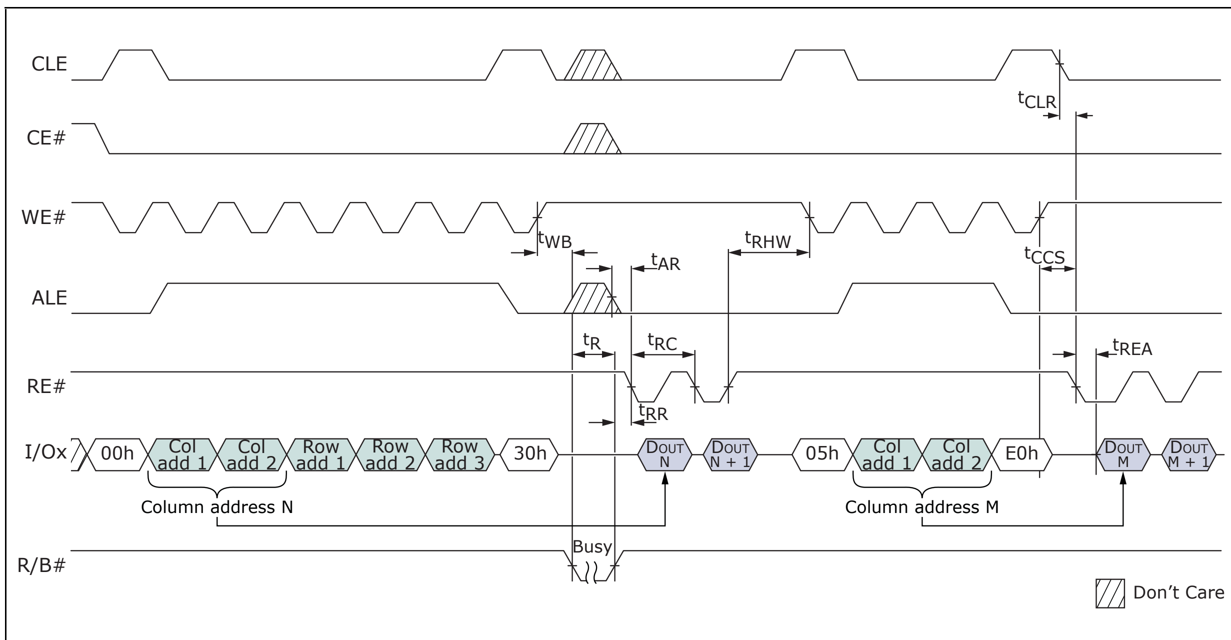


Figure 90. READ CACHE Mode Operations Timing Diagram, Part 1 of 2

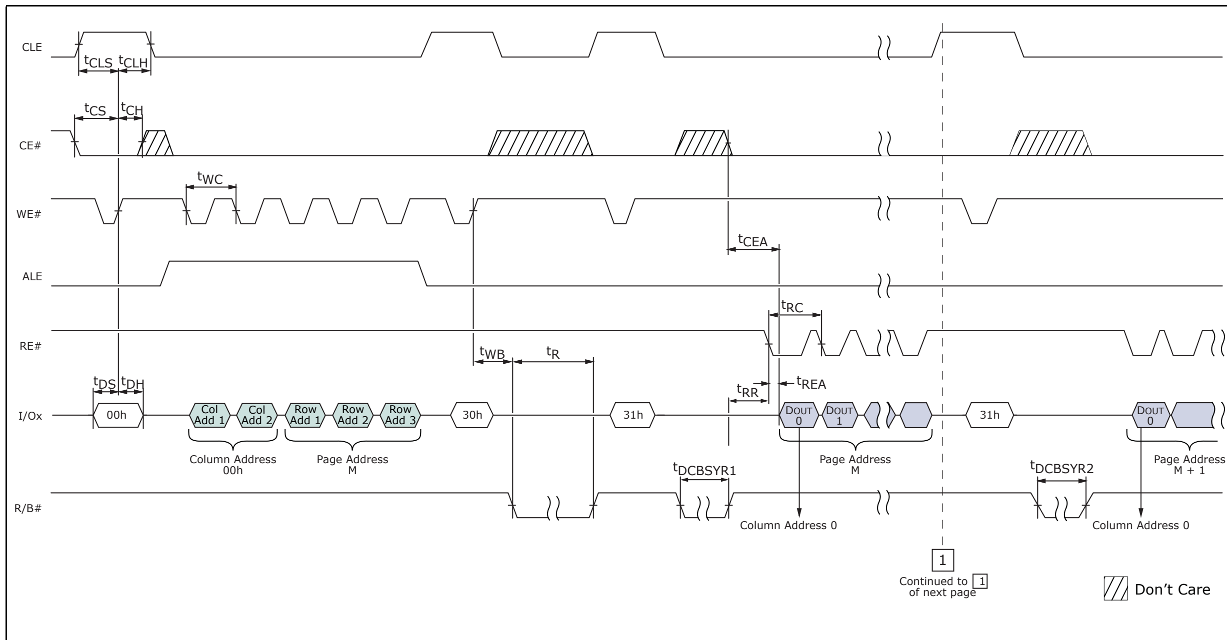
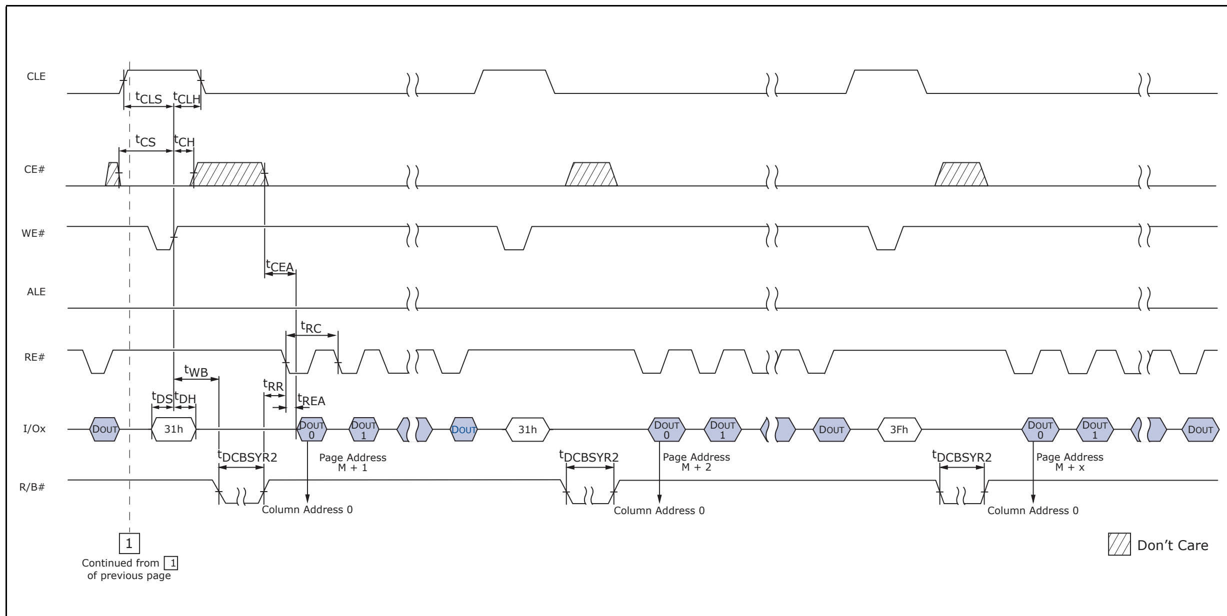


Figure 91. READ CACHE Mode Operations Timing Diagram, Part 2 of 2



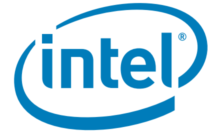


Figure 92. READ CACHE Mode Operations Timing without R/B#, Part 1 or 2

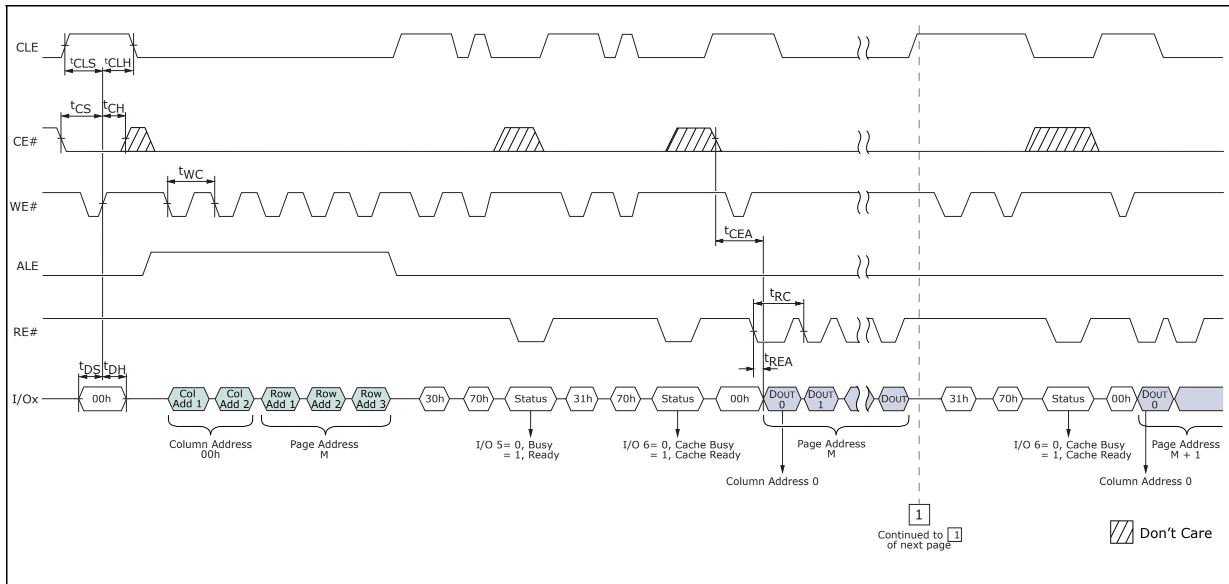


Figure 93. READ CACHE Mode Operations Timing without R/B#, Part 2 of 2

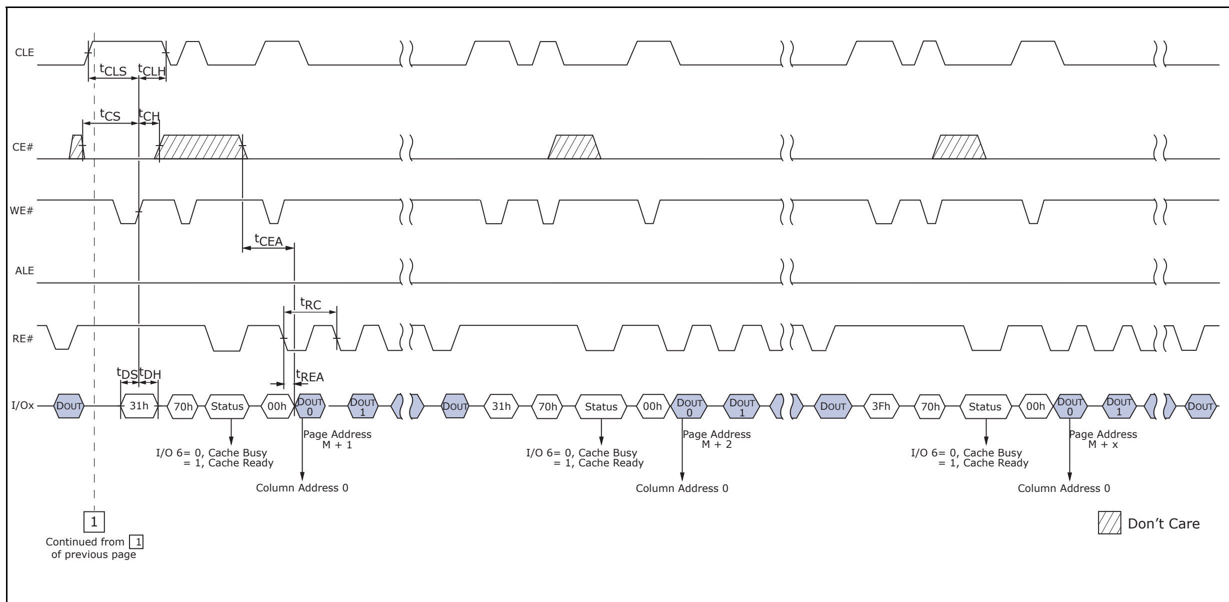
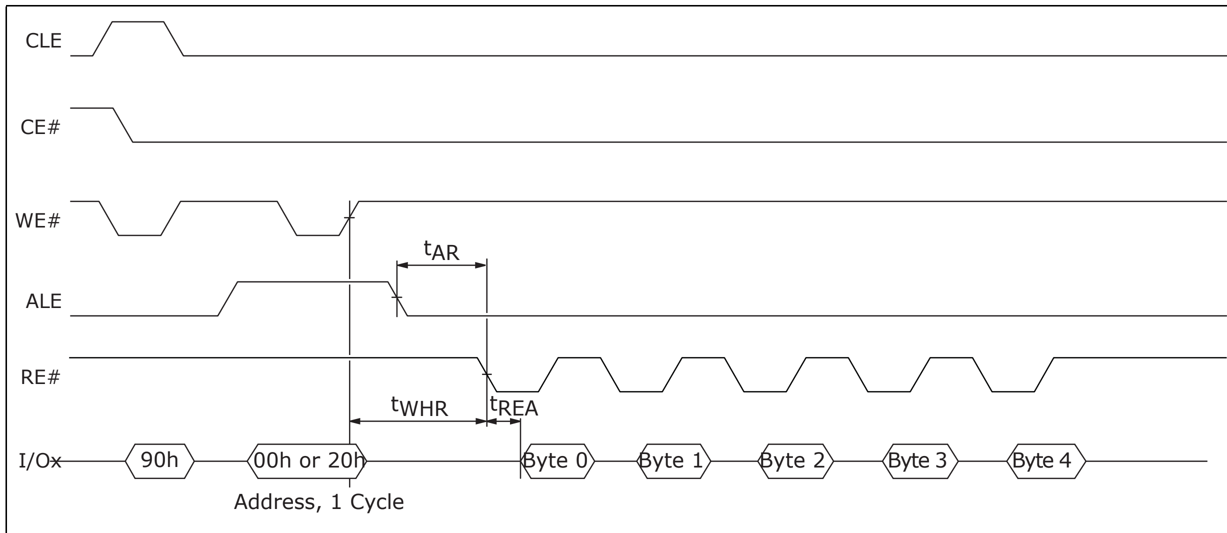
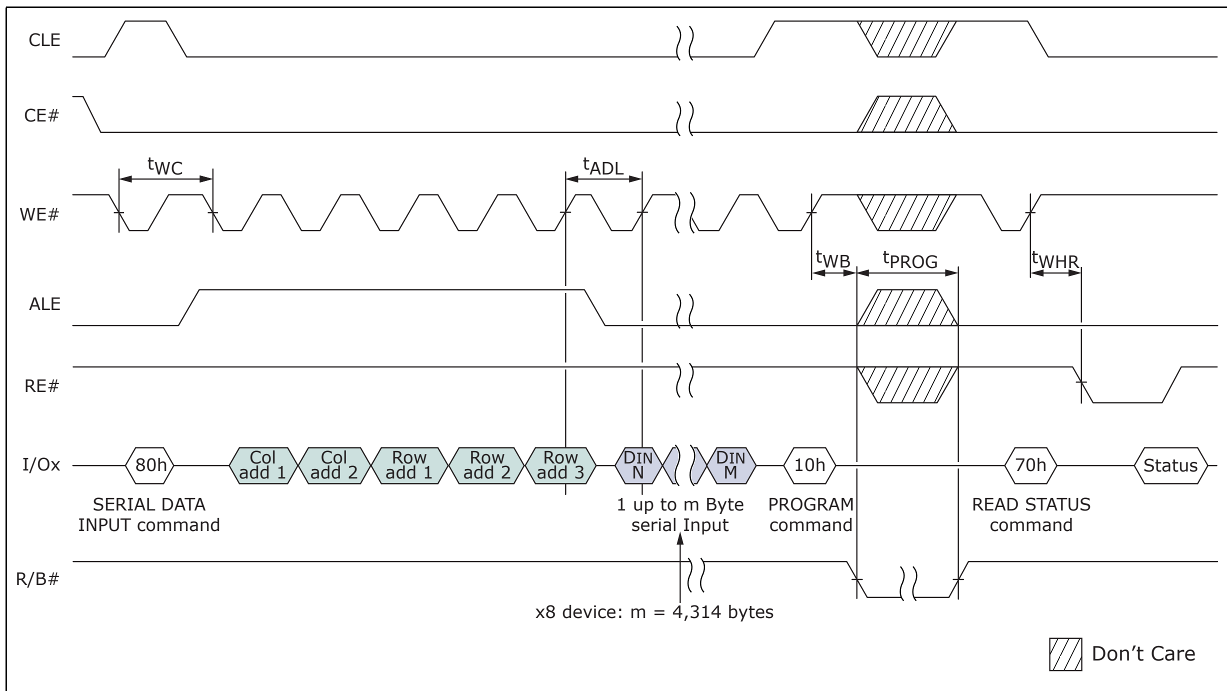


Figure 94. READ ID Operation



Note: See Table 9 on page 23 for actual values.

Figure 95. PAGE PROGRAM Operation



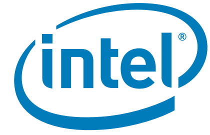


Figure 96. PAGE PROGRAM Operation with CE# "Don't Care"

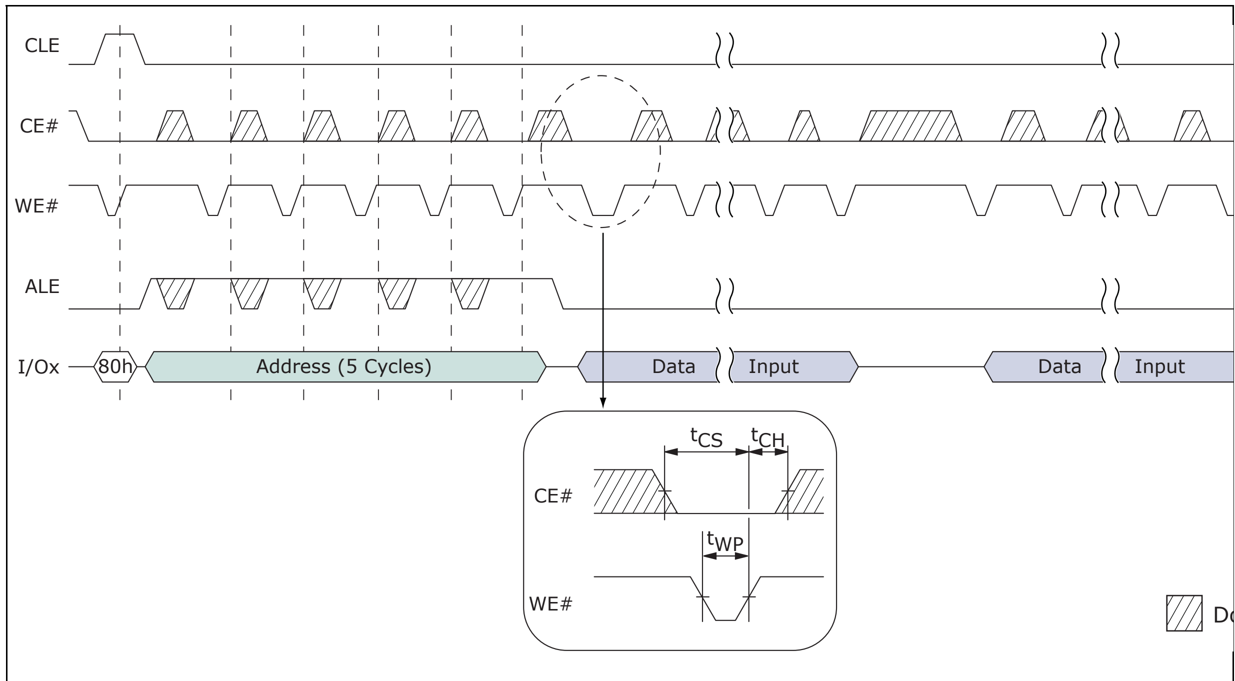
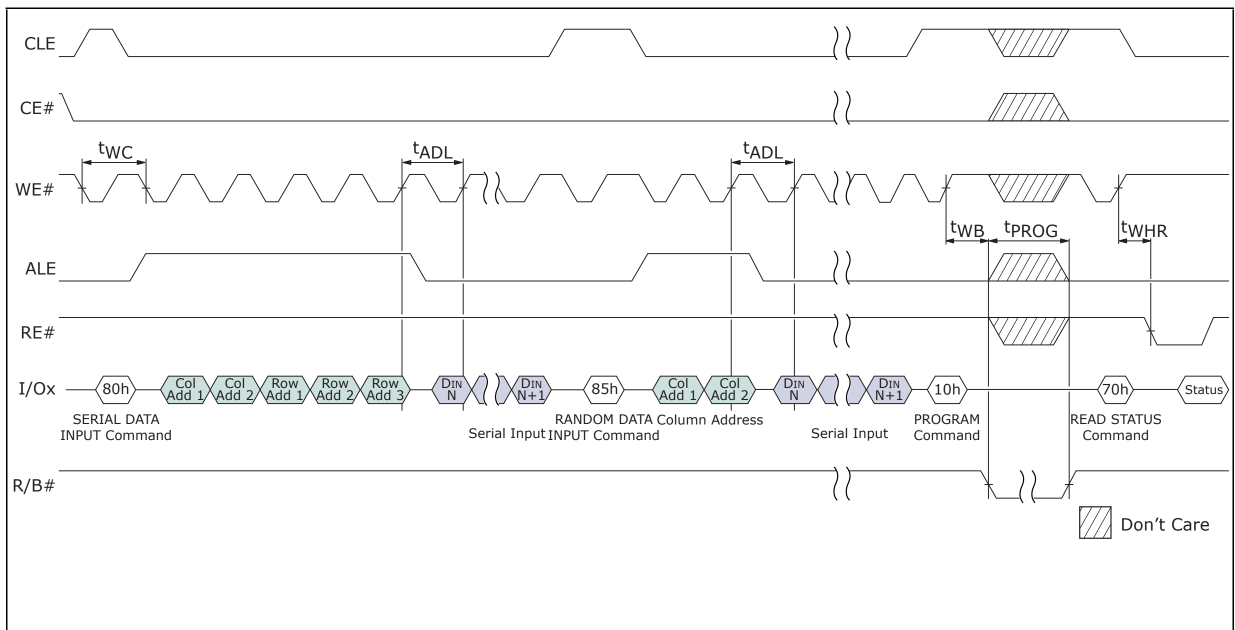


Figure 97. PAGE PROGRAM Operation with COPYBACK READ



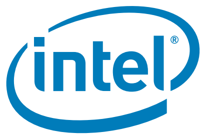


Figure 98. COPYBACK READ

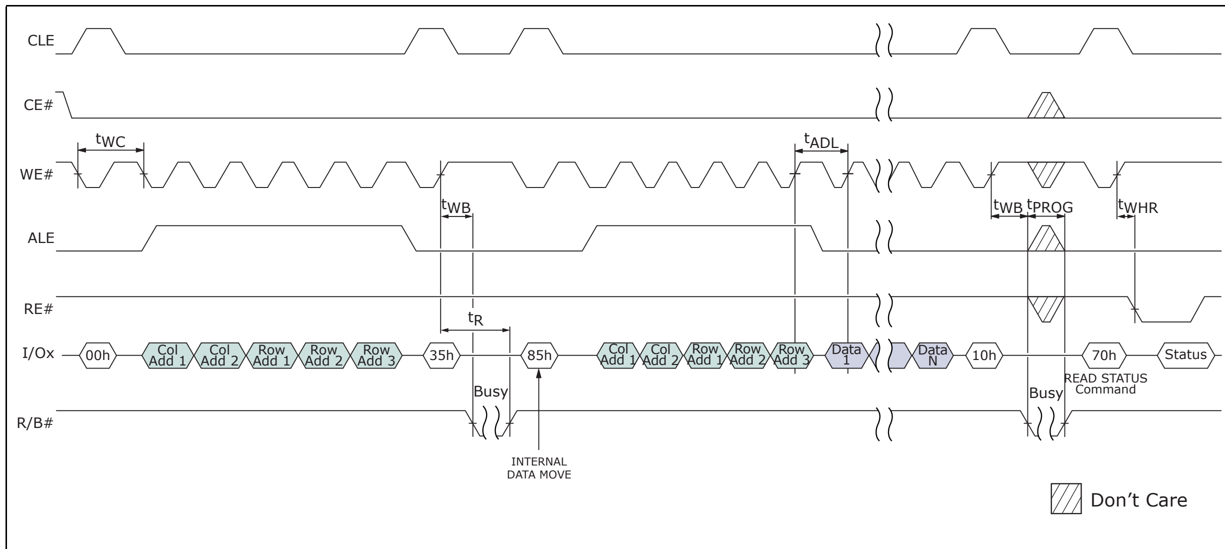
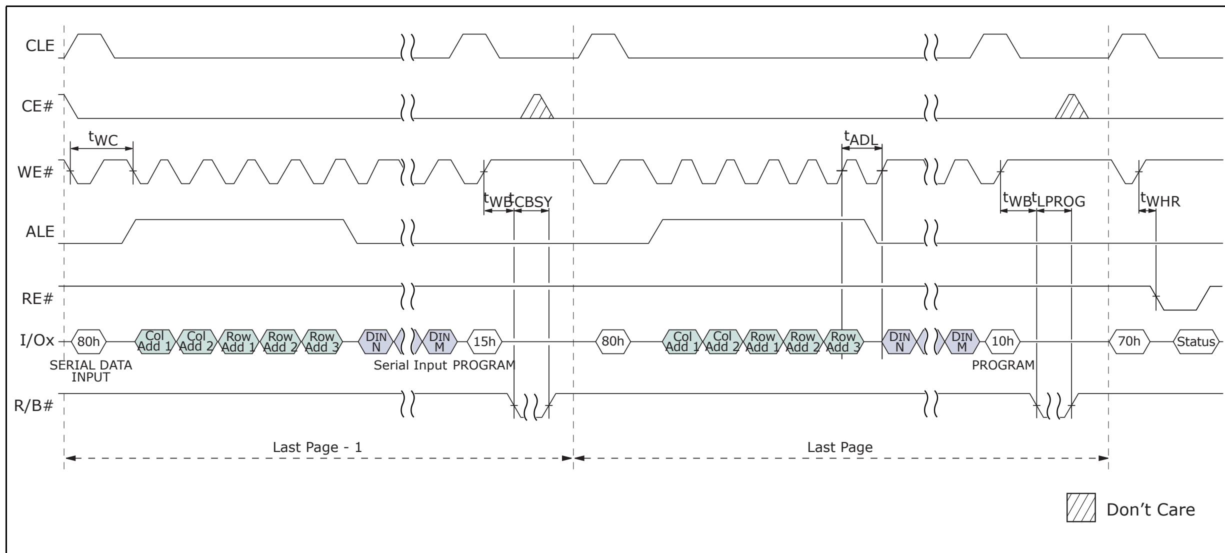


Figure 99. PAGE CACHE PROGRAM



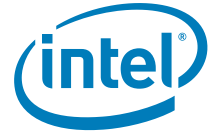


Figure 100. PAGE CACHE PROGRAM Ending on 15h

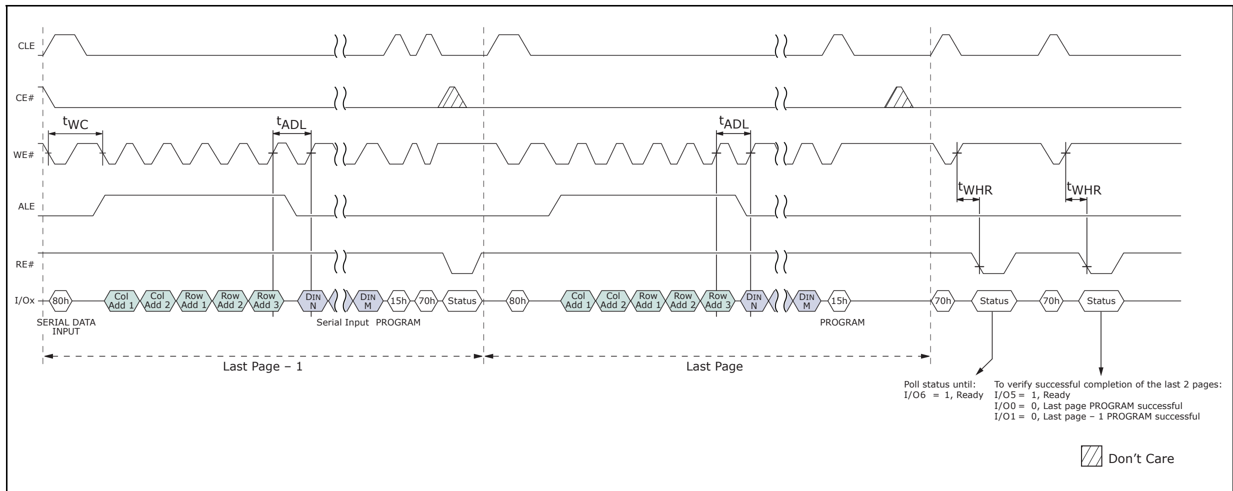


Figure 101. BLOCK ERASE Operation

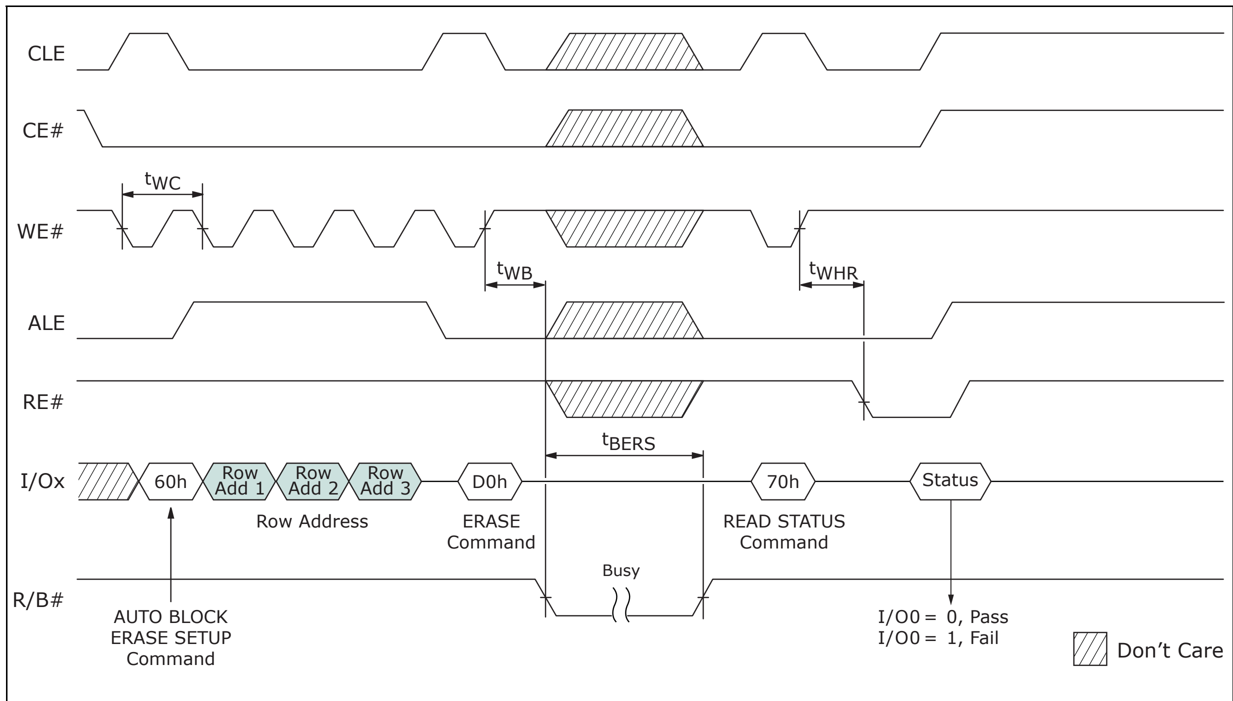
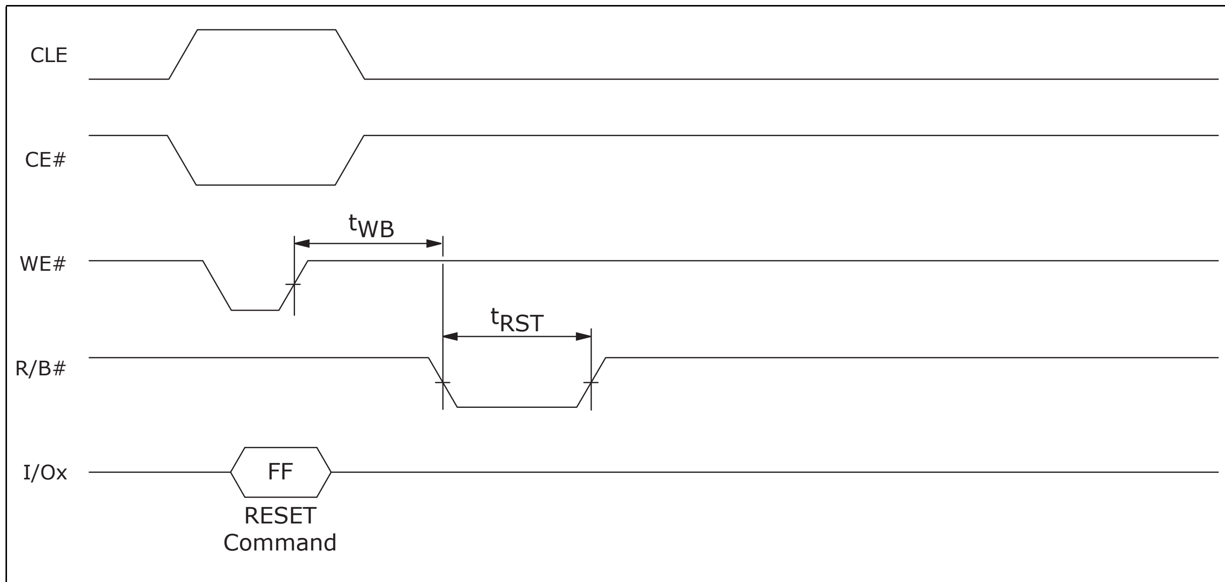


Figure 102. RESET Operation

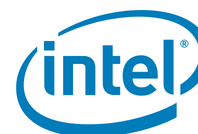


11.0 References

This document also references standards and specifications defined by a variety of organizations. Please use the following information to identify the location of an organization's standards information.

Table 26. Standards References

Date or Revision Number	Title	Location
February 2008	Open NAND Flash Interface Specification (ONFI) 2.0	http://www.onfi.org/docs/ONFI%202_0%20Gold.pdf



12.0 Glossary

This document incorporates many industry- and device-specific words. Use the following list to define a variety of terms and acronyms.

Table 27. Glossary of Terms and Acronyms

Term	Definition
DDP	Dual (2) Die Package
ECC	Error Correction Code
EDO	Extended Data Output
ONFI	Open NAND Flash Interface
QDP	Quad (4) Die Package
SDP	Single (1) Die Package
TSOP	Thin Small-Outline Package

13.0 Revision History

Date	Revision	
May 2009	002	Changed document status from "Advance" to "Preliminary". Updated cover page with new product names. Revised Section 7.9.1, "BLOCK ERASE 60h-D0h" on page 47 with new product name. Updated the following graphics with the new product names: • "Decoder" figure on page 2 • Figure 4, "SDP TSOP Configuration" on page 10 • Figure 5, "DDP TSOP Configuration" on page 10 • Figure 6, "QDP TSOP Configuration" on page 11 Updated the following tables with the new product names: • "Intel® NAND Flash memory Ordering Information" table on page 2 • Table 10, "Read Parameter Data Structure" on page 24 • Table 20, "Valid Blocks" on page 86 • Table 22, "Test Conditions" on page 87
March 2009	001	Initial release.