

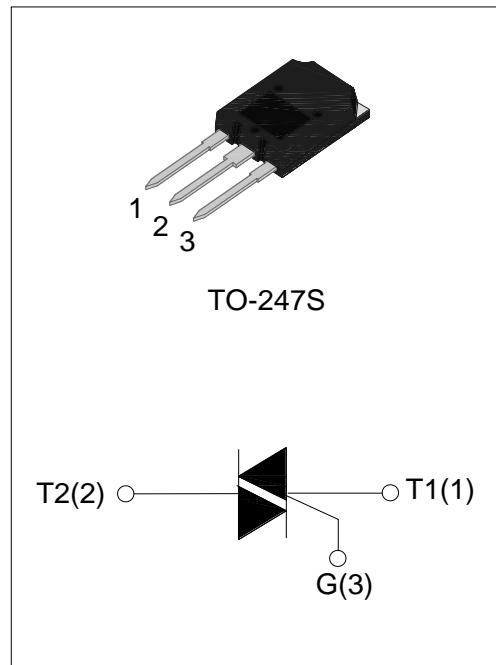


JST80 Series 80A TRIACs

Rev.2.0

DESCRIPTION:

JST80 series triacs, with high ability to withstand the shock loading of large current, provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrants products especially recommended for use on inductive load.



MAIN FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	80	A
V_{DRM}/V_{RRM}	1000/1200/1600	V
V_{TM}	1.55	V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Storage junction temperature range	T_{stg}	-40-150	°C
Operating junction temperature range	T_j	-40-125	°C
Repetitive peak off-state voltage ($T_j=25^\circ\text{C}$)	V_{DRM}	1000/1200/1600	V
Repetitive peak reverse voltage ($T_j=25^\circ\text{C}$)	V_{RRM}	1000/1200/1600	V
Non repetitive surge peak Off-state voltage	V_{DSM}	$V_{DRM}+100$	V
Non repetitive peak reverse voltage	V_{RSM}	$V_{RRM}+100$	V
RMS on-state current TO-247S ($T_C=70^\circ\text{C}$)	$I_{T(RMS)}$	80	A
Non repetitive surge peak on-state current (full cycle, $F=50\text{Hz}$)	I_{TSM}	800	A
I^2t value for fusing ($t_p=10\text{ms}$)	I^2t	3200	A^2s
Critical rate of rise of on-state current ($I_G=2 \times I_{GT}$)	dl/dt	100	$\text{A}/\mu\text{s}$
Peak gate current	I_{GM}	8	A
Average gate power dissipation	$P_{G(AV)}$	2	W
Peak gate power	P_{GM}	10	W

ELECTRICAL CHARACTERISTICS ($T_j=25^\circ\text{C}$ unless otherwise specified)

Symbol	Test Condition	Quadrant		Value	Unit
I_{GT}	$V_D=12V$ $R_L=33\Omega$	I - II -III	MAX	50	mA
V_{GT}		I - II -III	MAX	1.3	V
V_{GD}	$V_D=V_{DRM}$ $T_j=125^\circ\text{C}$ $R_L=3.3K\Omega$	I - II -III	MIN	0.2	V
I_L	$I_G=1.2I_{GT}$	I -III	MAX	80	mA
		II		120	
I_H	$I_T=100\text{mA}$		MAX	60	mA
dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^\circ\text{C}$		MIN	1000	V/ μs
(dV/dt)c	Without snubber $T_j=125^\circ\text{C}$		MIN	20	V/ μs

STATIC CHARACTERISTICS

Symbol	Parameter		Value(MAX)	Unit
V_{TM}	$I_{TM}=120\text{A}$	$tp=380\mu\text{s}$	$T_j=25^\circ\text{C}$	1.55 V
I_{DRM}			$T_j=25^\circ\text{C}$	50 μA
I_{RRM}	$V_D=V_{DRM}$	$V_R=V_{RRM}$	$T_j=125^\circ\text{C}$	10 mA

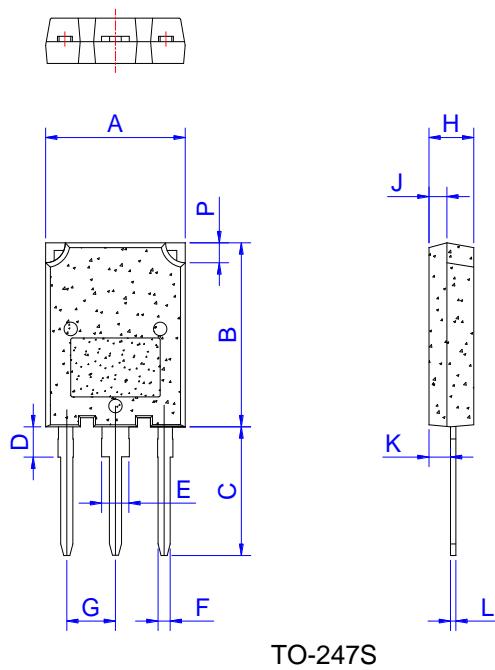
THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	junction to case(AC)	TO-247S	0.45	$^\circ\text{C}/\text{W}$

ORDERING INFORMATION

J	ST	80	CS	-1200	BW
JieJie Microelectronics Co.,Ltd					<u>$BW:I_{GT3} \leq 50\text{mA}$</u>
	Triacs				
		<u>$I_{T(\text{RMS})}:80\text{A}$</u>			
			CS:TO-247S		
				1000: $V_{DRM}/V_{RRM} \geq 1000\text{V}$	
				1200: $V_{DRM}/V_{RRM} \geq 1200\text{V}$	
				1600: $V_{DRM}/V_{RRM} \geq 1600\text{V}$	

PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.1		16.1	0.594		0.634
B	19.8		20.8	0.78		0.819
C	13.8		14.8	0.543		0.583
D	3.00		4.00	0.118		0.157
E	2.75		3.35	0.108		0.132
F	1.30		1.50	0.051		0.059
G	5.10		5.80	0.201		0.228
H	4.50		5.50	0.177		0.217
J	1.45		2.15	0.057		0.085
K	1.90		2.80	0.075		0.110
L	0.55		0.80	0.022		0.031
P	2.00		2.40	0.079		0.094

FIG.1 Maximum power dissipation versus RMS on-state current

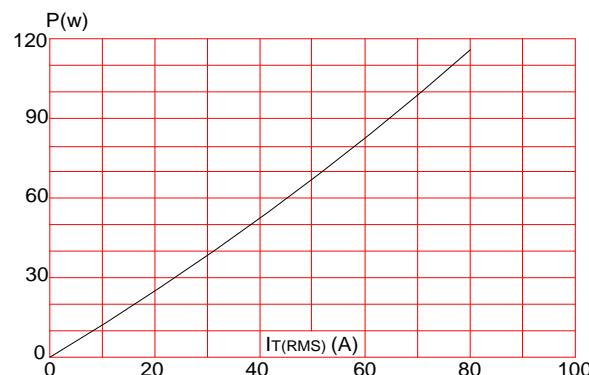


FIG.3: Surge peak on-state current versus number of cycles

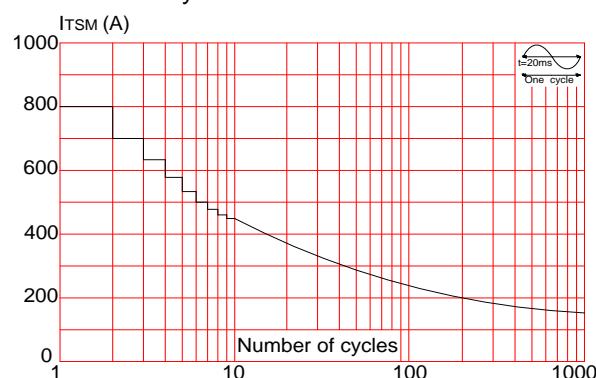


FIG.2: RMS on-state current versus case temperature

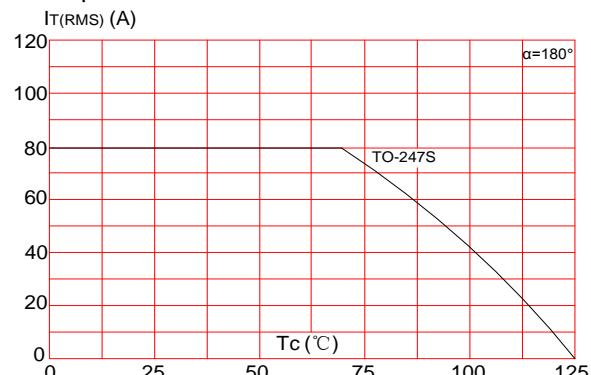


FIG.4: On-state characteristics (maximum values)

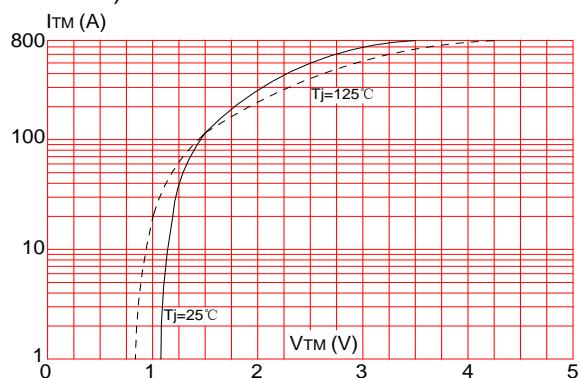




FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$, and corresponding value of I^2t ($dI/dt < 100\text{A}/\mu\text{s}$)

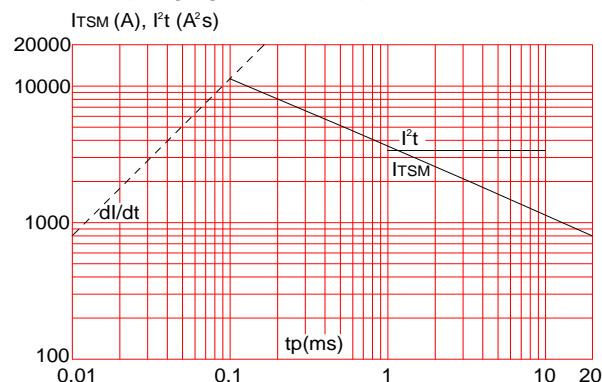
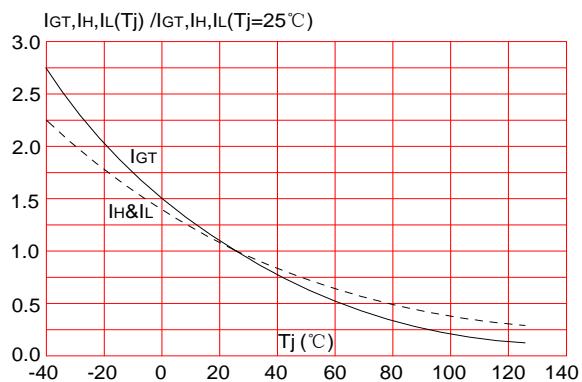


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document is the second version which is made in 25-Nov.-2014. This document supersedes and replaces all information previously supplied.



is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.

Copyright ©2014 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.