TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

J T M P 0 3 6 0 - 0 0 2 S

LSI for LCD Watches

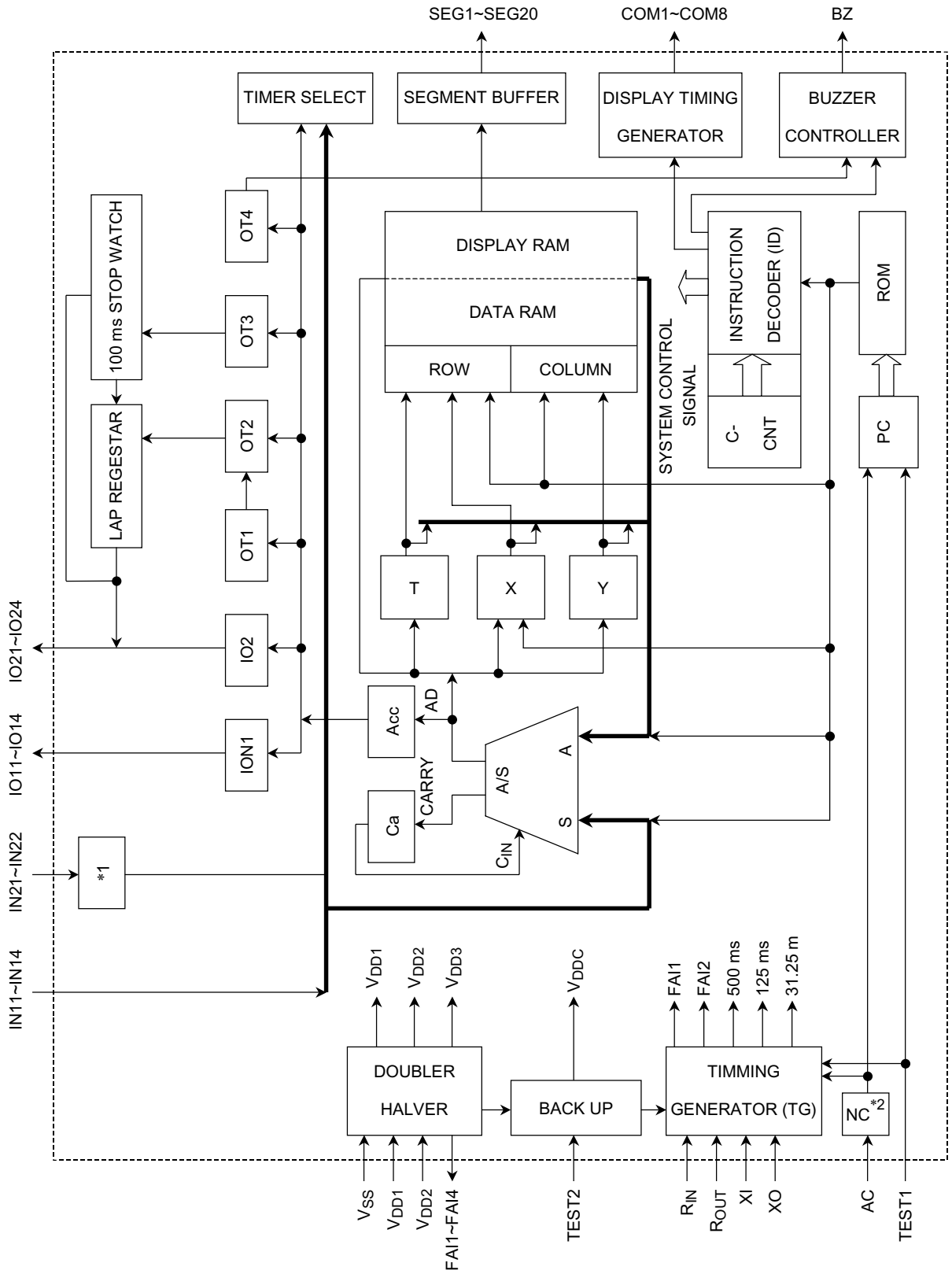
1. Summary

The JTMP0360-002S is a low-power LSI for watches with chronograph functions. This LSI features a chronograph, lap memory, an alarm function, and a built-in LCD driver.

1.1 Feature

- Bar graph chronograph and elapsed time displays
- Lap memory (max 10 laps)
- Lap/split time selectable
- 3.0 V single power supply
- Alarm/time signal function
- 12/24-hour display selectable

1.2 Block Diagram



*1: Anti-chattering circuit

*2: Noise Canceller

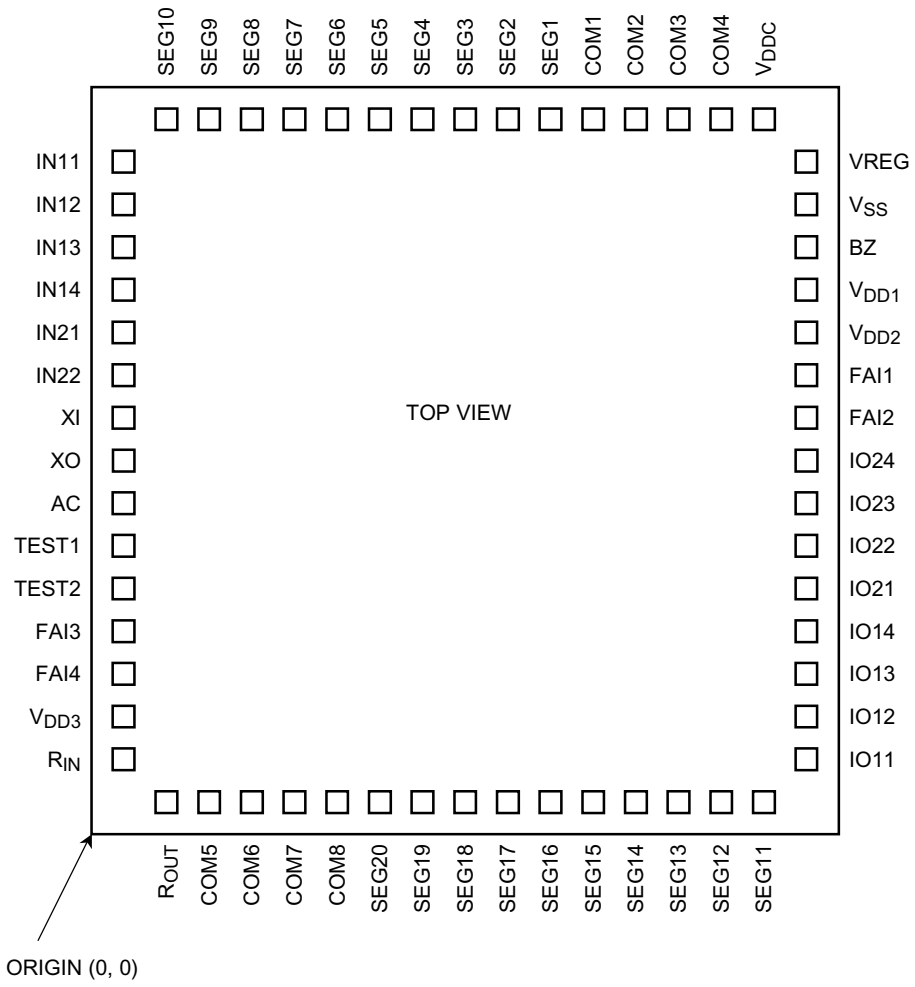
1.3 Pin Description (60 pins)

Pin Name	Symbol	No. of Pins
Power supply pin	V_{DD1}, V_{DD2}, V_{DD3}, V_{DDC}, V_{SS}, VREG	6
Oscillator pin	XI, XO, R_{OUT}, R_{IN}	4
Input pin	IN11~14, IN21, IN22, AC	7
Output pin	BZ	1
Display Pin	COM1~8, SEG1~20	28
Input/output pin	IO11~14, IO21~24	8
Test pin	TEST1, TEST2	2
Voltage doubler/halver pin	FAI1~4	4

1.4 Description of Functions

Pin Name	Function
XI, XO R_{OUT}, R_{IN}	Connects low-speed clock oscillator crystal
IN11~IN14 IN21, IN22	6-bit input pin. When input to the accumulator, only four bits can be read simultaneously.
IO11~IO14 IO21~IO24	Input/output ports with output latch
BZ	Mainly for buzzer, alarm, and time signal output
FAI1~FAI4	For 0.1 μF voltage doubler/halver capacitor connection
VREG	—
TEST1, TEST2	For testing (by Toshiba) at shipping. Fix to LOW.
AC	For system setting
V_{SS} V_{DD1} V_{DD2} V_{DD3} V_{DDC}	0 V (GND) Connects to V_{SS} via 0.1 μF capacitor (1.5 V at voltage step-down) 3 V Connects to V_{SS} via 0.1 μF capacitor (3.0 V at voltage step-down) Connects to V_{SS} via 0.1 μF capacitor
SEG1~20	Outputs segment signals
COM1~8	Outputs common signals

1.5 Pad Layout



Chip size: 3.52 × 3.33 (mm)
Chip thickness: 440 ± 30 (μm)

1.6 Pad Location Table

(μm)

IN11	(	168,	2784)
IN12	(	168,	2624)
IN13	(	168,	2439)
IN14	(	168,	2279)
IN21	(	168,	2119)
IN22	(	168,	1959)
XI	(	168,	1799)
XO	(	168,	1639)
AC	(	168,	1479)
TEST1	(	168,	1319)
TEST2	(	168,	1159)
FAI3	(	168,	966)
FAI4	(	168,	806)
V_{DD3}	(	168,	646)
R_{IN}	(	168,	403)

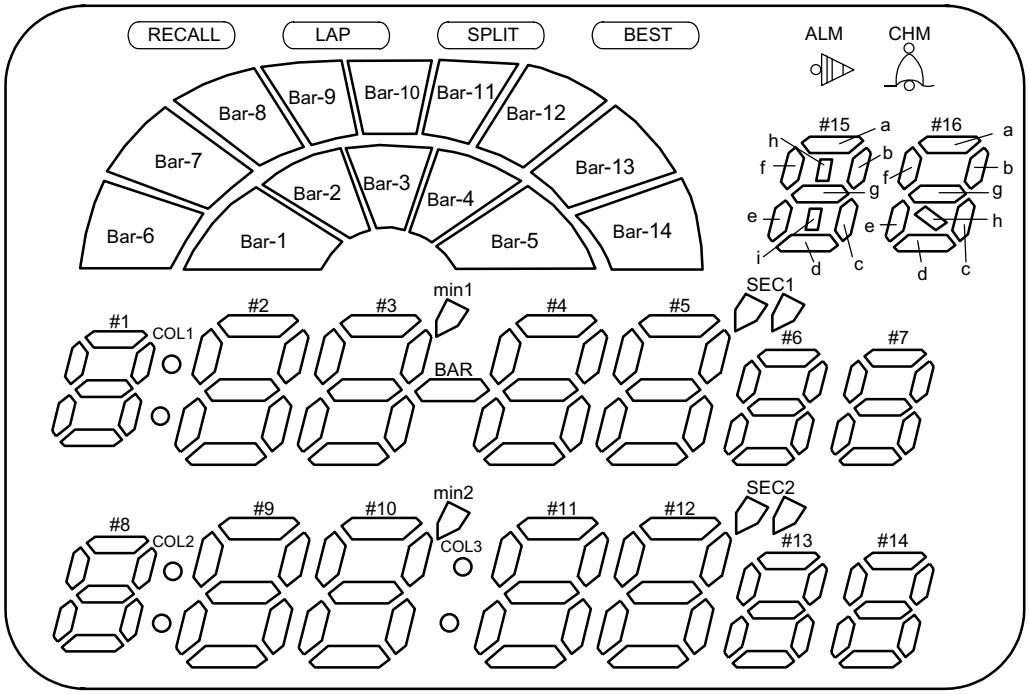
IO11	(	3270,	435)
IO12	(	3270,	595)
IO13	(	3270,	755)
IO14	(	3270,	915)
IO21	(	3270,	1075)
IO22	(	3270,	1235)
IO23	(	3270,	1395)
IO24	(	3270,	1555)
FAI2	(	3270,	1715)
FAI1	(	3270,	1875)
V_{DD2}	(	3270,	2035)
V_{DD1}	(	3270,	2195)
BZ	(	3270,	2355)
V_{SS}	(	3270,	2515)
VREG	(	3270,	2784)

R_{OUT}	(	444,	168)
COM5	(	654,	168)
COM6	(	864,	168)
COM7	(	1074,	168)
COM8	(	1283,	168)
SEG20	(	1443,	168)
SEG19	(	1603,	168)
SEG18	(	1763,	168)
SEG17	(	1923,	168)
SEG16	(	2083,	168)
SEG15	(	2243,	168)
SEG14	(	2403,	168)
SEG13	(	2563,	168)
SEG12	(	2723,	168)
SEG11	(	2883,	168)

V_{DDC}	(	2873,	3015)
COM4	(	2713,	3015)
COM3	(	2528,	3015)
COM2	(	2368,	3015)
COM1	(	2183,	3015)
SEG1	(	2023,	3015)
SEG2	(	1851,	3015)
SEG3	(	1691,	3015)
SEG4	(	1531,	3015)
SEG5	(	1371,	3015)
SEG6	(	1211,	3015)
SEG7	(	1051,	3015)
SEG8	(	891,	3015)
SEG9	(	731,	3015)
SEG10	(	571,	3015)

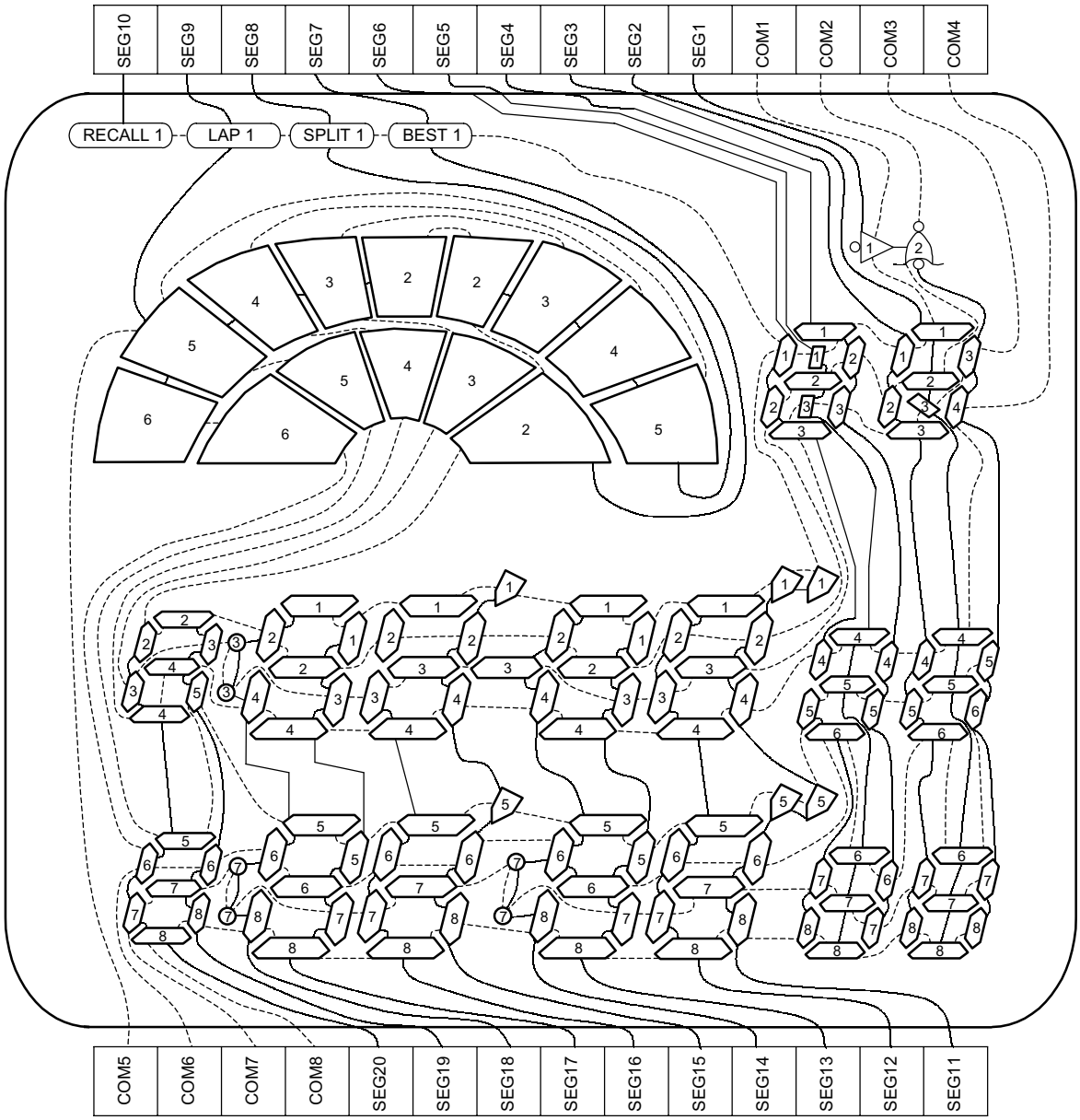
2. Function Specifications

2.1 Display configuration and segment symbols



	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
SEG1	ALM	CHM	#16-b	#16-c	#7-b	#7-c	#14-b	#14-c
SEG2	#16-a	#16-g	#16-h	#7-a	#7-g	#14-a	#14-g	#14-d
SEG3	#16-f	#16-e	#16-d	#7-f	#7-e	#7-d	#14-f	#14-e
SEG4	#15-a	#15-b	#15-c	#6-b	#6-c	#13-b	#13-c	—
SEG5	#15-h	#15-g	#15-i	#6-a	#6-g	#13-a	#13-g	#13-d
SEG6	#15-f	#15-e	#15-d	#6-f	#6-e	#6-d	#13-f	#13-e
SEG7	BEST	Bar-5	Bar-4	Bar-3	Bar-2	Bar-1	—	—
SEG8	SPLIT	Bar-11	Bar-12	Bar-13	Bar-14	—	—	—
SEG9	LAP	Bar-10	Bar-9	Bar-8	Bar-7	Bar-6	—	—
SEG10	RECALL	—	—	—	—	—	—	—
SEG11	SEC1	#5-b	#5-g	#5-c	SEC2	#12-b	#12-g	#12-c
SEG12	#5-a	#5-f	#5-e	#5-d	#12-a	#12-f	#12-e	#12-d
SEG13	#4-b	#4-g	#4-c	#4-d	#11-b	#11-g	#11-c	#11-d
SEG14	#4-a	#4-f	BAR	#4-e	#11-a	#11-f	COL3	#11-e
SEG15	min1	#3-b	#3-g	#3-c	MIN2	#10-b	#10-g	#10-c
SEG16	#3-a	#3-f	#3-e	#3-d	#10-a	#10-f	#10-e	#10-d
SEG17	#2-b	#2-g	#2-c	#2-d	#9-b	#9-g	#9-c	#9-d
SEG18	#2-a	#2-f	COL1	#2-e	#9-a	#9-f	COL2	#9-e
SEG19	—	#1-a	#1-b	#1-g	#1-c	#8-b	#8-g	#8-c
SEG20	—	#1-f	#1-e	#1-d	#8-a	#8-f	#8-e	#8-d

2.2 LCD connection diagram

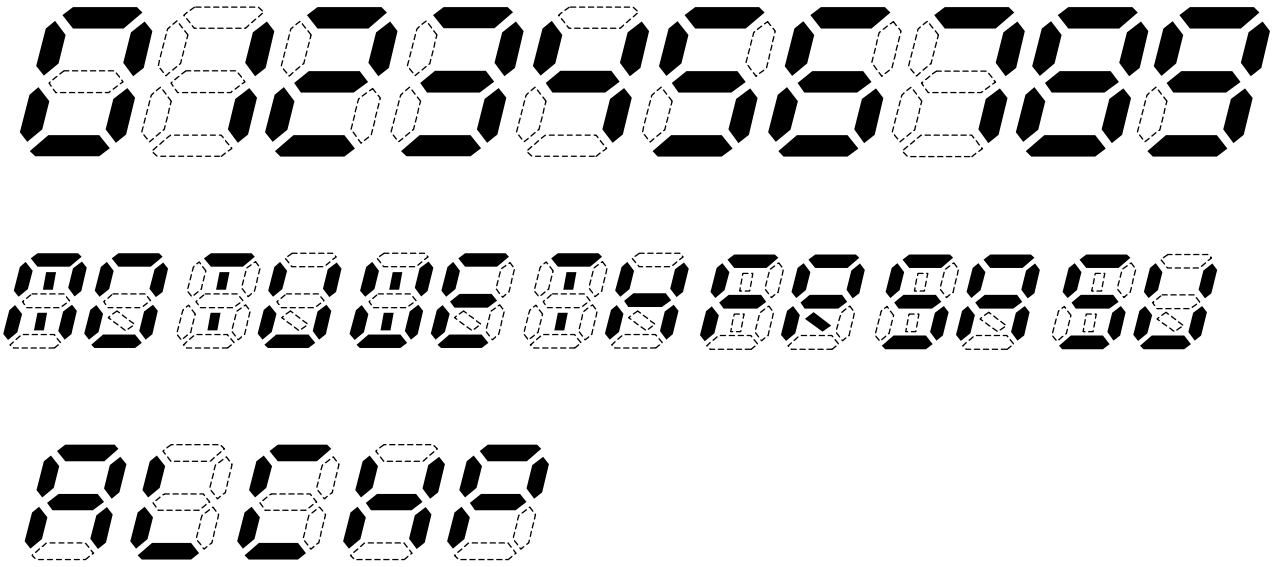


Note: The figures in the display are common numbers.

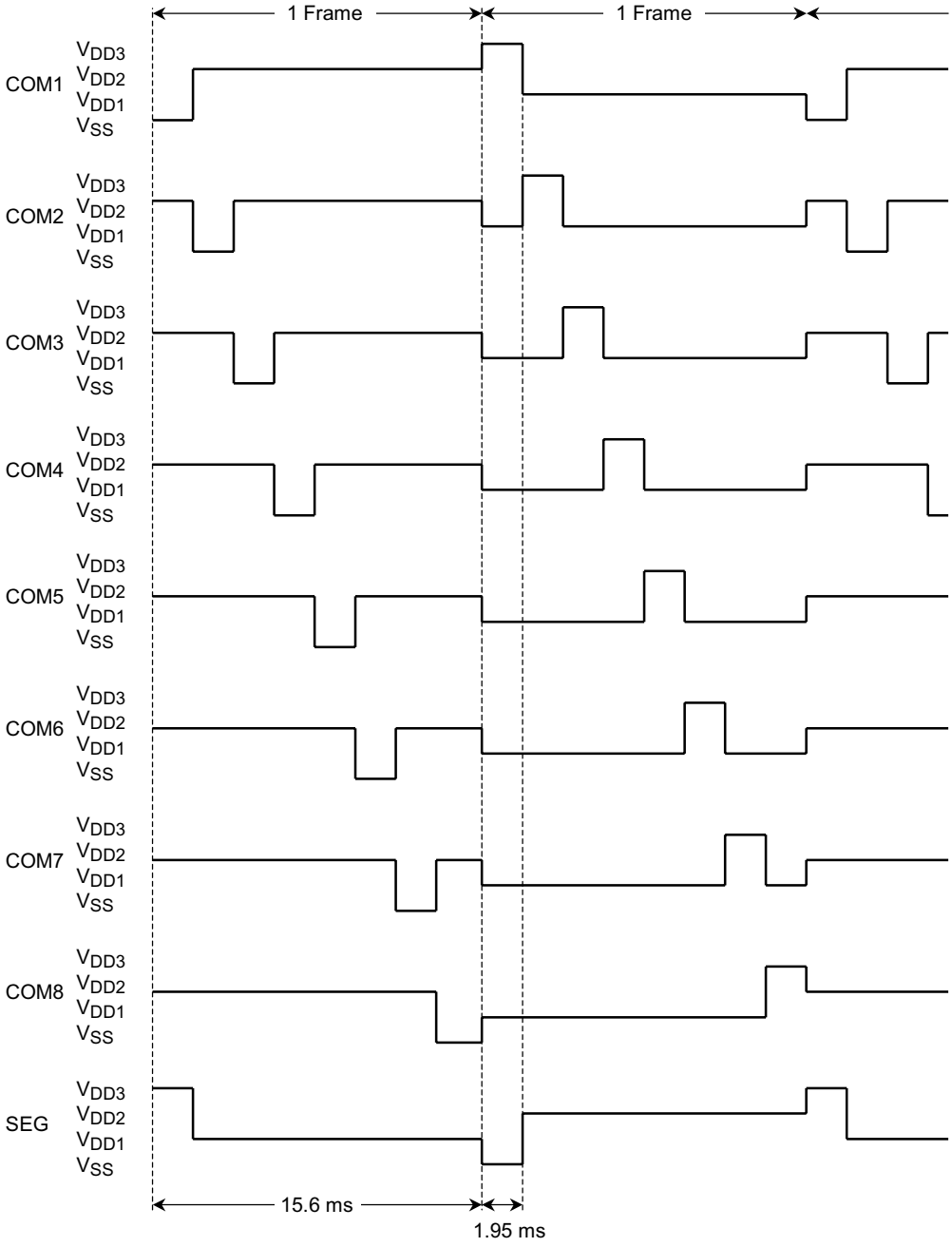
——— Segment

---------- Common

2.3 Liquid crystal display

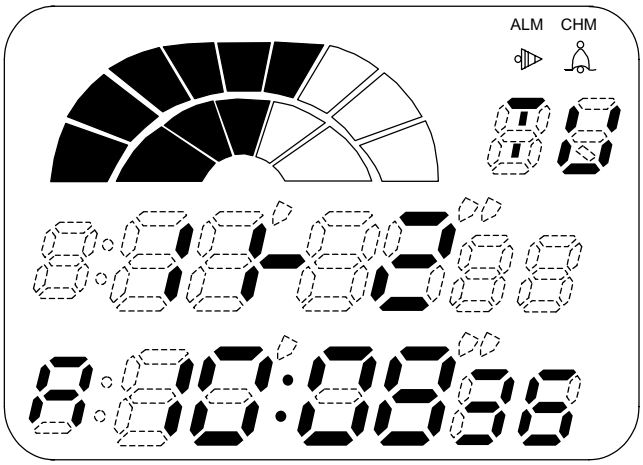


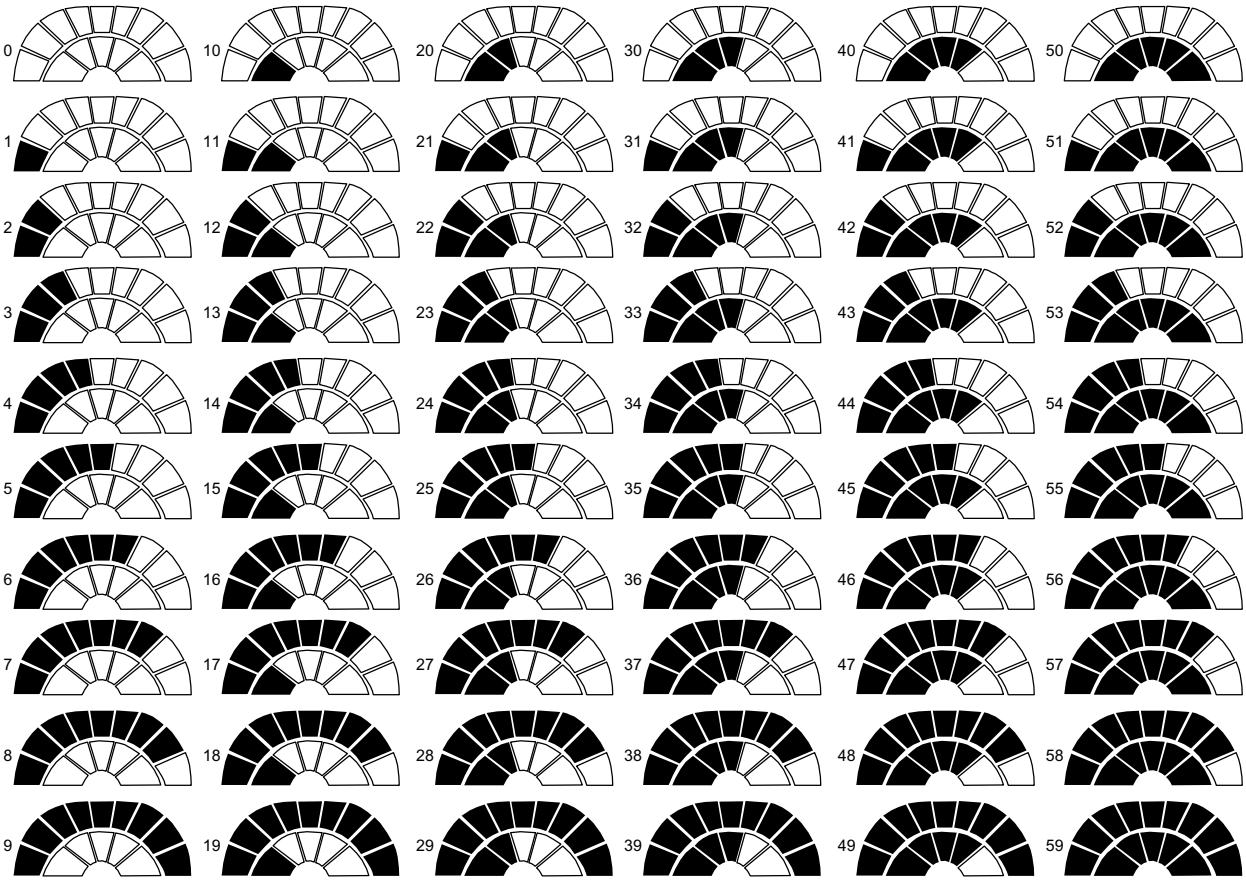
2.4 Liquid crystal drive wave forms



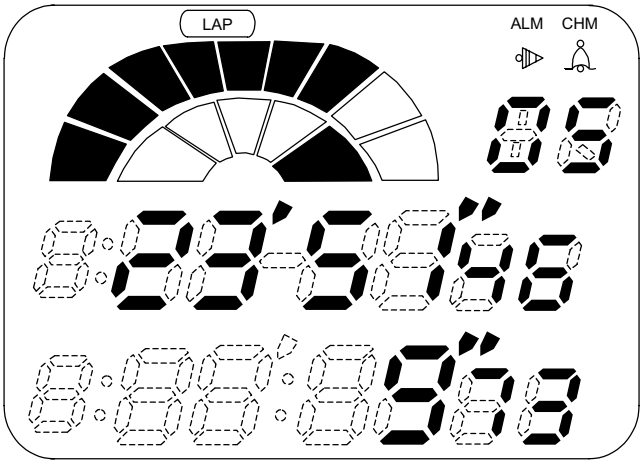
2.5 Display

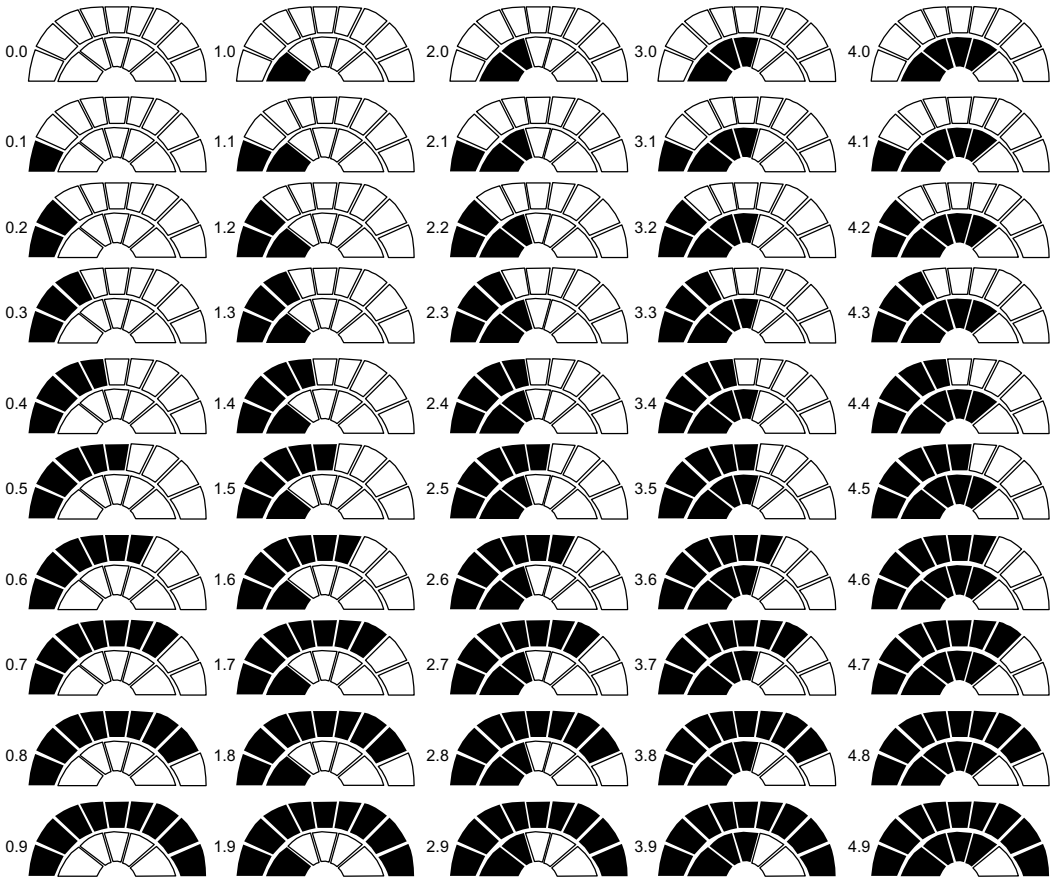
2.5.1 TIME mode display

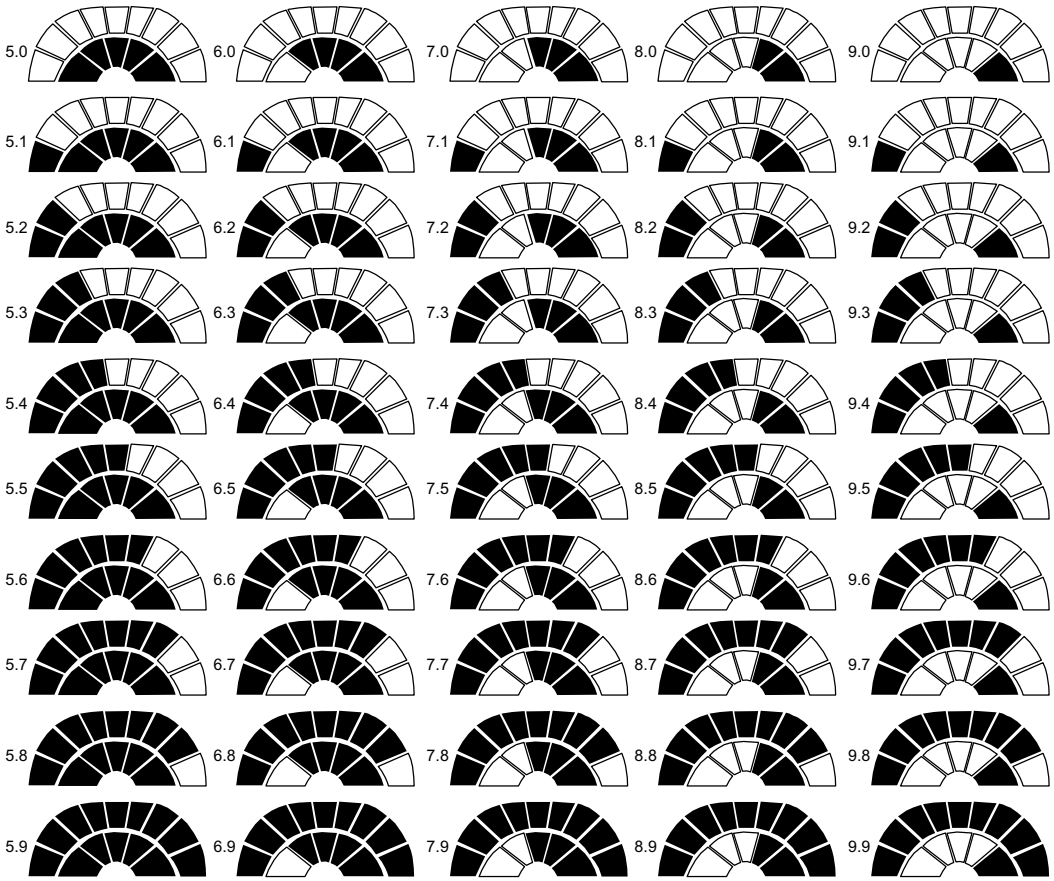




2.5.2 CHRONO mode display






5.0
6.0
7.0
8.0
9.0
5.1
6.1
7.1
8.1
9.1
5.2
6.2
7.2
8.2
9.2
5.3
6.3
7.3
8.3
9.3
5.4
6.4
7.4
8.4
9.4
5.5
6.5
7.5
8.5
9.5
5.6
6.6
7.6
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9.6
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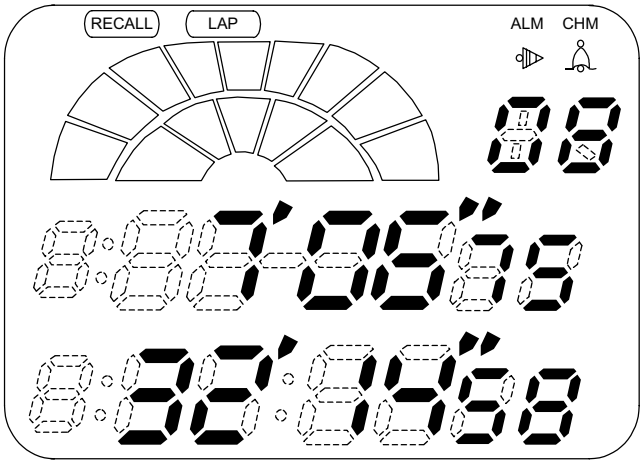
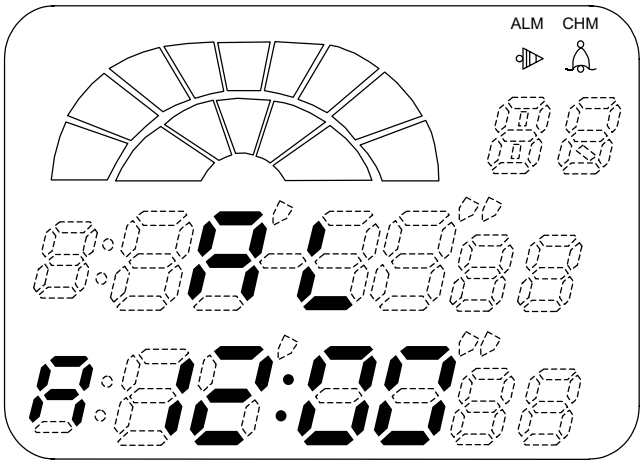
9.9

2.5.3 MEMORY RECALL mode display

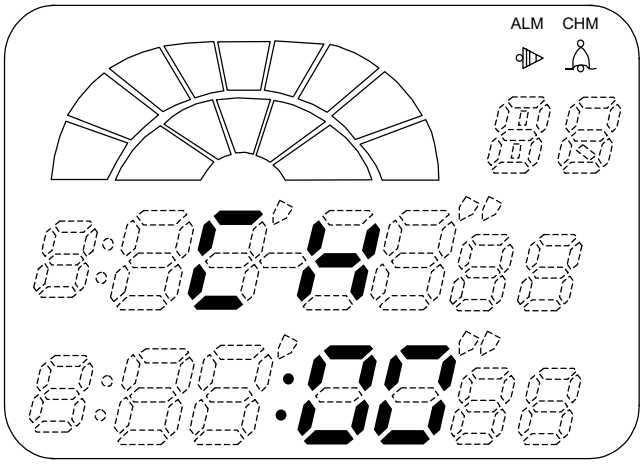


2.5.4 ALARM mode display

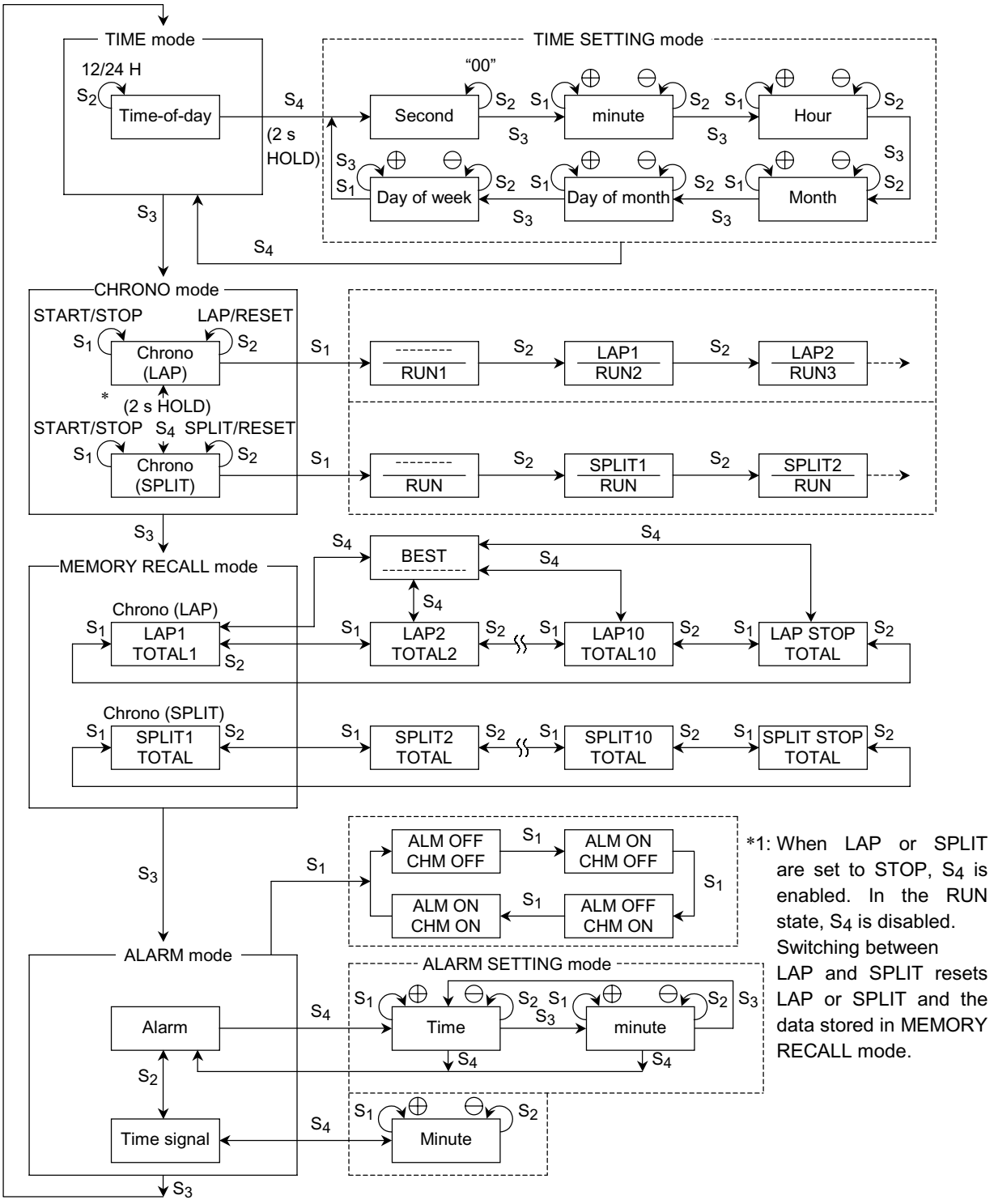
(1) Alarm display



(2) Time signal display



2.6 Mode transition diagram



*1: When LAP or SPLIT are set to STOP, S_4 is enabled. In the RUN state, S_4 is disabled. Switching between LAP and SPLIT resets LAP or SPLIT and the data stored in MEMORY RECALL mode.

Note: For S_1, S_2, S_3 and S_4, see the corresponding example circuit.

2.7 Mode description

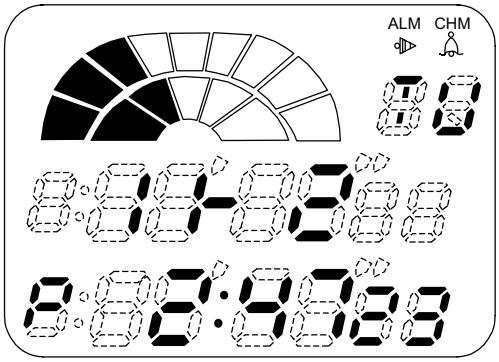
2.7.1 TIME mode

TIME mode is used to display the current time and make time settings.

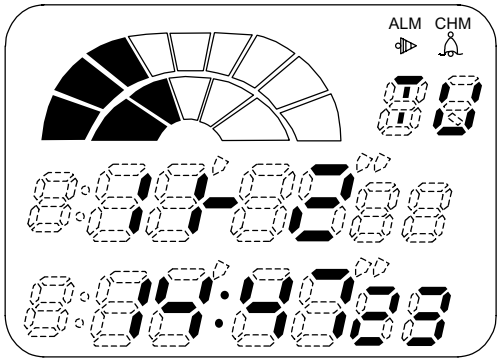
- Middle row columns #2 and #3 display the month, columns #4 and #5 display the day of the month with unnecessary zeros suppressed.
- Upper row columns #15 and #16 display the day of the week.
- Lower row column #8 displays AM/PM.
- Lower row columns #9 and #10 display the hour, columns #11 and #12 display minutes, and #13 and #14 display seconds.
- The ON/OFF states of the time signal and alarm are displayed in the upper right corner.
- When the alarm or time signal is set, the alarm or time signal sign in the top row flashes. When the LAP or SPLIT functions are running in CHRONO mode, the LAP or SPLIT signs flash.
- Pressing multiple switches simultaneously invalidates the switches pressed.
- Pressing a second switch while still pressing the first invalidates both switches.
- S_2 can be used to switch between a 12-and 24-hour clock. Such switching can only be performed in TIME mode.

<Display example>

(a) 12-hour clock



(b) 24-hour clock

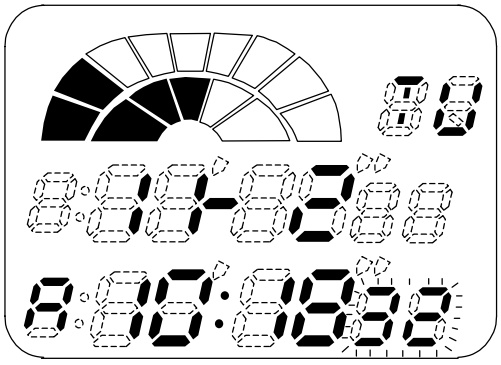


2.7.2 TIME SETTING mode

- Access TIME SETTING mode by pressing S_4 for two seconds in TIME mode.
- Pressing S_3 in TIME SETTING mode displays in turn the seconds, the minutes, the hour, the month, the day of the month, the day of the week, then the seconds again. Set each while it is flashing.
- In TIME SETTING mode, the ALM/CHM signs turn OFF and the sound is disabled even if they were set ON before entering TIME SETTING mode. When returning from TIME SETTING mode to TIME mode, the ALM/CHM sign returns to the status before the switch to TIME SETTING mode.
- In TIME SETTING mode, pressing S_4 switches to TIME mode. S_4 can be pressed from the second, minute, month, day of the month, or day of the week displays.
- If any switch is not pressed for one minute in TIME SETTING mode, the device automatically switches to TIME mode.
- Pressing multiple switches simultaneously invalidates the switches pressed.
- Pressing a second switch while still pressing the first invalidates both switches.

<Display example>

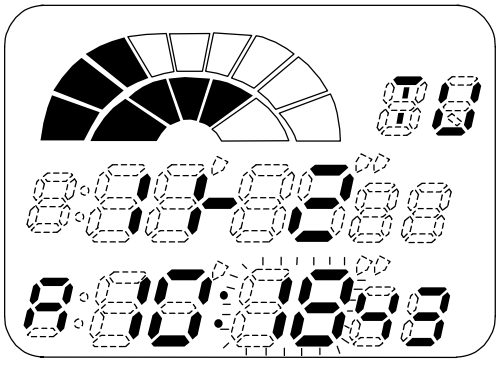
(a) Setting the seconds



- Pressing S_2 swich seconds display is 0-29, the seconds are simply set to "00". If the seconds display is 30-59, the seconds are simply set to "00" and one minute is incremented.

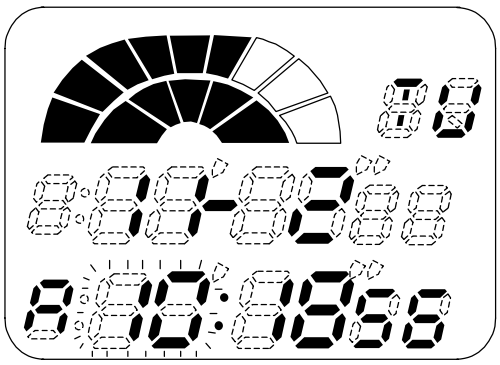
  *: S_1 is invalid

(b) Setting the minutes



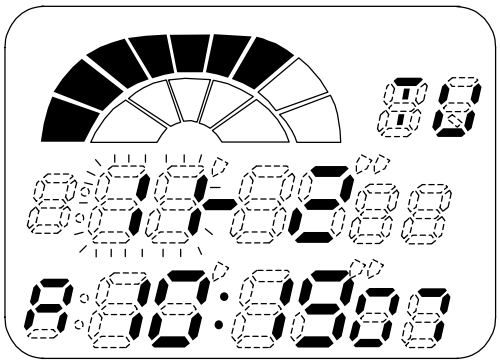
- Use S_1 or S_2 to set the minutes. Each press of S_1 increments the time by one minute. Pressing S_2 decrements the time by one minute. Pressing either S_1 or S_2 for two seconds fast-winds the time at a speed of 4 Hz for as long as the switch is depressed. Pressing another switch during the fast winding immediately cancels the fast winding.
  To return to fast winding, press S_1 or S_2 as above after releasing all other switches.
- The count range is 0~59.

(c) Setting the hour



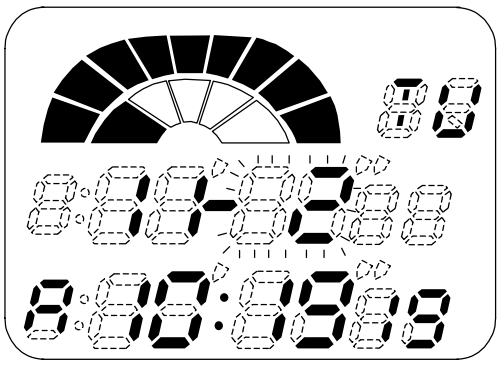
- Use S_1 and S_2 to set the hour as in "Setting the minutes".
  Displays the range:
  For 12-hour clock
  → AM12~11↔ PM12~11←
  For 24-hour clock
  → 0~23←

(d) Setting the month



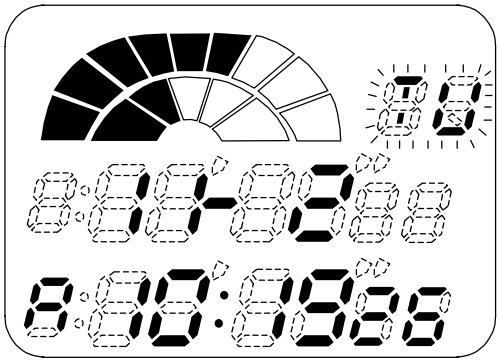
- Use S_1 or S_2 to set the month as in "Setting the minutes".
  Displays the range:
  → 1~12 ←

(e) Setting the day of the month



- Use S_1 and S_2 to set the day of the month as in "Setting the minutes".
  For January, March, May, July, August, October, and December, the range displayed is:
  → 1~31 ←
  For April, June, September, and November, the range displayed is:
  → 1~30 ←
  For February, the range displayed is:
  → 1~29 ←

(f) Setting the day of the week



- Use S_1 or S_2 to correct the month as in "Correcting the minutes".
  Displays the range:
  → SU~SA←

*: TIME SETTING mode can display some days of the month that do not actually exist (February 30, February 31, April 31, June 31, September 31, November 31). When switching from TIME SETTING mode to TIME mode, the first day of the following month is displayed.

(Example) February 30 in TIME SETTING mode,

S_4 ↓

becomes March 1 in TIME mode.

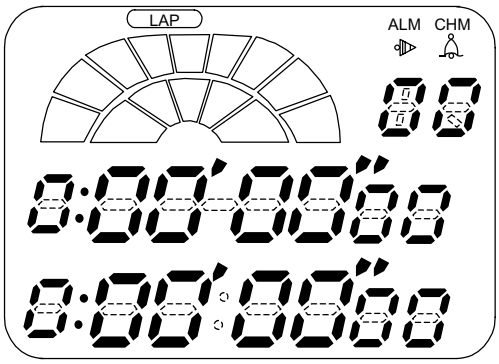
2.7.3 CHRONO mode

CHRONO mode displays lap and split time.

- Middle and lower row columns #1 and #8 display the hour; columns #2 and #3, and #9 and #10 display the minutes ; columns #4 and #5, and #11 and #12 display the seconds; columns #6 and #13 display tenths of seconds ; and columns #7 and #14 display hundredths of seconds.
- The middle row displays lap and split time.
- Upper row columns #15 and #16 display the lap or split count number.
- The lower row displays the RUN time.
- Clocking is up to 9 hours, 59 minutes, 59 seconds, 99 hundredths of seconds.
- In the RUN state, after 9 hours and 59 minutes, 59 seconds, and 99 hundredths of seconds, the count-up returns to 0, but because of zero suppression, the counting starts from display of a single zero.
- Displays the ALM/CHM ON/OFF status.
- In CHRONO mode, a switch-push sound is generated when S_1 or S_2 are pressed. In the case of S_4, the sound is generated after S_4 is held for two seconds.
- To switch between lap and split, depress S_4 for two seconds. This resets the lap or split display. (Switching is indicated by the switch-push sound. Lap/split switching also resets the data stored in MEMORY RECALL mode.
  During the RUN state, S_4 is invalid and cannot be used for switching.
- The lap/split count number starts from 01. When 99 is reached, the count returns to 00. This cycle is repeated indefinitely.
- After an ALL CLEAR in CHRONO mode, the LAP mode reset state is displayed.
- If other switches are pressed at the same time as S_1, S_1 takes precedence.
- Pressing switches other than S_1 at the same time invalidates the switches pressed.
- Pressing a second switch while still pressing the first, unless the first switch is S_1, invalidates both switches.

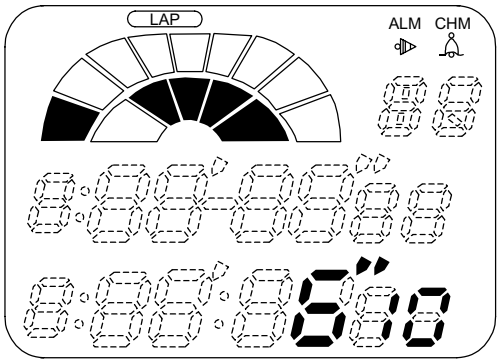
(1) LAP mode display

(a) Reset state



- In LAP mode, after a reset and in a state other than RUN, the display is as at left.
- The LAP sign at the top of the display is lit.

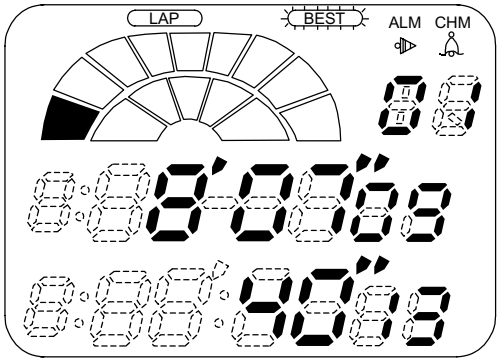
(b) RUN 1 state Lap 0



- Pressing S_1 sets the watch to RUN.
  The RUN state is displayed (zero suppressed) in the lower row. The graphic display in the upper row functions at the same time.
- As long as lap time is not recorded, the middle row display is blank.

  *: Once a digit is displayed in this column, the digit will not be zero suppressed. However, pressing S_2 (lap) resets and zero suppresses the lower row.

(c) RUN 2 state Lap 1

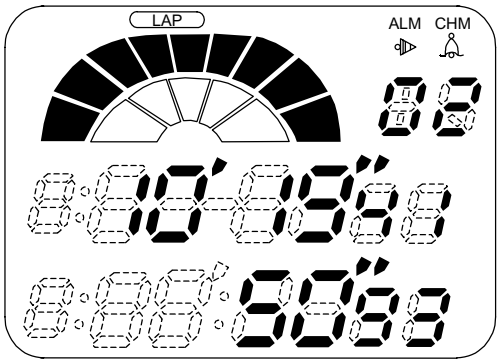


- In lap 0, RUN 1 state, pressing S_2 displays the lap time in the middle row, and the lap number at the far right of the upper row. Also, pressing S_2 in lap 0, RUN 1 state resets the time display in the lower row and starts the count from 0.
- If lap time is measured when no other lap time is recorded, the lap time recorded is the "best lap" time, and the best lap function is activated.

If another lap time is recorded, it is compared to the current best time. If the lap time is shorter than the current best lap time, the best lap function is activated. If the lap time is longer than the current best lap time, the best lap function is not activated. If the lap time is the same as the current best lap time, the lap time recorded first remains the best lap time. Therefore, where same lap times are recorded, the best lap function is not activated.

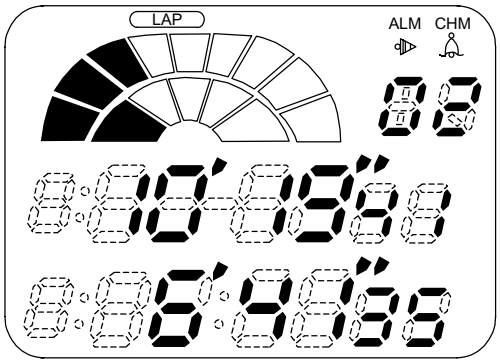
*: Best lap function
The best lap is the fastest lap.
When a best lap time occurs, the BEST sign in the top row flashes at 2 Hz, and the best time sound is output. While the best lap time remains displayed in the middle row, the BEST sign in the top row continues flashing.

(d) RUN 3 state Lap 2



- Compares the best lap time with the current lap. Because the current lap time is longer, the BEST sign is not lit.

(e) RUN 3 stop state



- Pressing S1 stops the RUN state.
- Even if the time to when the count stops is shorter than the best time, that time is ignored because it is not a full lap time.

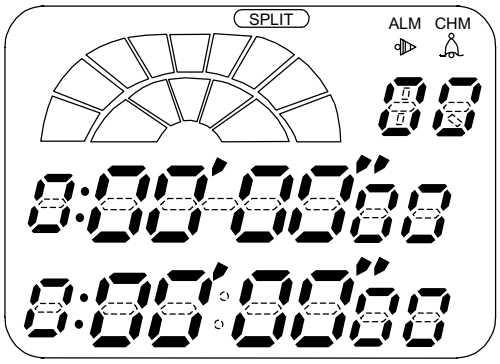
*: Even if the count is stopped with the BEST sign still flashing, the BEST sign continues to flash. If the count is restarted, the BEST sign continues flashing because the best lap time is displayed in the middle row.

*: During best time sound output (during RUN state)

- If the count is stopped by pressing S_1, the S_1 switch-push sound takes precedence. If the best time sound is ON, it stops immediately.
- If the lap is recorded using S_2, the S_2 switch-push sound takes precedence. If the best time sound is ON, it stops immediately.
- If the lap is recorded using S_2 and that lap time is a best time, the S_2 switch-push sound takes precedence. If the best time sound is ON, it stops immediately, then starts again after the S_2 switch-push sound ends.
- If the mode is switched using S_3, the switch-push sound is not output. However, the best time sound stops immediately and the device switches to MEMORY RECALL mode.
- Except for pressing S_4 and S_1 together, pressing more than one switch at the same time invalidates both switches. Therefore, the best time sound continues.

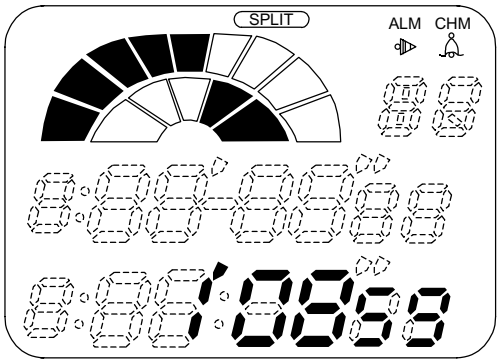
(2) SPLIT mode display

(a) Reset state



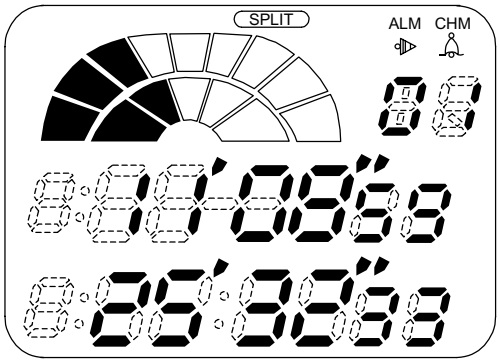
- Executing a reset in SPLIT mode produces the display shown at left.

(b) RUN state Split 0



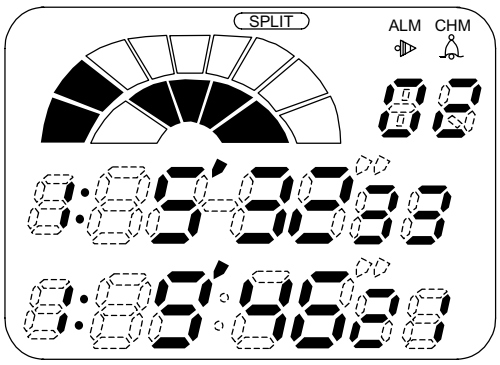
- Pressing S_1 sets the device to RUN and displays the RUN count in the lower row. The upper row graphic display comes on at the same time. (The lower row RUN count display is zero suppressed.)

(c) RUN state Split 1



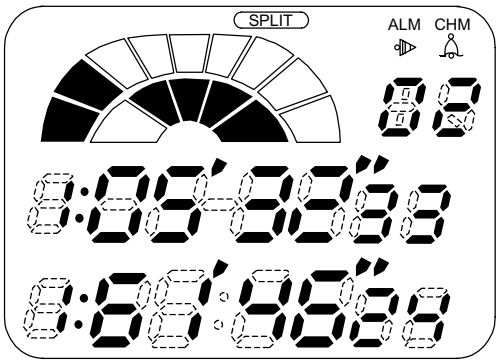
- Pressing S_2 in RUN split 0 state displays the time elapsed as split time in the middle row, and displays the split number at the right end of the upper row.

(d) RUN state Split 2



- Split 2 functions the same as RUN split 1. Pressing S_2 updates the time displayed in the middle row with the time elapsed from start, which becomes the new split time, and displays the split number at the right end of the upper row.

(e) RUN stop state



- Pressing S_1 stops the RUN count.
- Pressing S_2 after stopping the RUN count displays the reset state.

*: The RUN time displayed in the lower row in SPLIT mode is not reset when split data is recorded. Once a digit is displayed in this column the digit will not be zero suppressed.

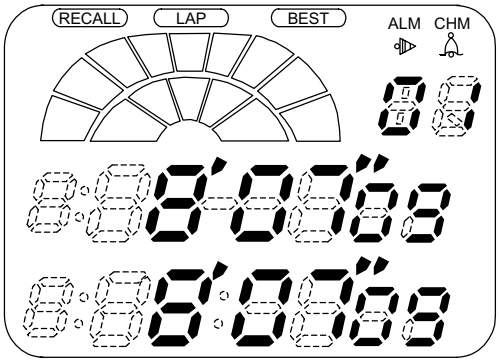
2.7.4 MEMORY RECALL mode

MEMORY RECALL mode stores and displays the lap or split data recorded in CHRONO mode.

- Middle and lower row columns #1 and #8 display the hour; columns #2 and #3, and #9 and #10 display the minutes; columns #4 and #5, and #11 and #12 display the seconds; columns #6 and #13 display tenths of seconds; and columns #7 and #14 display hundredths of seconds. Upper row columns #15 and #16 display the lap or split number.
- The upper row displays the lap or split numbers. The middle row displays the data of the lap or split numbers. The lower row display varies according to which of split or lap data is displayed. For lap time, the lower row shows the time elapsed from the start time to the lap number, in accordance with the lap number at that time. For split time, the lower row shows the total time elapsed irrespective of the split number.
- This mode does not support a graphic display.
- Up to 10 units of data in addition to time data can be stored and displayed.
- MEMORY RECALL mode cannot include both lap data and split data. Either lap or split data is displayed immediately before switching out of CHRONO mode. MEMORY RECALL mode can include one but not both.
- In CHRONO mode, performing lap/split switching by depressing S_4 for two seconds clears the MEMORY RECALL data. If lap is selected for CHRONO mode, the LAP sign is displayed in MEMORY RECALL mode and lap data is displayed. If split is selected for CHRONO mode, the SPLIT sign is displayed in MEMORY RECALL mode and split data is displayed.
- If 10 or fewer units of data are recorded, all the data and stop times are displayed continuously. If over 10 units of data are recorded, only the latest ten units of data are stored and older data is deleted.
- The lap/split numbers start from 01 and continue to 99. After 99, the count returns to 00, 01, 02 up to 99 again, then repeats.
- After switching from MEMORY RECALL mode with lap or split data displayed to another mode, then returning to MEMORY RECALL mode, MEMORY RECALL mode displays the lap or split data from the lowest number, regardless of the number at the time the previous mode was switched. (As long as you did not start in CHRONO mode or did not switch between lap and split after leaving MEMORY RECALL mode.)
- MEMORY RECALL mode simultaneously displays the ON/OFF status of both ALM/CHM (alarm and chime).
- Pressing multiple switches simultaneously invalidates the switches pressed.
- Pressing a second switch while still pressing the first invalidates both switches.

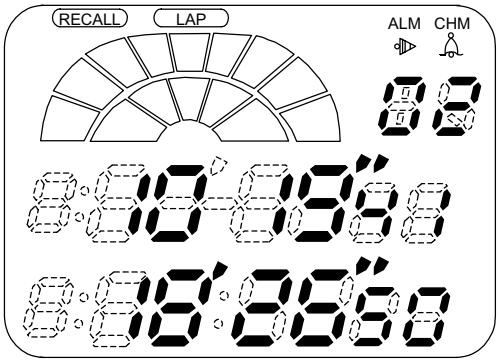
(1) LAP mode

(a) Lap n



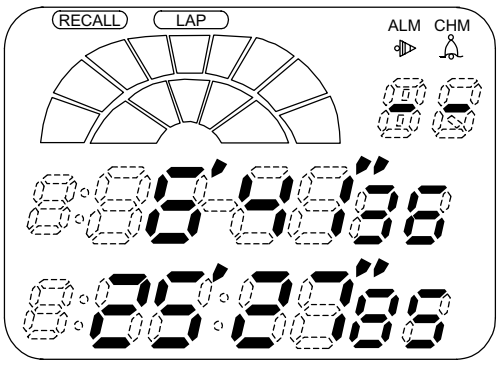
- After lap data is recorded in CHRONO mode, switching to MEMORY RECALL mode displays the data in the middle row starting from the lowest lap number.
- The lower row displays the total time from the start to the applicable lap number.
- Where a best lap is stored in memory, the BEST sign is lit while the data of that lap is displayed.

(b) Lap n + 1



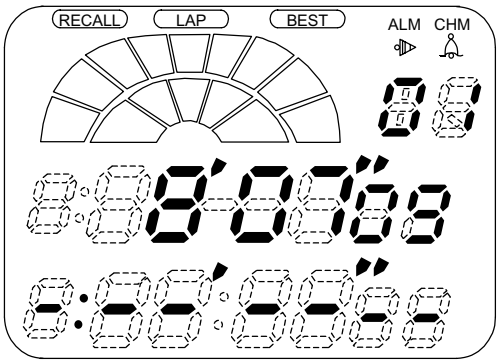
- Pressing S_1 displays the next lap data. Pressing S_2 displays the previous lap data.
- For the applicable lap number, the lower row displays the total time from the start.

(c) Lap stop



- The data at the point the count was stopped is displayed in the middle row. The lower row displays the total time from start to stop.
  The upper row shows "——" as at left.

(d) Best lap



- Whatever data is displayed in MEMORY RECALL mode, while S_4 is depressed, the best lap time is displayed. (If another switch is pressed while S_4 is depressed, the display returns to the lap or stop data displayed before switching to the best lap time display.
- When S_4 is released, the display returns to the lap or stop data displayed before switching to the best lap time display.
- In the best lap time display, the lap number appears in the upper row. The best lap time is displayed in the middle row, as at left.
- The best time is the fastest time among all the lap times recorded. Where a lap number n (100 < n) is the same as the best time number n (100 > n), the BEST sign is not lit even though lap number n, which is not the best time, is displayed.

- When S3 is pressed with LAP mode only selected in CHRONO mode, the display is as at left when MEMORY RECALL mode is entered. The best lap time is as in Figure 2.

  *: When an ALL CLEAR is executed and reset MEMORY RECALL mode is executed (when switching from split to lap in CHRONO mode), the display is as in Figure 1.

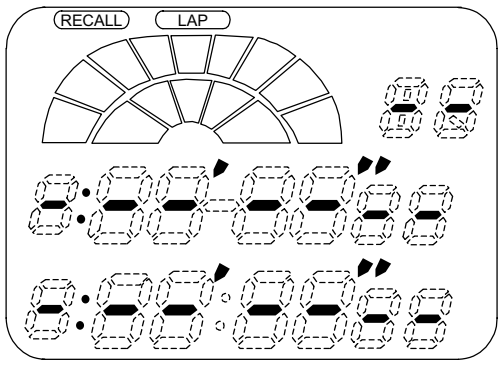


Figure 1

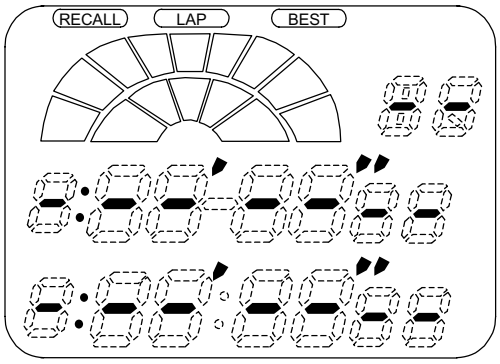
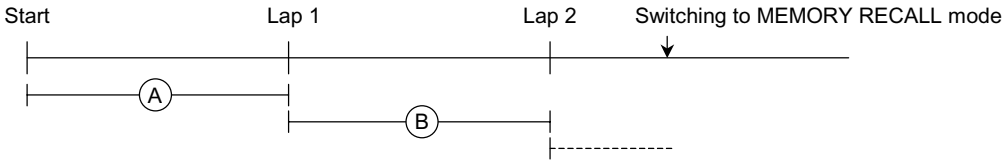


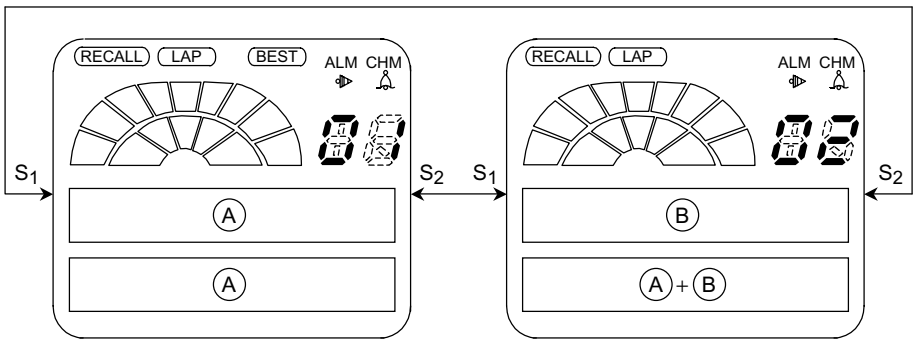
Figure 2

- When recording lap n in LAP mode and pressing S_3 with the count running to switch into MEMORY RECALL mode, the data up to lap n is displayed. (Lap 1 < Lap 2)

<Example>



(MEMORY RECALL mode display)

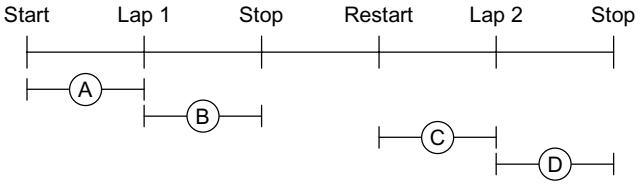


<Lap 1> display <Lap 2> display

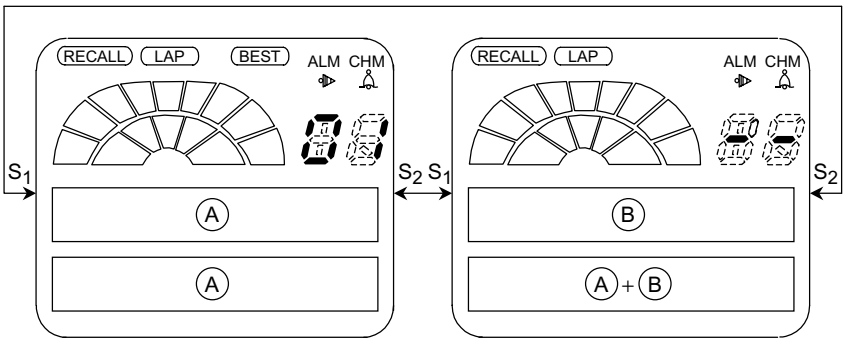
- In CHRONO mode, if you start a lap n, record, then stop and restart, the count starts from the stop time. The data following lap n + 1 continues from the stop time.
  (The counting from the previous stop time continues until a reset.)

  *: Lap 1 < Lap 2

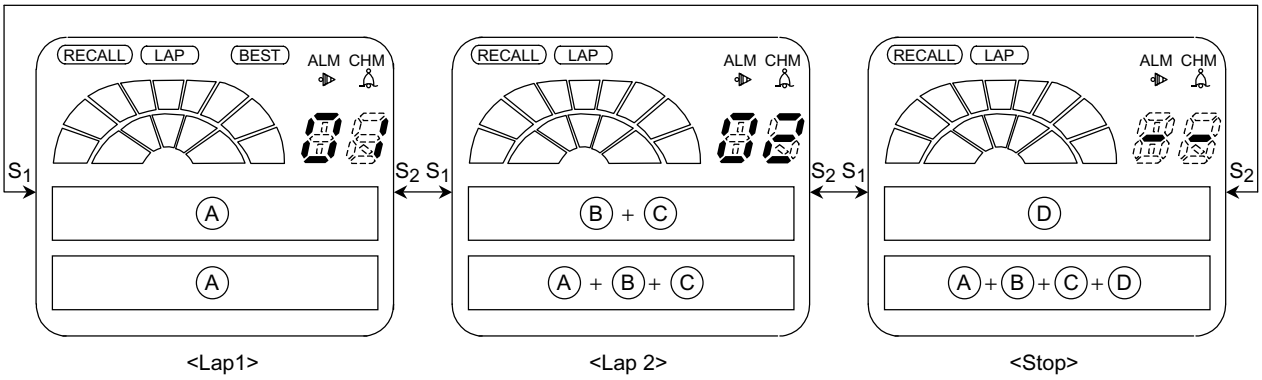
  <Example>



(MEMORY RECALL mode display when start → lap 1 → stop.)

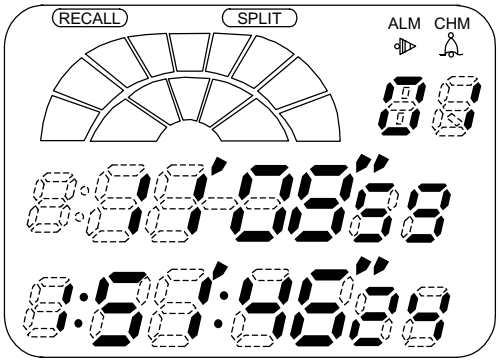


(MEMORY RECALL mode display when start → lap 1 → stop → restart → lap 2 → stop.)



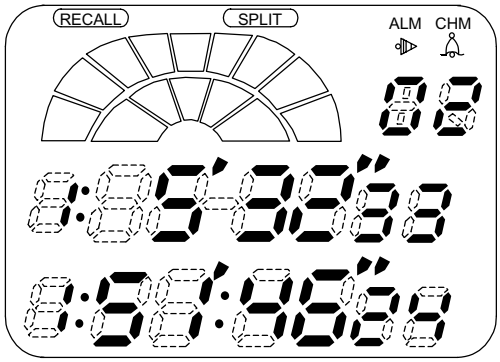
(2) Split mode display

(a) Split n



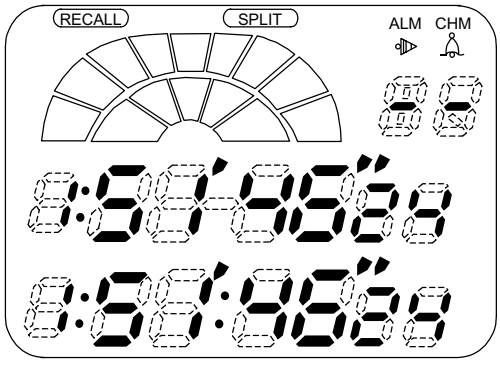
- When entering MEMORY mode after recording split data in CHRONO mode, data is displayed in the middle row starting from the lowest split number.
- The lower row displays the total time, irrespective of the split number.

(b) Split n + 1



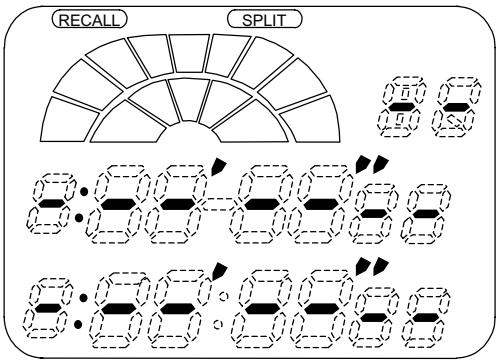
- Each press of S_1 displays the next split data.
  Each press of S_2 displays the previous split data.
- The lower row displays the final (at STOP) total time.

(c) Split stop



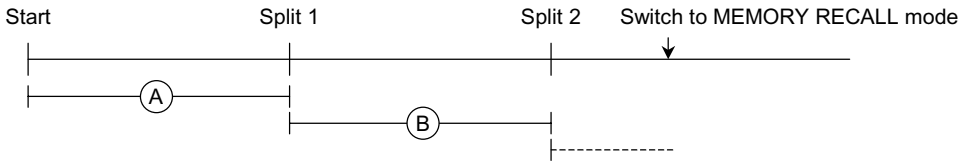
- As the middle row displays the data for when the count was last stopped, this is the same data as in the lower row.
  The upper row shows "——" as at left.

- With only the split mode activated in CHRONO mode, pressing S_3 to enter MEMORY RECALL mode produces a display as below. Resetting MEMORY RECALL mode (switching from lap to split) also produces a display as below.

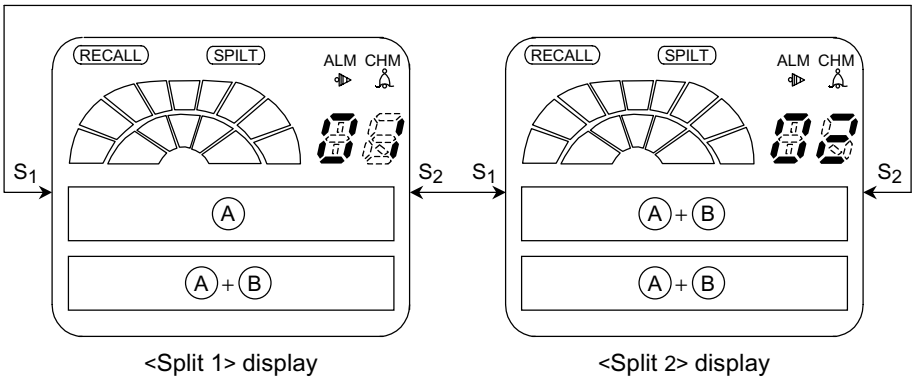


- When recording split n in SPLIT mode and pressing S_3 with the count running to switch into MEMORY RECALL mode, the data up to split n is displayed.

<Example>

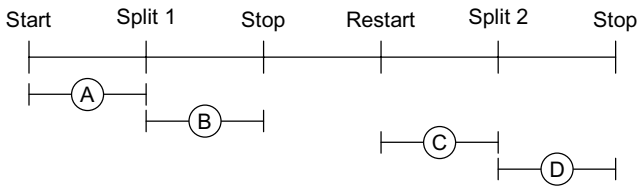


(Display in MEMORY RECALL mode)

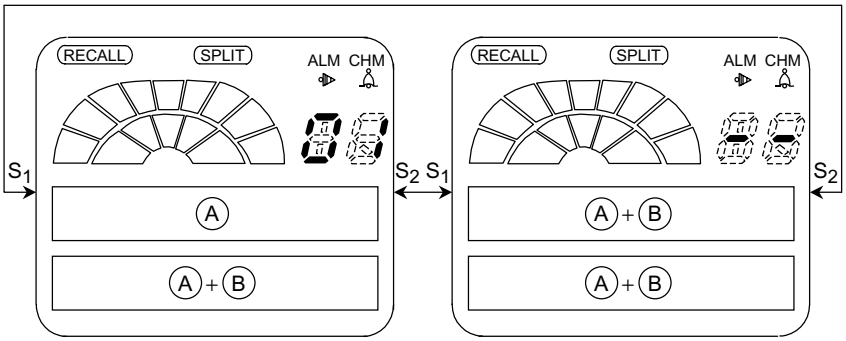


- In CHRONO mode, if you start a split n count, record, then stop and restart, the count from the stop time. The data following split n + 1 continues from the stop time. (The data continues until a reset.)

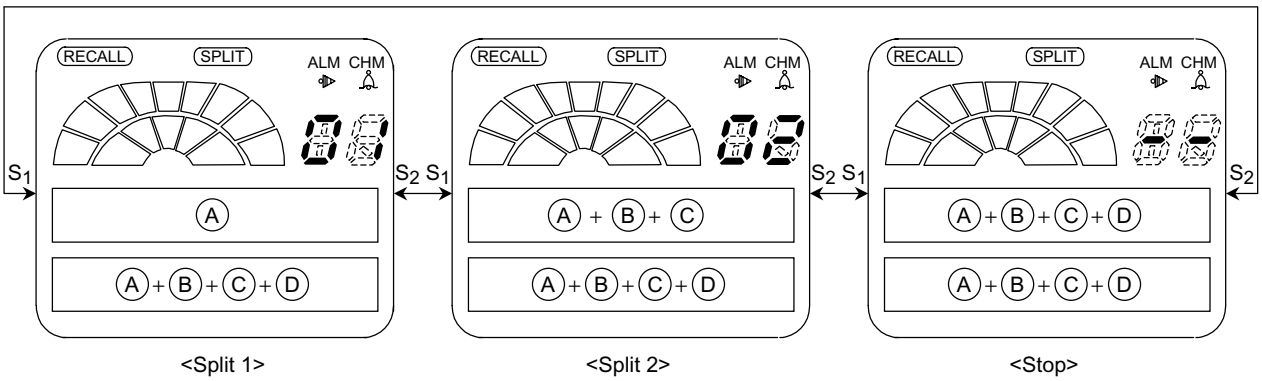
<Example>



(MEMORY RECALL mode display when start → split 1 → stop.)



(MEMORY RECALL mode display when start → split 1 → stop → restart → split 2 → stop.)



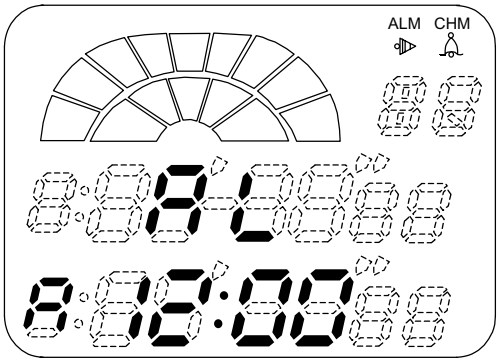
2.7.5 ALARM mode

ALARM mode is used to set and display the alarm and time signal.

- In this mode, the graphic display and upper row columns #15 and #16 go OFF.
- In MEMORY RECALL mode, press S_3 to switch to ALARM mode.
- The alarm and time signal ON/OFF states are displayed by the upper right sign. (Lit: ON, unlit: OFF)
- In ALARM mode, each press of S_1 turns the alarm ON, time signal OFF → alarm OFF, time signal ON → alarm/time signal ON → alarm/time signal OFF → alarm ON, time signal OFF...
- In ALARM mode, depressing S_1 for two seconds sounds a test alarm. While S_1 is depressed, the alarm continues sounding. (When the alarm is sounding, pressing another switch turns the alarm sound OFF. If the test alarm is sounding when the preset alarm or time signal are due to come ON, the test alarm tone takes precedence and the set alarm or time signal chime do not sound.)
- If the settings for the alarm and time signal are for the same time, the alarm takes precedence.
- The ALARM mode does not allow 12-hour/24-hour clock switching. (Such switching is supported only in TIME mode.) The 12-hour and 24-hour clocks conform to TIME mode.
- Press S_2 to switch between the alarm and time signal displays.
- After ALL CLEAR, the alarm display shows “AM12:00” if the 12-hour clock is selected, and “0:00” if the 24-hour clock is selected. After the ALL CLEAR, the time signal display shows “00”.
- Pressing multiple switches simultaneously invalidates the switches pressed.
- Pressing a second switch while still pressing the first invalidates both switches.

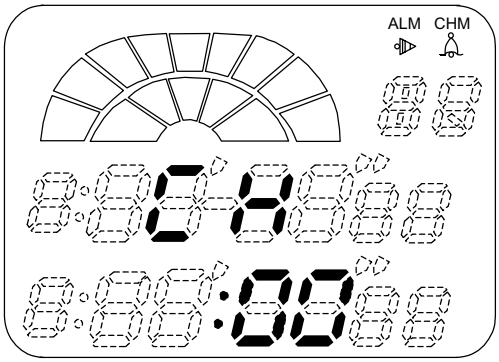
Alarm/time signal <Display configuration>

(a) Alarm display



- The middle row displays “AL”. The bottom row displays the set time-of-day.
- Press S_2 to switch between the alarm and time signal.

(b) Time signal display



- The middle row displays “CH”. The bottom row displays the set minutes of the hour.

2.7.6 ALARM SETTING mode

- Press S_4 while the alarm or time signal is displayed to switch to ALARM SETTING mode for the alarm or time signal.
- If a switch is not pressed for one minute while in ALARM SETTING mode, the device automatically switches to ALARM mode.
- When switching to ALARM SETTING mode from ALARM mode, even if the alarm/time signal are set, the ALM or CHM sign goes OFF and the alarm and chime (time signal) sounds are disabled.
- In ALARM SETTING mode, press S_4 to switch to ALARM mode.
  When switching to ALARM mode from ALARM SETTING mode,

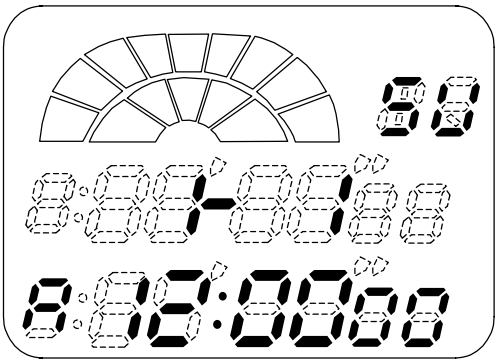
  the alarm is set and the ALM sign is lit. The CHM sign returns to the status prevailing before switching to ALARM SETTING mode.
  When switching to ALARM mode from ALARM SETTING mode for the time signal, the time signal is set and the CHM sign is lit. The ALM sign returns to the status prevailing before switching to ALARM SETTING mode.
- The method of correcting the alarm hour and minutes, and the method of correcting the time signal minutes is the same as for correcting the hour and minutes in TIME SETTING mode. Press S_3 to switch between the alarm hours and minutes to be set.
- Pressing multiple switches simultaneously invalidates the switches pressed.
- Pressing a second switch while still pressing the first invalidates both switches.

2.7.7 ALARM functions

- With the ALM sign lit, when the current time matches the set alarm time, the alarm sounds for 20 seconds.
- In ALARM SETTING mode, even if the set alarm time matches the current time, the alarm will not sound.
- To stop the alarm sound in any mode except ALARM SETTING mode, press any one of switches S_1~S_4.
- If the alarm sound comes on while you are depressing a switch in any mode except SETTING mode, release the switch then press it again to stop the alarm sounding.
- While switching from TIME mode to TIME SETTING mode by depressing S_4 for two seconds (in TIME mode), the alarm will sound if the set alarm time matches the current time. However, keep S_4 depressed. As soon as the mode is switched, the alarm sound and the ALM sign go off.

2.7.8 ALL CLEAR

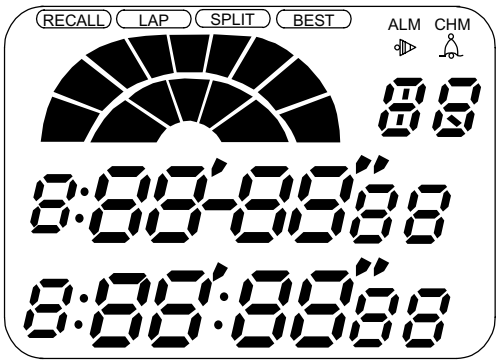
After an ALL CLEAR, TIME mode is selected. The count starts from January 1 (Sunday) AM12 hours, 0 minutes, 0 seconds. After an ALL CLEAR, the display is as below.



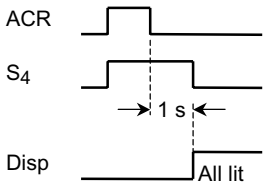
2.7.9 ALL segments lit

Immediately after an ALL CLEAR, press S_4 (until the display comes ON) to light all segments (the display is as below). Then, to switch from all segments being lit to TIME mode, push any one of S_1~S_4.

*: After an ALL CLEAR, TIME mode starts counting. Therefore, when you return to TIME mode, the time count has advanced.

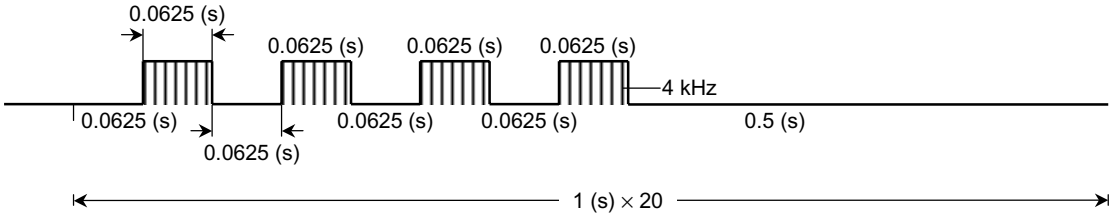


Timing flow chart

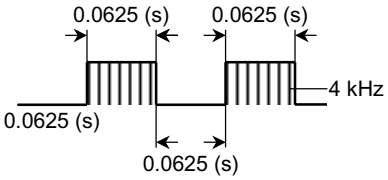


2.7.10 Alarm waveform

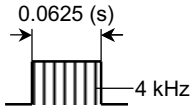
<Alarm sound>



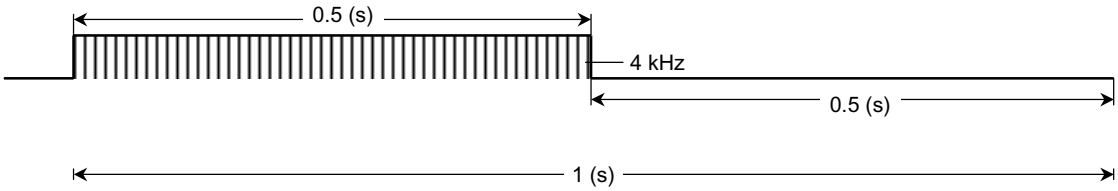
<Chime sound (Time signal) >



<Switch-push sound>



<Best lap time sound>



2.8 ALL Clear function

When power is applied or when the supply of power is interrupted (e.g. if the battery is changed), the internal state of the IC may become unstable, even though it appears to be operating normally. For this reason it is vital to verify that the crystal oscillation circuit is oscillating normally and stably (at 32 kHz) and then to use the system reset pin to initialize the IC (i.e. clear it) before use.
Note that a clear operation using the built-in power-on clear circuit should not be used in this case. Refer to "5. Handling precautions" for details of ALL Clear function.

3. Electrical specifications

Maximum Ratings
(Unless otherwise specified, V_{SS} = 0 V, V_{DD1} = 1.5 V, V_{DD2} = 3.0 V, V_{DD3} = 4.5 V, Ta = 25°C)

No.	Characteristics	Symbol	Rating	Unit
1	Power supply voltage (1)	$V_{SS} - V_{DD1}$	−0.2~+3.0	V
2	Power supply voltage (2)	$V_{SS} - V_{DD2}$	−0.2~+5.0	V
3	Power supply voltage (3)	$V_{SS} - V_{DD3}$	−0.2~+6.5	V
4	V_{DD1} system input voltage	V_{IN1}	V_{SS} − 0.2~V_{DD1} + 0.2	V
5	V_{DD2} system input voltage	V_{IN2}	V_{SS} − 0.2~V_{DD2} + 0.2	V
6	V_{DD3} system Input voltage	V_{IN3}	V_{SS} − 0.2~V_{DD3} + 0.2	V
7	V_{DD1} system output withstanding voltage	V_{OUT1}	V_{SS} − 0.2~V_{DD1} + 0.2	V
8	V_{DD2} system output withstanding voltage	V_{OUT2}	V_{SS} − 0.2~V_{DD2} + 0.2	V
9	V_{DD3} system output withstanding voltage	V_{OUT3}	V_{SS} − 0.2~V_{DD3} + 0.2	V
10	Operating temperature range	T_{opr}	−10~+60	°C
11	Storage temperature range	T_{stg}	−40~+125	°C

Recommended Operating Conditions
(Unless otherwise specified, V_{SS} = 0 V, V_{DD1} = 1.5 V, V_{DD2} = 3.0 V, V_{DD3} = 4.5 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Test Diagram	(Note)
V_{DD1} system operating voltage range	$\lvert V_{DD1} \rvert$	V_{DD1}	No load	1.20	1.50	1.80	V	—	—
V_{DD2} system operating voltage range	$\lvert V_{DD2} \rvert$	V_{DD2}	No load	2.40	3.00	3.60	V	3.6	1
V_{DD3} system operating voltage range	$\lvert V_{DD3} \rvert$	V_{DD3}	No load	3.60	4.50	5.40	V	—	—
Low-speed clock crystal oscillator frequency	fXT	X_{IN}, X_{OUT}	V_{DD} = 3.0 V	—	32.768	—	kHz	3.1	—
High-speed clock CR oscillator frequency	fCR	R_{IN}, R_{OUT}	V_{DD} = 3.0 V R = 100 kΩ	—	400	—	kHz	3.1	—

DC Characteristics

(Unless otherwise specified, V_{SS} = 0 V, V_{DD1} = 1.5 V, V_{DD2} = 3.0 V, V_{DD3} = 4.5 V, Ta = 25°C)

Characteristics	Symbol	Applic-able Pin	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Test Diagram	(Note)
V_{DD1} system leak current	IDD1L	V_{DD1}	—	—	—	—	1.0	μA	3.4	—
V_{DD2} system leak current	IDD2L	V_{DD2}	—	—	—	—	1.0	μA	3.4	—
V_{DD3} system leak current	IDD3L	V_{DD3}	—	—	—	—	1.0	μA	3.4	—
V_{DD1} system step-down voltage	VDCO1	V_{DD1}	—	R_L = 3 MΩ	1.4	—	—	V	3.5	—
V_{DD3} system step-up voltage	VUCO3	V_{DD3}	—	R_L = 3 MΩ	4.3	—	—	V	3.5	—
Oscillation start voltage	VSTA	X_{IN}, X_{OUT}	—	—	2.6	—	—	V	3.3	5
Oscillation hold voltage	VHOLD	X_{IN}, X_{OUT}	—	—	2.4	—	—	V	3.3	—
CR Oscillator voltage Dependency	V_{CR}	R_{IN}, R_{OUT}	—	V_{DD2} = 2.4~3.6 V	−30	—	30	%	3.3	—
Low oscillation frequency VTH dependency	$\Delta\varepsilon I_C$	X_{IN}, X_{OUT}	—	—	—	—	8	ppm	3.3	8
Low oscillation Frequency V_{DD2} dependency	$\Delta\varepsilon V_{DD2}$	X_{IN}, X_{OUT}	—	V_{DD2} = 2.4~3.6 V	—	—	4	ppm	3.3	7, 9
Low oscillation frequency C_G dependency	$\Delta\varepsilon C_G$	X_{IN}, X_{OUT}	—	C_G = 5~20 pF	—	20	—	ppm	3.3	6, 9
Oscillator output resistance	ROUTX	X_{IN}, X_{OUT}	—	—	—	250	—	kΩ	—	—
Built-In CD capacitance	CD	X_{IN}, X_{OUT}	—	—	—	20	—	pF	—	9

DC Characteristics (Current dissipation)

CPU Block (V_{DD} – V_{SS} system)

Characteristics	Symbol	Applic-able Pin	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Test Diagram	(Note)
High-speed operation mode current dissipation	IDD (OPH)	—	—	V_{DD} = 3.0 V fCR = 400 kHz	—	100	200	μA	3.1	2
Low-speed operation mode current dissipation	IDD (OPL)	—	—	V_{DD} = 3.0 V fXT = 32.768 kHz	—	2.5	4.0	μA	3.1	3
STOP mode current dissipation	IDD (STOP)	—	—	V_{DD} = 3.0 V fXT = 32.768 kHz	—	1.0	2.0	μA	3.1	4

DC Characteristics (Pin capacity)

(Unless otherwise specified, V_{SS} = 0 V, V_{DD1} = 1.5 V, V_{DD2} = 3.0 V, V_{DD3} = 4.5 V, Ta = 25°C)

Characteristics	Symbol	Applicable Pin	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Test Diagram	(Note)
Output current "H"	I_{OH1}	OUT, IO	—	V_{DD2} = 2.5 V V_{OH1} = 2.0 V	—	—	−250	μA	3.2	—
Output current "L"	I_{OL1}	OUT, IO	—	V_{DD2} = 2.5 V V_{OL1} = 0.5 V	10	—	90	μA	3.2	—
Output current "H"	I_{OH2}	BZ/DC1	—	V_{DD2} = 2.5 V V_{OH2} = 2.0 V	—	—	−250	μA	3.2	—
Output current "L"	I_{OL2}	BZ/DC1	—	V_{DD2} = 2.5 V V_{OL2} = 0.5 V	250	—	—	μA	3.2	—
Output current "H"	I_{OH3}	SEG, COM	—	For $V_{SS} - V_{DD3}$ V_{OH3} = 4.0 V	—	—	−80	μA	3.2	—
Output current "L"	I_{OL3}	SEG, COM	—	For $V_{SS} - V_{DD3}$ V_{OL3} = 0.5 V	80	—	—	μA	3.2	—
Output current "H"	I_{OH4}	SEG, COM	—	For $V_{SS} - V_{DD1}$ V_{OH4} = 1.0 V	—	—	−80	μA	3.2	—
Output current "L"	I_{OL4}	SEG, COM	—	For $V_{SS} - V_{DD1}$ V_{OL4} = 2.0 V	80	—	—	μA	3.2	—
Output current "H"	I_{OH5}	SEG, COM	—	For $V_{SS} - V_{DD2}$ V_{OH5} = 2.5 V	—	—	−80	μA	3.2	—
Output current "L"	I_{OL5}	SEG, COM	—	For $V_{SS} - V_{DD2}$ V_{OL5} = 3.5 V	80	—	—	μA	3.2	—
Input current "H"	I_{IH1}	AC	—	V_{IH1} = 3.0 V	30	50	75	μA	3.2	—
Input current "L"	I_{IL1}	AC	—	V_{IL1} = 0 V	−1.0	—	1.0	μA	3.2	—
Input current "H"	I_{IH2}	TEST1, TEST2 IN1, IN2	—	V_{IH2} = 3.0 V	30	50	75	μA	3.2	—
Input current "L"	I_{IL2}	TEST1, TEST2 IN1, IN2	—	V_{IL2} = 0 V	−1.0	—	1.0	μA	3.2	—

Note1: The voltage range where the oscillation and step-up voltage are held and the internal circuits operate correctly.

Note2: The current consumed in High-Speed mode after all clear.

Note3: The current consumed in Low-Speed mode set by the [FXT] instruction after all clear.

Note4: The current consumed in OFF mode set by the [STOP] instruction after all clear.

Note5: The value of the V_{SS2} voltage when a stepped voltage is applied to V_{SS2} and less than 10 seconds is required until a normal waveform is output to ϕ1 output.

Note6: $\Delta\varepsilon C_G$ is calculated by the following equation. Note that T_0 = 1000 ms.

$$\Delta\varepsilon C_G = \frac{T\ (C_G = 20\ pF) - T\ (C_G = 5\ pF)}{T_0} \times 10^6\ [ppm]$$

Note7: $\Delta\varepsilon V_{DD2}$ is calculated by the following equation.

$$\Delta\varepsilon V_{DD2} = \left| \frac{T\ (V_{DD2} = 3.6\ V) - T\ (V_{DD2} = 2.4\ V)}{T_0} \right| \times 10^6\ [ppm]$$

Note8: When the mean value t of the periodic anomaly of a 100% sample and the typical anomaly,

$$\sigma = \sqrt{\Sigma(ti - t)^2 / (n - 1)}$$

$$\Delta\varepsilon I_C = \pm 3\sigma$$

Note9: This is a guaranteed design value. The characteristics are checked by an initial sample.

Test circuits

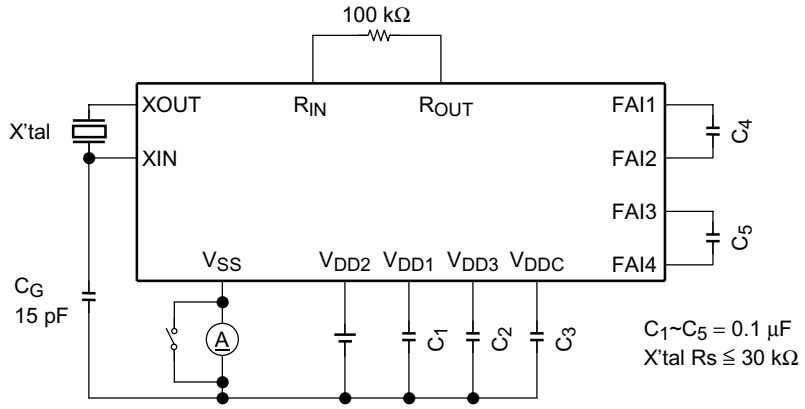


Figure 3.1 Measurement of Current Dissipation and Osicillation Frequency

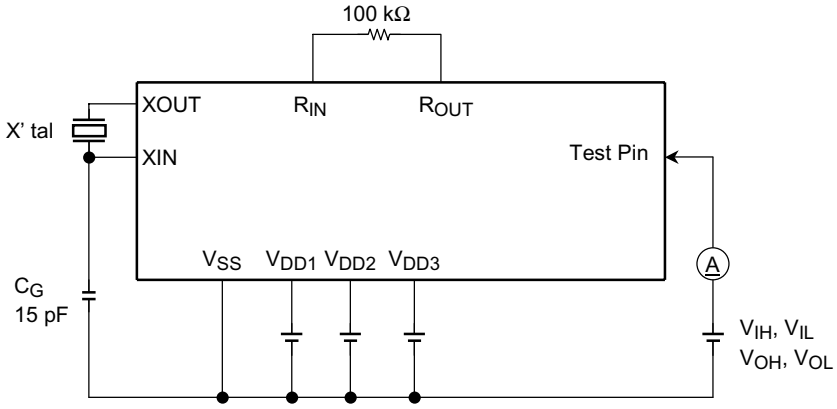


Figure 3.2 Measurement of Input/Output Current

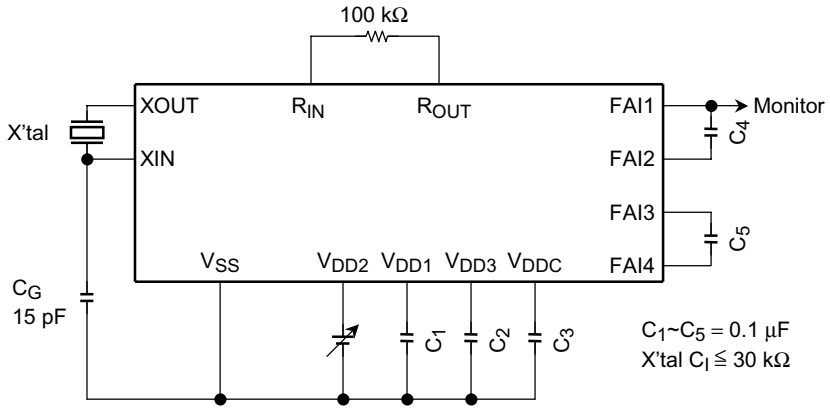


Figure 3.3 Measurement of VSTA and VHOLD

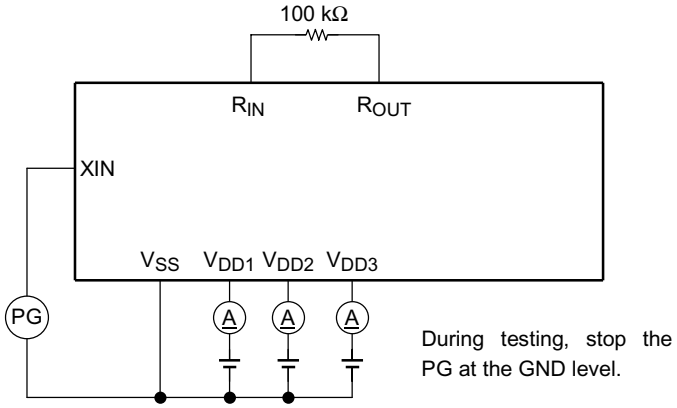


Figure 3.4 V_{DD1}, V_{DD2} and V_{DD3} Leakage Currents

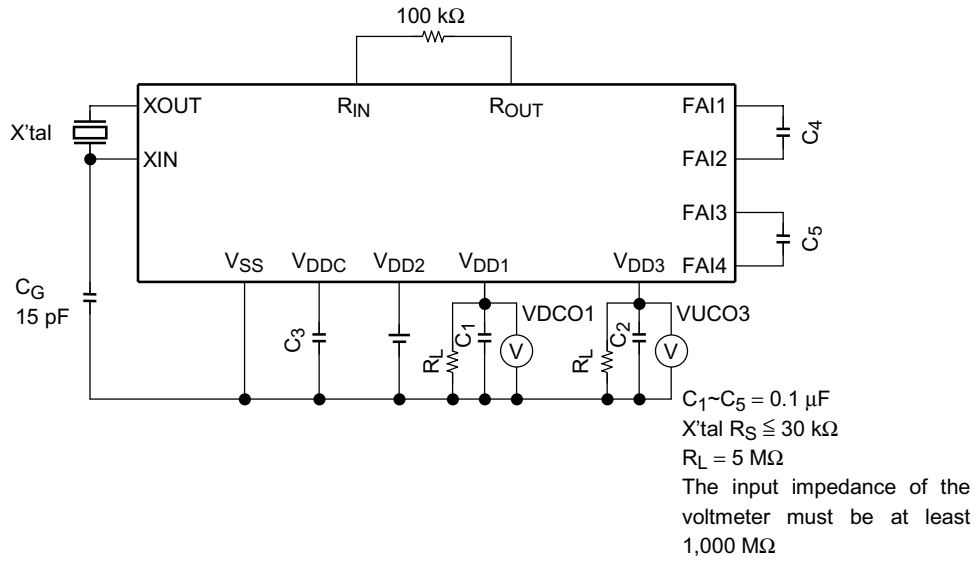


Figure 3.5 Measurement of VDCO, VUCO

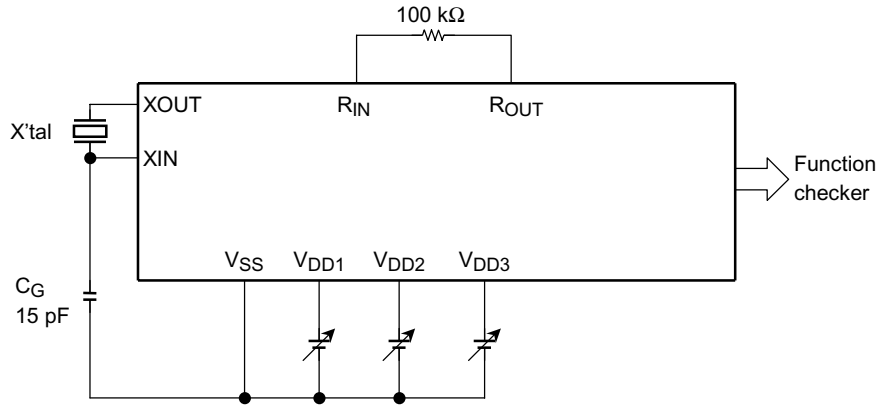
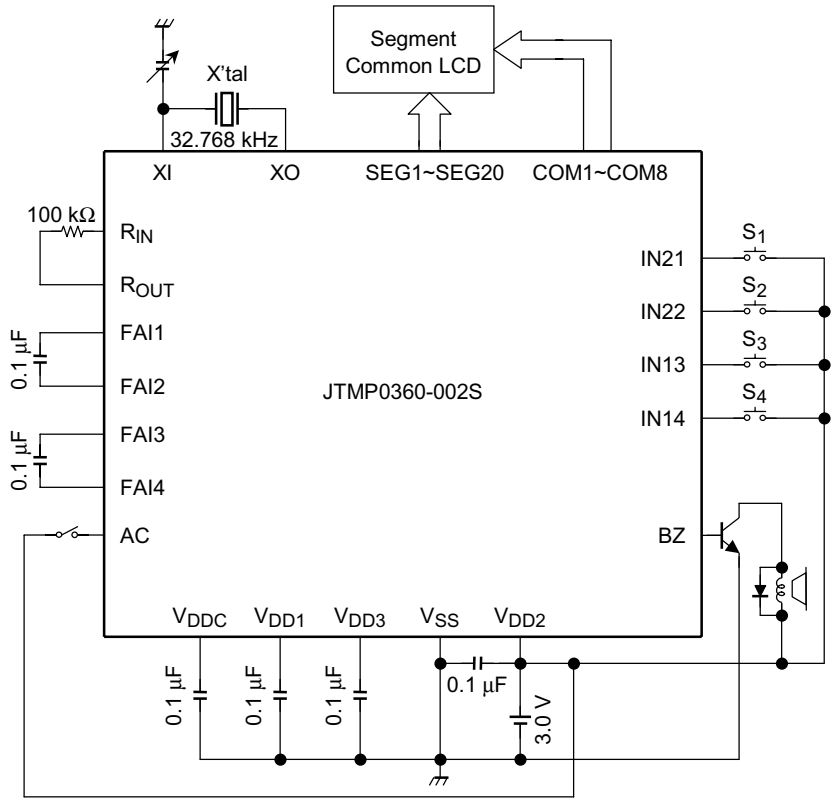


Figure 3.6 Measurement of V_{DD1}, V_{DD2} and V_{DD3} Operating Voltage Ranges

4. Application Circuit



5. Handling precautions

Described below are precautions for handling the device.

5.1 Reset by AC pin

<At normal operation>

When the power supply voltage is within the operating voltage and the crystal oscillator is operating, holding the AC pin at High for 2 ms or longer initializes the internal LSI (Figure 5.1).

When the AC pin level goes to Low, reset is released, starting execution of the program. The AC pin is internally pulled down. A switch can configure a simple reset circuit. Note that the AC pin incorporates a noise canceller; thus, to assure reset, the AC pin must be held High for at least 2 ms (Figure 5.2).

<At power on>

When the crystal oscillator is not operating normally, for example, at power on, the noise canceller does not operate. As a result, the level is not read from the AC pin. While the AC pin is held High, backup is performed to start operation of the crystal oscillator. The AC pin must be held High for 3 seconds until the crystal oscillator operates normally (Figures 5.3 and 5.4). If oscillation does not start after the above operation, an OFF instruction may be executed. In such a case, inputting High to one of the IN11 to IN14 pins while holding the AC pin at High releases the OFF instruction and starts oscillation.

Note1: At power on or power cutoff, operation of the internal IC is unstable. An all-clear is required.

Note2: To check that the all-clear is complete, confirm that the IC is in initial state, for example, by checking the LCD display.

Note3: During backup, the power supply voltage (V_{DD2}) is directly applied to the crystal oscillator. Thus, current dissipation (60 (A typ.) during backup increases more than usual.

5.2 Reset by simultaneous high input to SW pins (IN21, 22, 13, 14)

Simultaneously inputting High to the SW (IN21, 22, 13, 14) pins for at least two seconds performs a reset. However, because a noise canceller is incorporated to prevent erroneous resets, resets are valid when the crystal oscillator is operating normally (Figures 5.5 and 5.6).

Backup is performed while a reset signal input to the SW pins via the noise canceller resets the internal system. The power supply voltage (V_{DD2}) is directly applied to the oscillator. Thus, current dissipation (60 (A typ.) during backup increases more than usual (Figure 5.4).

Backup is released approximately two seconds after a reset by the SW pins is released. The current value returns to normal.

The all-clear timing by AC pin and all-clear circuit are shown below.

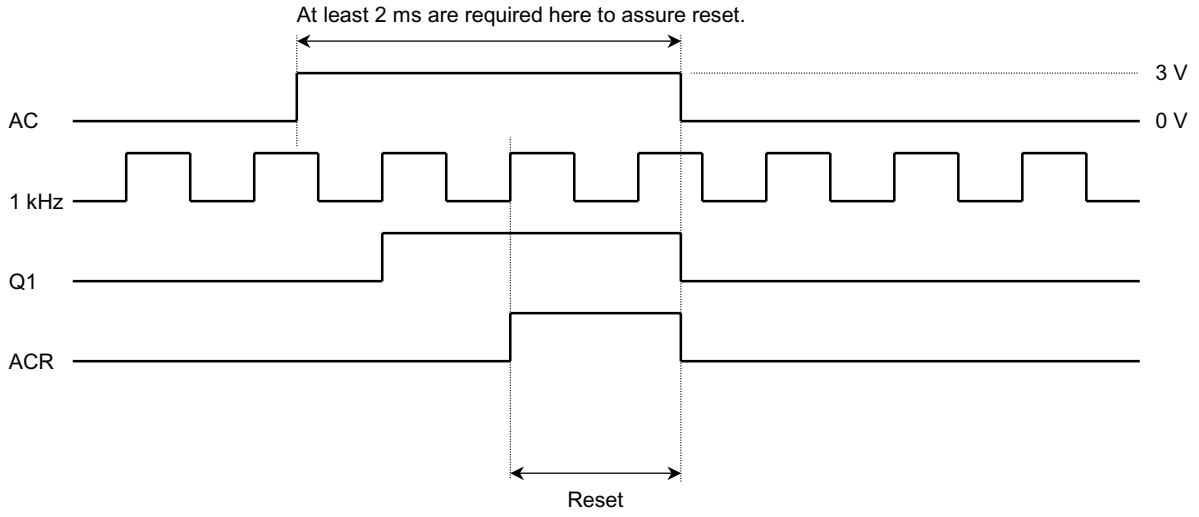


Figure 5.1 All-Clear Timing Chart

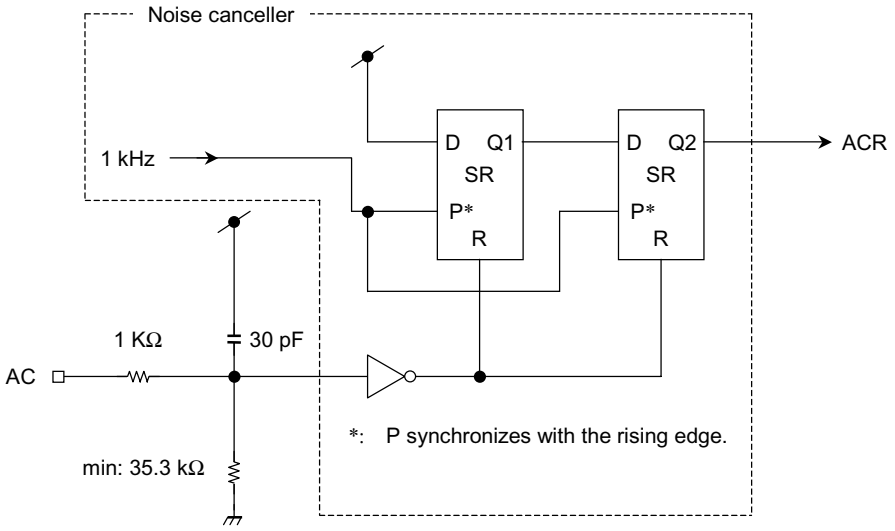


Figure 5.2 All-Clear Circuit

Below is a timing chart for backup.

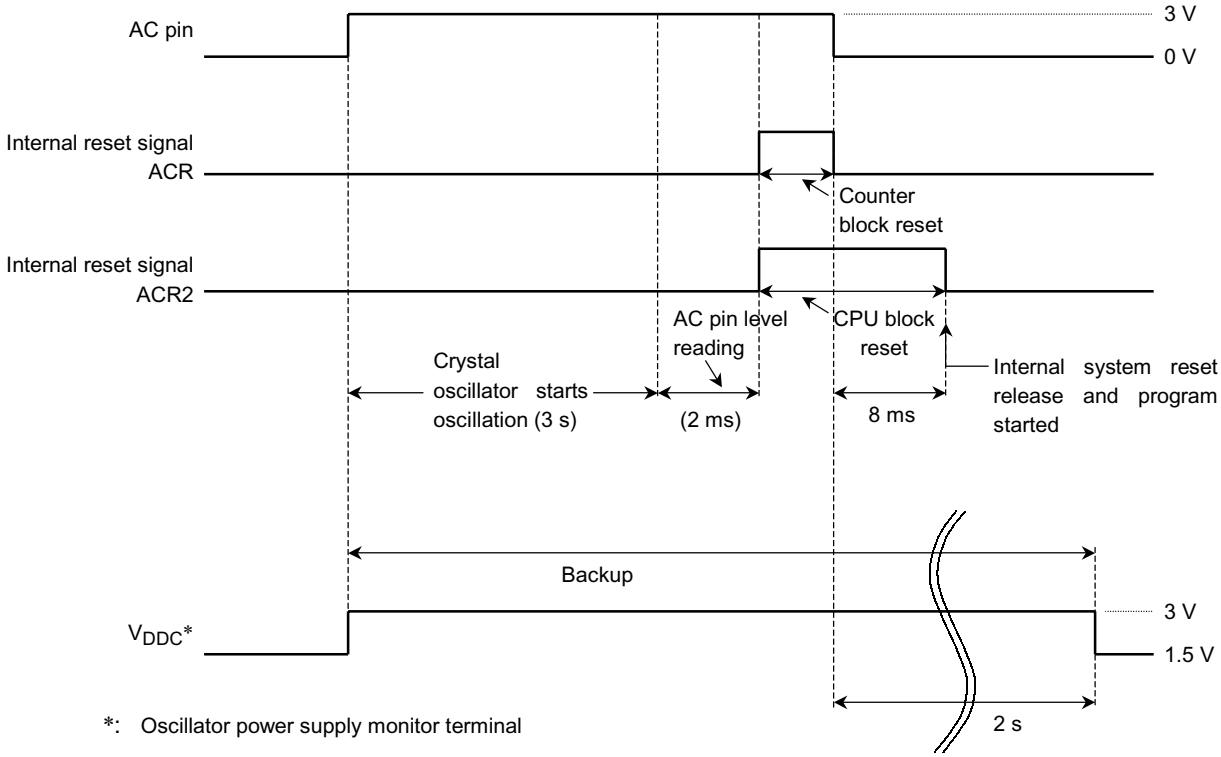


Figure 5.3 Backup Timing Chart

Below is a circuit diagram for the backup circuit.

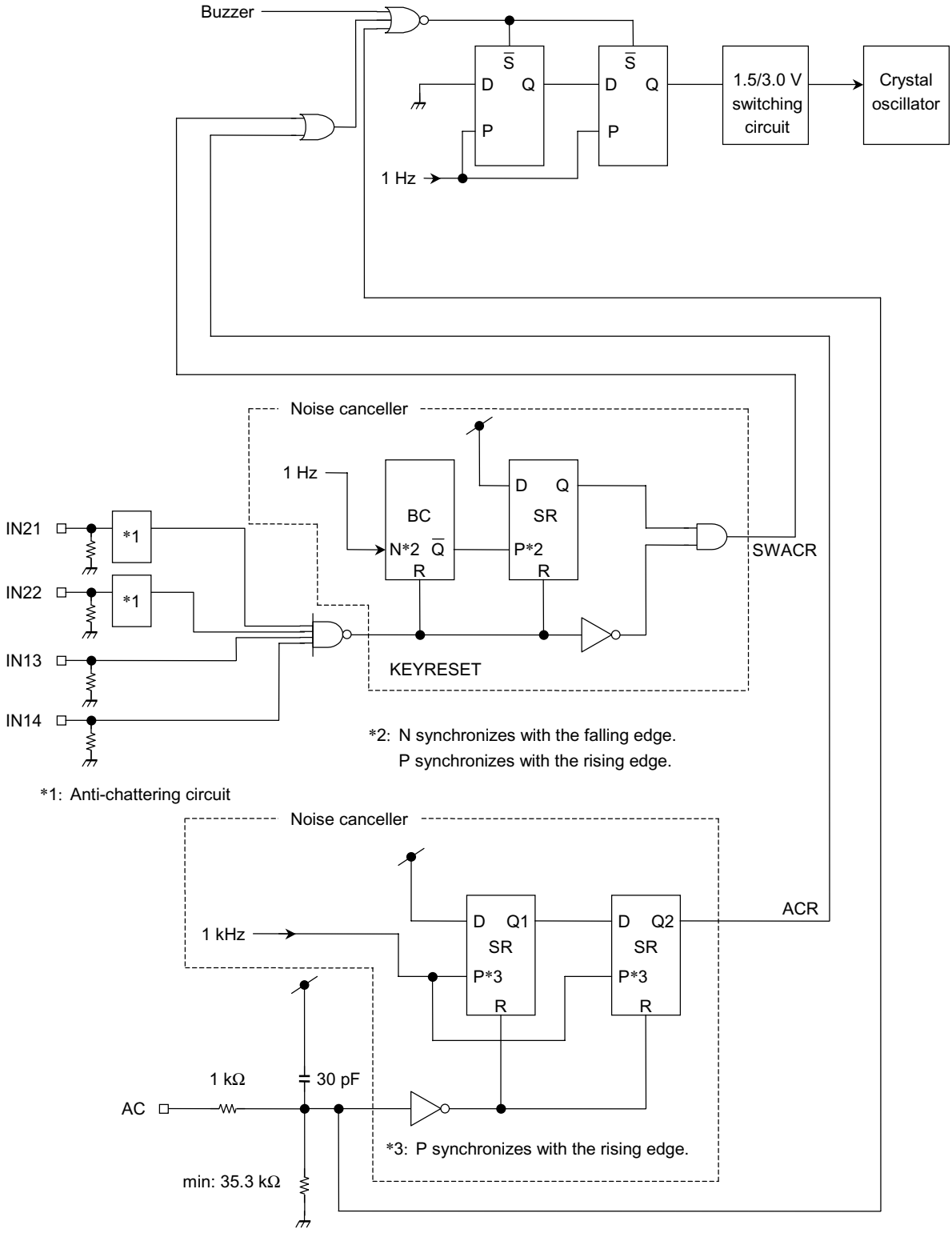


Figure 5.4 Backup Circuit

Below are a timing chart for the all-clear and a circuit diagram for the all-clear circuit using simultaneous pressing of the switches.

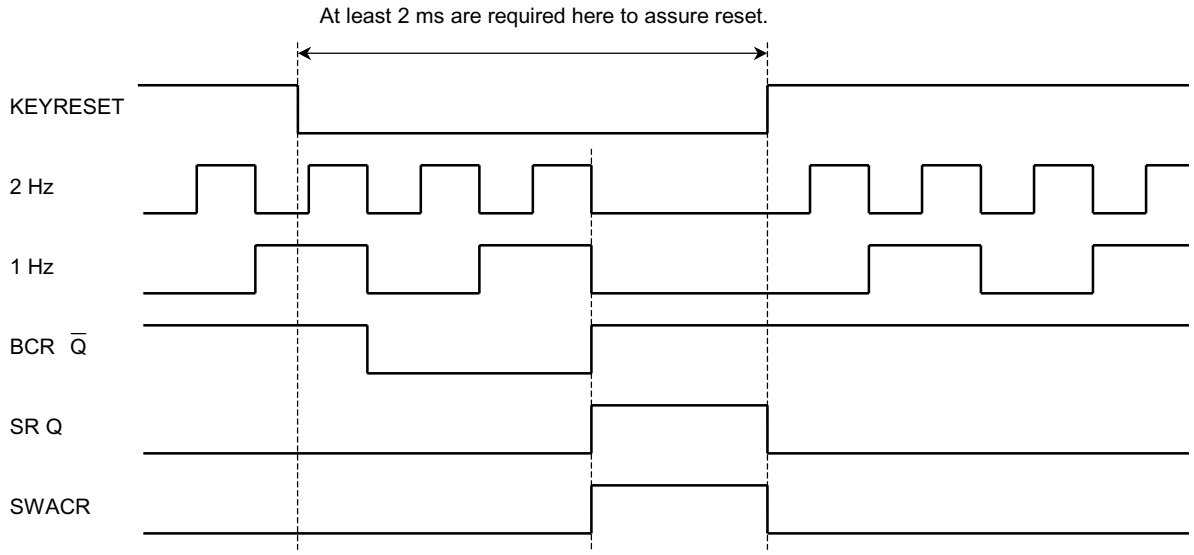


Figure 5.5 SW All-Clear Timing Chart

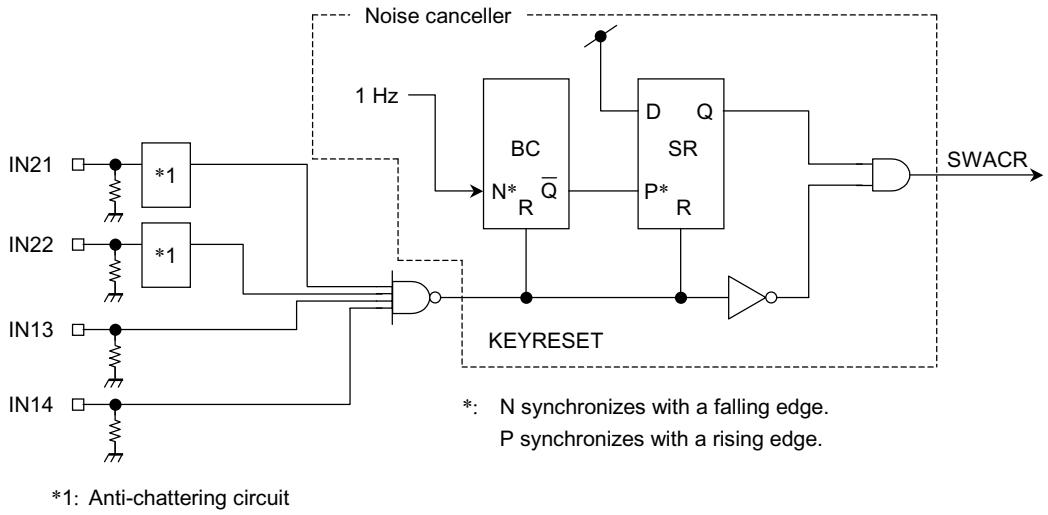


Figure 5.6 SW All-Clear Circuit