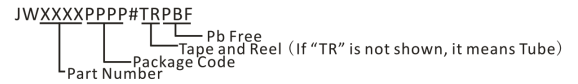




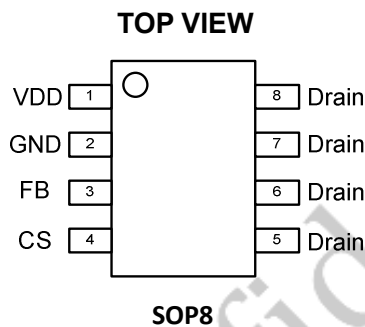
**ORDER INFORMATION**

LEAD FREE FINISH	TAPE AND REEL	PACKAGE	TOP MARKING
JW1501ASOPB#PBF	JW1501ASOPB#TRPBF	SOP8	JW1501A
JW1501BSOPB#PBF	JW1501BSOPB#TRPBF	SOP8	JW1501B

Note:



**PIN CONFIGURATION**



**ABSOLUTE MAXIMUM RATING<sup>1)</sup>**

VDD Voltage.....	34.5V
VDD DC Clamp Current .....	10mA
Drain pin.....	-0.3 to 650V
FB voltage range.....	-0.7 to 7V
CS voltage range.....	-0.3 to 7V
Junction Temperature <sup>2)</sup> .....	150°C
Storage Temperature .....	-65°C to +150°C
Lead Temperature (Soldering, 10sec.).....	260°C

**RECOMMENDED OPERATING CONDITIONS**

VDD Voltage.....	11 to 27V
Operating Temperature Range.....	-40°C to +85°C
Maximum Switching Frequency @ Full Loading & Flyback PSR Mode.....	70kHz
Minimum Switching Frequency @ Full Loading & Flyback PSR Mode.....	35kHz
Junction Temperature (T <sub>J</sub> ).....	-40°C to 125°C

**THERMAL PERFORMANCE<sup>3)</sup>**

	$\theta_{JA}$	$\theta_{JC}$
SOP8 .....	96...	45°C/W

Note:

- 1) Exceeding these ratings may damage the device.
- 2) JW1501A/B guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
- 3) Measured on JE51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS**

<i>T<sub>A</sub>=25 °C, unless otherwise stated</i>						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
<b>Supply Voltage Section (VDD Pin)</b>						
Start-up current into VDD pin	I <sub>VDD_st</sub>			2	15	uA
Operation Current	I <sub>VDD_Op</sub>	V <sub>FB</sub> =1.1V, VDD=18V	0.3	0.7	0.9	mA
Standby Current	I <sub>VDD_standby</sub>			0.5	1	mA
VDD Under Voltage Lockout Exit	V <sub>DD_ON</sub>		15	16.3	17.5	V
VDD Under Voltage Lockout Enter	V <sub>DD_OFF</sub>		8	9	10	V
VDD OVP Threshold	V <sub>DD_OVP</sub>		28	30	32	V
VDD Zener Clamp Voltage	V <sub>DD_Clamp</sub>	I(V <sub>DD</sub> ) = 5 mA	32.5	34.5	36.5	V
<b>Control Function Section (FB Pin)</b>						
Internal Error Amplifier (EA) Reference Input	V <sub>FB_REF</sub>		1.97	2.0	2.03	V
Short Load Protection (SLP) Threshold	V <sub>FB_SLP</sub>			0.7		V
Short Load Protection (SLP) Debounce Time	T <sub>FB_Short</sub>			10		ms
Demagnetization Comparator Threshold	V <sub>FB_DEM</sub>			25		mV
Minimum OFF time	T <sub>off_min</sub>	(Note 4)		2		us
Maximum OFF time	T <sub>off_max</sub>	(Note 4)	3.6	4	4.5	ms
Maximum Cable Drop compensation current	I <sub>Cable_max</sub>		48	53	58	uA
<b>Current Sense Input Section (CS Pin)</b>						
CS Input Leading Edge Blanking Time	T <sub>LEB</sub>			500		ns
Current limiting threshold	V <sub>cs(max)</sub>		490	500	510	mV
Over Current Detection and Control Delay	T <sub>D_OCP</sub>			100		ns
<b>Power MOSFET Section (Drain Pin)</b>						
Breakdown Voltage	JW1501A	V <sub>BR</sub>		600		V
	JW1501B			650		
MOS R <sub>dson</sub>	JW1501A	R <sub>dson</sub>		3.3		ohm
	JW1501B			2.5		

<i>Over Temperature Protection</i>						
Thermal Shutdown	TSD	(Note 5)	---	165	--	°C
Thermal Recovery	TRC	(Note 5)	---	135	--	°C

**Note:**

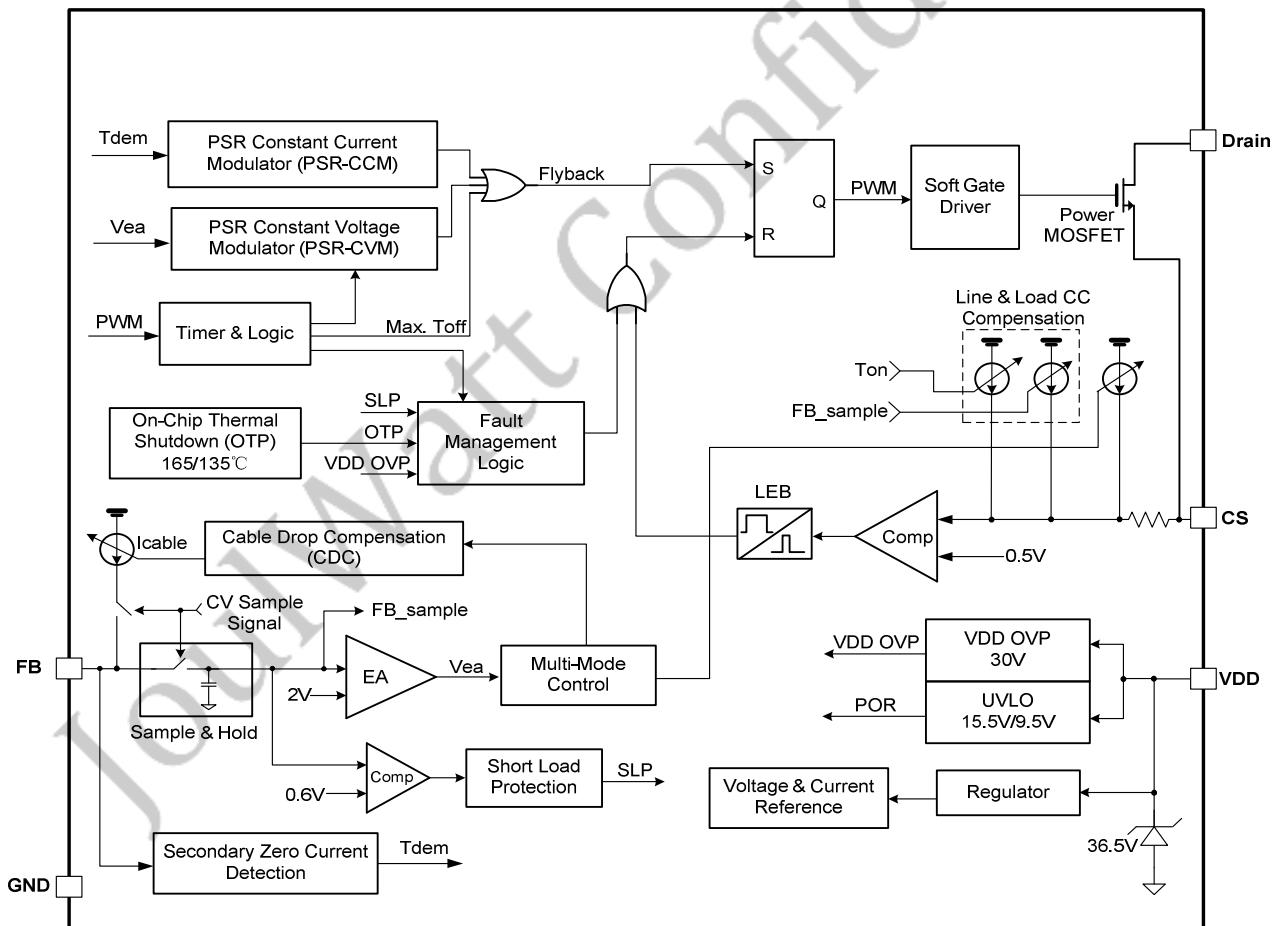
- 4) Guaranteed by design.
- 5) Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50°C ambient.

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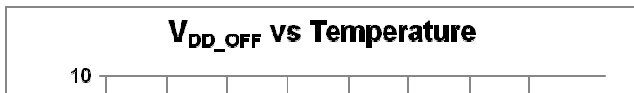
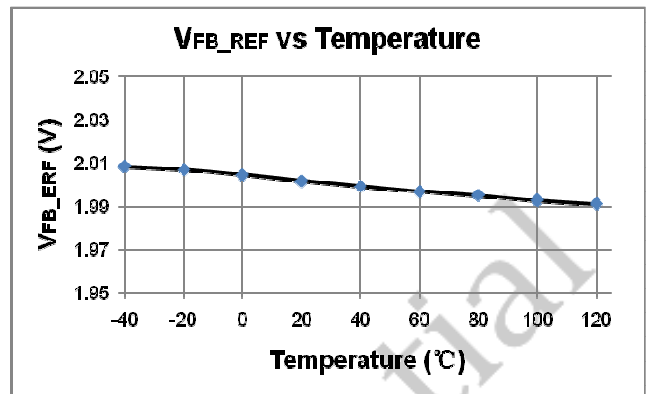
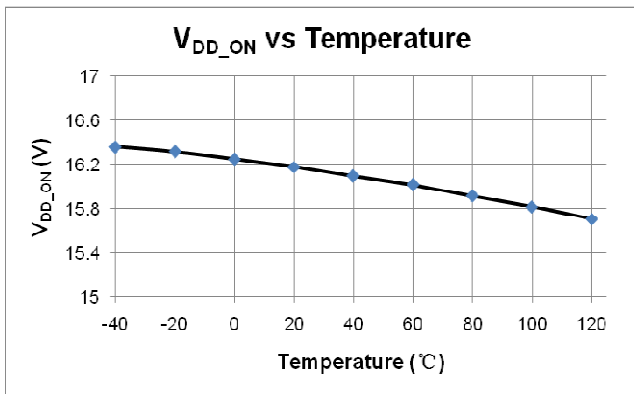
**PIN DESCRIPTION**

Pin	Name	Description
1	VDD	Power Supply Pin of the Chip.
2	GND	The Ground of the IC
3	FB	System feedback pin which regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding.
4	CS	Current Sense Input Pin.
5,6,7,8	Drain	The Power MOSFET Drain

**BLOCK DIAGRAM**



TYPICAL PERFORMANCE CHARACTERISTICS



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**FUNCTIONAL DESCRIPTION**

JW1501A/B is a multi-mode, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

**System Start-Up Operation**

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches UVLO turn-on voltage of 16.3V (typical), JW1501A/B begins switching and the IC operation current is increased to be 1mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

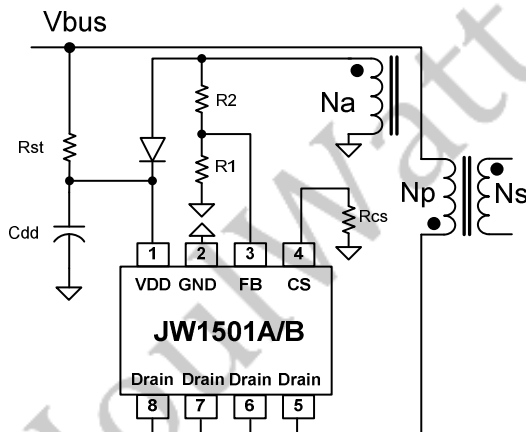


Fig.1

Once JW1501A/B enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 0.5mA typically, which helps to reduce the standby power loss.

**PSR Constant Voltage Modulation (PSR-CVM)**

In primary side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates the CV sampling signal timing waveform in JW1501A/B. As shown in Fig.2, it is clear that there is a down slope representing a decreasing total rectifier VF and its voltage drop as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the CV sampling signal blocks the leakage inductance reset and ringing. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the PSR Constant Voltage Modulator (PSR-CVM) for CV control. The internal reference voltage for EA is trimmed to 2V with high accuracy.

During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for “demagnetization plateau”, where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively.

When system enters over load condition, the output voltage falls down and the FB sampled voltage should be lower than 2V internal reference which makes system enter CC Mode automatically.

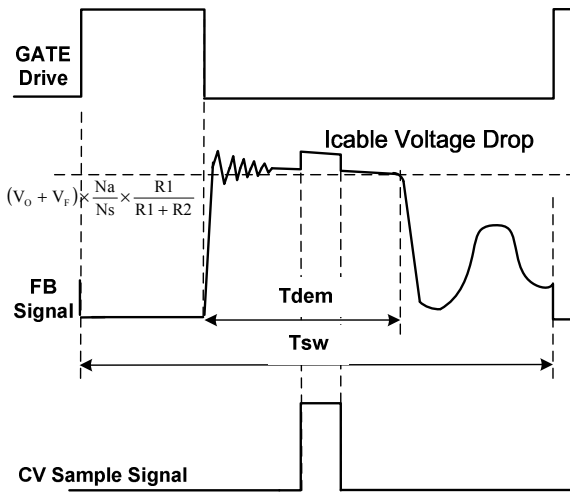


Fig.2

**PSR Constant Current Modulation (PSR-CCM)**

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at  $I_{pp(max)}$ , as shown in Fig.3.

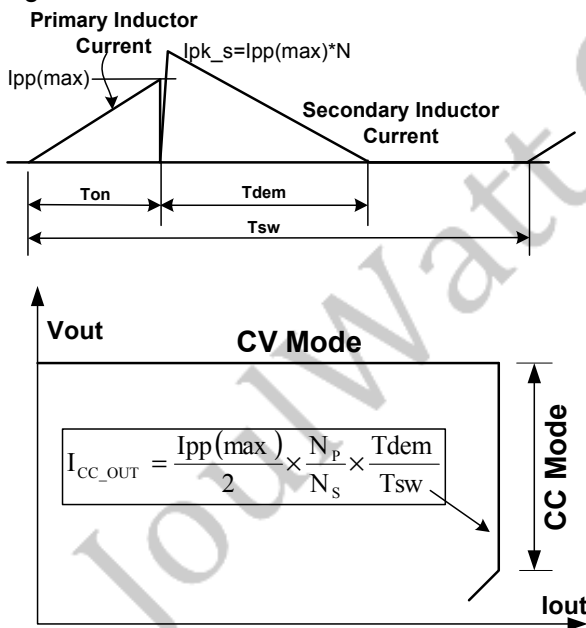


Fig.3

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time ( $T_{dem}$ ), and switching period ( $T_{sw}$ ) determines the secondary average output current  $I_{out}$ . Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3. When the average output current  $I_{out}$  reaches the regulation reference in the PSR Constant Current Modulator (PSR-CCM) block,

the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

In JW1501A/B, the ratio between  $T_{dem}$  and  $T_{sw}$  in CC mode is 1/2. Therefore, the average output current can be expressed as:

$$I_{PSR\_CC\_OUT} (mA) \cong \frac{1}{4} \times N \times \frac{500mV}{R_{cs}(\Omega)}$$

In the equation above,

$N$ ---The turn ratio of primary side winding to secondary side winding.

$R_{cs}$ --- the sensing resistor connected between the power MOSFET source to GND.

**Multi- Mode Control in CV Mode**

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in JW1501A/B which is shown in the Fig 4.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.

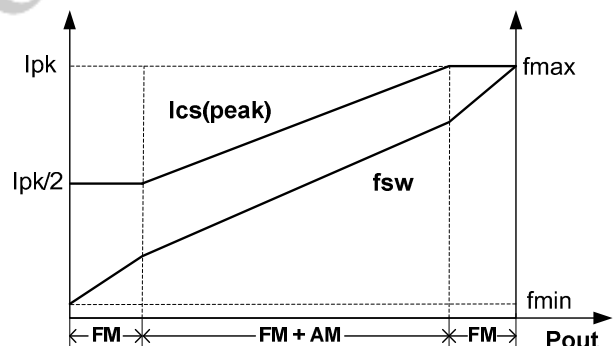


Fig.4

**Programmable Cable Drop Compensation (CDC) in CV Mode**

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In JW1501A/B, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power  $P_{out}$ . Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of  $R_1$  and



R2 (as shown in Fig.), the cable loss compensation can be programmed. The percentage of maximum compensation is given by

$$\frac{\Delta V(\text{cable})}{V_{\text{out}}} \approx \frac{I_{\text{cable\_max}} \times (R1/R2)}{V_{\text{FB\_REF}}} \times 100\%$$

For example, R1=3KΩ, R2=18KΩ, The percentage of maximum compensation is given by:

$$\frac{\Delta V(\text{cable})}{V_{\text{out}}} = \frac{63\mu\text{A} \times (3\text{K}/18\text{K})}{2\text{V}} \times 100\% = 8.1\%$$

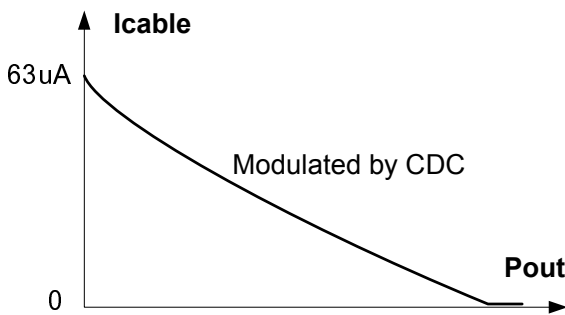
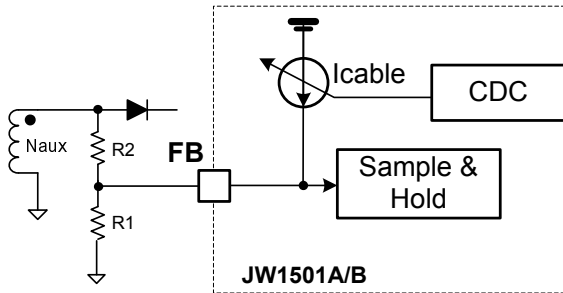


Fig.5

**Optimized Dynamic Response for PSR**

In JW1501A/B, the dynamic response performance is optimized to meet USB charge requirements.

**Audio Noise Free Operation for PSR**

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation.

In JW1501A/B, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

**Short Load Protection (SLP)**

In JW1501A/B, the output is sampled on FB pin and then compared with a threshold of UVP (0.7V typically) after an internal blanking time (10ms typical).

In JW1501A/B, when sensed FB voltage is below 0.7V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

**VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than 30V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD\_OFF (typical 9V) and then the system will restart up again. An internal 34.5V (typical) zener clamp is integrated to prevent the IC from damage.

**On Chip Thermal Shutdown (OTP)**

When the IC temperature is over 165°C, the IC shuts down. Only when the IC temperature drops to 135°C, IC will restart.

**Pin Floating Protection**

In JW1501A/B, if pin floating situation occurs, the IC is designed to have no damage to system.

**Soft Totem-Pole Gate Driver**

JW1501A/B has a soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp is added for power MOSFET gate protection when high VDD input.

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