JW15158K

Offline QR GaN Flyback Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW15158K is an isolated offline Flyback converter with GaN integrated, which features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and benefits EMI performance with nature frequency variation. And an internal frequency limitation is utilized to overcome the inherent disadvantages of QR Flyback.

The JW15158K comprises a HV pin for startup to eliminate conventional startup resistor and save standby mode energy consumption. Also, the HV pin is used for X-cap discharge when AC input is removed, which helps to reduce X-cap discharge loss and achieve extremely low standby power loss.

The JW15158K is available in ESOP10 package. The high level of integration provides an easy-to-use, low component count and high efficiency application solution for isolated power delivery.

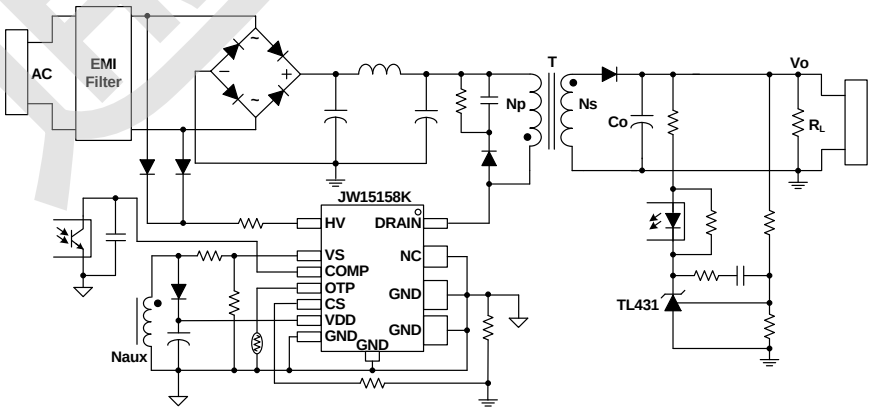
FEATURES

- Integrated 650V GaN
- Built-in High-Voltage Startup
- X-capacitor Discharge Function
- Wider VDD Operation Range
- QR Operation for High Efficiency
- Optional OCP and OPP Function for Different PD and QC Output Application
- Very Low Standby Power Consumption
- Cycle-by-Cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP, Brown-In, Brown-out, CS Open Protection, OCP, OPP, OLP, External OTP and Internal OTP
- Frequency Jitter to Ease EMI Compliance
- Available in ESOP10 Package

APPLICATIONS

- PD and QC Chargers
- AC/DC Adapters with Wide Output Range

TYPICAL APPLICATION



电话:0755-83387360 手机：13826508770（王先生） 邮箱：3007605919@qq.com 网址：www.sztssd.com 地址:深圳市福田区中航路鼎诚国际南座18楼1814室

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW15158KESOPAX#TR	ESOP10	J15158K YW□□□□□	Green

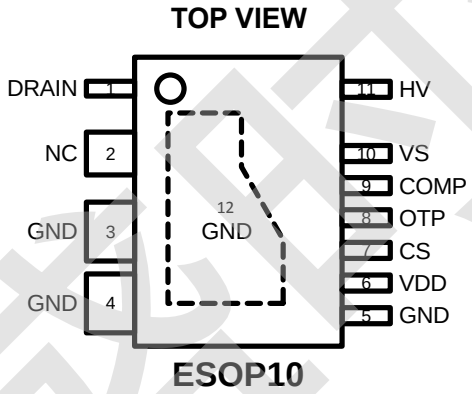
Notes:

1) JW□□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

2) Line1: J □□□□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

HV Voltage 700V
DRAIN Pin 650V
VDD Pin 95V
COMP, OTP, CS Pin ..... -0.3V to 5V (5V to 5.5V<10us)
VS Pin ..... -0.3V to 5V (-0.75V to -0.3<10us, 5V to 5.5V<10us)
Junction Temperature[2)] 150ºC
Storage Temperature ..... -65ºC to 150ºC
Lead Temperature (Soldering, 10sec.) 260ºC

RECOMMENDED OPERATING CONDITIONS [3)]

VDD Voltage ..... 8V to 83V
Operating Junction Temperature (T_J) ..... -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
ESOP10	TBD	TBD

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW15158K includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

T_A = 25ºC, unless otherwise stated.

Advance Information, not production data, subject to change without notice.

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
High Voltage Section (HV Pin)						
Supply Current from HV Pin	I_{HV}	V_{HV}=120V, V_{VDD}=0V	2.5	3	3.5	mA
Leakage Current of HV Pin	I_{HV_LK}	V_{HV}=500V, V_{VDD}=20V			30	uA
Brown-In Threshold	V_{BR_IN}	V_{HV} increasing	104	112	120	V
Brown-Out Threshold	V_{BR_OUT}	V_{HV} decreasing	90	97	105	V
Brown-Out Blanking Time[6]	t_{BR_OUT}		50	62	73	ms
Supply Voltage Section (VDD Pin)						
Turn-On Threshold Voltage	V_{DD_ON}	V_{VDD} increasing	15	16.5	18	V
Turn-Off Threshold Voltage	V_{DD_OFF}	V_{VDD} decreasing	7	8	9	V
Reset Threshold Voltage	V_{DD_RST}	Fault State	4	4.75	5.5	V
Startup Current	I_{DD_ST}	V_{VDD}=V_{DD_ON}-0.5 V	200	275	350	uA
Operating Supply Current	I_{DD_OP}	V_{VDD}=20V, f_S=f_{max}	0.5	0.75	1	mA
VDD OVP Voltage	V_{DD_OVP}	V_{VDD} increasing	88.5	91	94.5	V
Voltage Sense Section (VS Pin)						
Maximum VS Source Current Capability	I_{VS_MAX}	V_{VS}=-0.4V	2.5	2.9	3.3	mA
Adaptive Blanking Time for VS Sampling[5]	t_{VS_BLK}	V_{COMP}=0.55V		0.6		us
		V_{COMP}=4V		1.2		us
Output OVP Threshold	V_{VS_OVP}	V_{VS} increasing	2.85	3	3.25	V
Output OVP Debounce Cycle Counts[5]	N_{VS_OVP}	Fault State		3		Cycle
Current Sense Section (CS Pin)						
Max CS Offset Current	I_{CS_MAX}	V_{COMP}=4V	95	100	105	uA
Min CS Offset Current	I_{CS_MIN}	V_{COMP}=0V at Burst Mode	22	27	32	uA
CS Off Threshold	V_{CS_TH}	V_{CS} decreasing	10	30	50	mV
Leading-Edge Blanking Time[5]	t_{LEB}	V_{CS}=0		220		ns
OCP Enable Threshold	V_{OCP_EN}		0.61	0.65	0.69	V
OCP Internal Threshold[5]	V_{OCP}			0.2		V
OCP Blanking Time[6]	t_{OCP_BLK}	Fault State	85	105	125	ms
Auto-Restart Cycles for OCP[6]	N_{OCP_HIC}	Fault State		4		Cycle
OPP Internal Threshold[5]	V_{OPP}			0.8		V
OPP Blanking Time[6]	t_{OPP_BLK}	Fault State	85	105	125	ms
Auto-Restart Cycles for OPP[6]	N_{OPP_HIC}	Fault State		4		Cycle

CS OVP Threshold	V_{CS_OVP}			2		V
Frequency Section						
Maximum Switching Frequency	f_{max}	V_{COMP}=3.5V	180	205	230	kHz
Minimum Switching Frequency	f_{min}	V_{COMP}=0.8V	21	25	29	kHz
Maximum ON Time	T_{ON_MAX}		15	18	21.5	us
Minimum ON Time	T_{ON_MIN}		240	295	350	ns
Maximum Switching Cycle	T_{S_MAX}		52	61	70	us
Frequency Jittering Amplitude[5)]	ΔF_{JIT}			±7%		
Counting Cycles for Jittering[5)]	N_{JIT_CYC}			32		Cycle
Feedback Section (COMP Pin)						
Open Pin Voltage[6)]	V_{COMP_MAX}	Open Loop		4		V
Internal Pull-Up Resistor[5)]	R_{COMP_UP}			20		kΩ
COMP to CS Offset Current Gain[5)]	G_{COMP_CS}	COMP > 2.8V		20		V/mA
		COMP < 1.0V		16		V/mA
Threshold Enter PFM Mode	V_{COMP_PFM}	V_{COMP} decreasing	2.6	2.8	3	V
Threshold Enter PWM Mode	V_{COMP_PWM}	V_{COMP} decreasing	0.9	1	1.1	V
Threshold Enter Burst Mode	V_{BUR_L}	V_{COMP} decreasing	0.47	0.5	0.53	V
Threshold Exit Burst Mode	V_{BUR_H}	V_{COMP} increasing	0.56	0.6	0.63	V
Over Load Protection Threshold[6)]	V_{OLP}	Fault State		3.7		V
OLP Blanking Time[6)]	t_{OLP_BLK}	Fault State	85	105	125	ms
Auto-Restart Cycles for OLP[6)]	N_{OLP_HIC}	Fault State		4		Cycle
GaN Section						
Drain-source On-state Resistance	R_{DS_ON}	V_{GS}=6V,T_J=25℃		165	260	mΩ
External Over Temperature Protection (OTP Pin)						
Over Temperature Protection (OTP) Enter Threshold	V_{OTP_IN}	V_{OTP} decreasing	220	255	290	mV
Over Temperature Protection (OTP) Exiting Threshold	V_{OTP_OUT}	V_{OTP} increasing	460	495	530	mV
OTP Pull-Up Current Source	I_{OTP}		23	27.5	32	uA
Internal Over Temperature Protection						
Thermal Shutdown Threshold[6)]	T_{OTP}	Internal junction temperature		140		°C
OTP Hysteresis[6)]	T_{HYS}	Internal junction temperature		30		ºC

Note：

5) Guaranteed by design.

6) Derived from bench characterization. Not tested in production.

PIN DESCRIPTION

PIN ESOP10	NAME	DESCRIPTION
1	DRAIN	Drain terminal of the Internal GaN.
2	NC	
3, 4, 5, 12	GND	The ground of IC.
6	VDD	Bias power input to the controller. A hold-up capacitor to GND is required.
7	CS	Current sensing input pin. This pin sense the primary switch current for peak current control and OCP. Besides, this pin is used to choose OCP or OPP function at the initial start.
8	OTP	External temperature sensing pin. An external NTC (negative temperature coefficient) thermistor to GND is required.
9	COMP	Feedback input pin for Flyback QR controller. Connect to an opto-coupler.
10	VS	Voltage sensing input pin. Coupled to the auxiliary winding via a resistor divider to monitor the output voltage for OVP protection. This pin also detects the resonant valley to implement QR operation.
11	HV	High voltage input pin. This pin provides source current to charge VDD. This pin is used for X-cap discharge when AC input is removed. Besides, this pin also senses input voltage for brown-in and brown-out protection.

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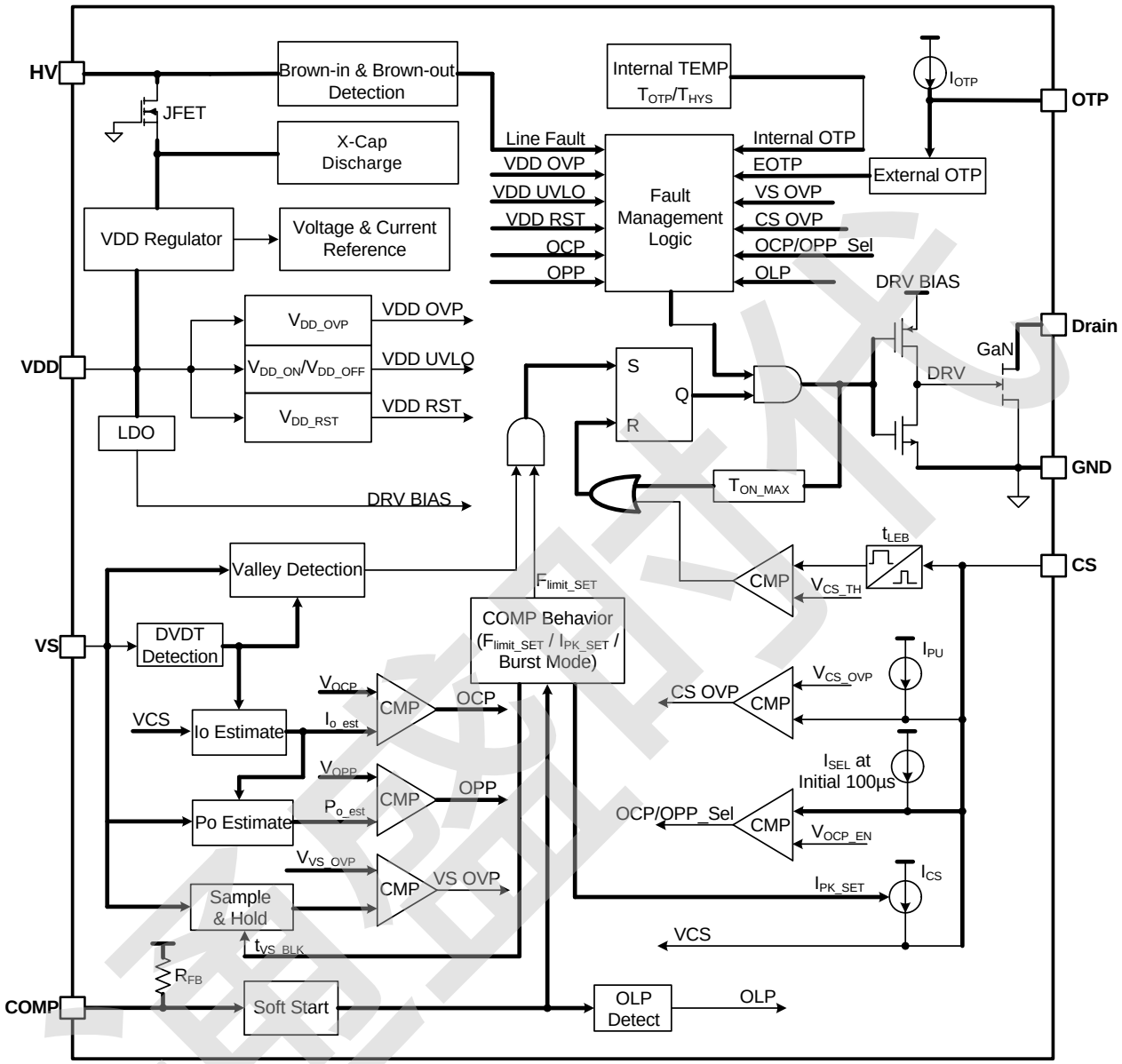
BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The JW15158K is an offline flyback converter with GaN integrated, which features multi-mode quasi-resonant (QR) operation. The Quasi-Resonant (QR) with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

JW15158K has an inherent frequency jittering mechanism to improve EMI performance under QR operation.

1. Start-Up

1.1. HV Start-Up

When HV pin is connected to AC rectified voltage, a current source which is drawn from HV pin charges VDD capacitor. As soon as VDD pin voltage reaches turn-on threshold V_{DD_ON}, the controller starts switching and internal start-up circuit is disabled. The controller stops switching and start-up current source is turned on again when a fault is triggered or VDD voltage falls below V_{DD_OFF}.

1.2 Soft-Start

In the absence of a detected fault, the converter begins to work normally along with soft start. The internal soft-start time is within 4ms with the feedback signal V_{COMP} rising gradually from minimum level to maximum level. Every restart up is followed by a soft start.

2. Normal Operation

After the converter start-up, it enters normal operation. The JW15158K realizes output adjustment based on the feedback signal transmitting to the primary-side controller by the opto-coupler.

The JW15158K is a multi-mode QR converter with secondary-side regulation. According to the feedback signal V_{COMP}, the converter operates in different modes for efficiency optimization. Fig.1 illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in Fig.1.

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to f_{max}. For medium-load range, the Pulse Frequency Modulation (PFM) is used and primary peak current is nearly fixed to achieve high efficiency. When load is further reduced, switching frequency is fixed at f_{min} along with primary peak current varying from 50% to 25% of its maximum. When the system is at very light load condition, the control mode of JW15158K changes to burst mode. When the voltage of COMP pin drops below V_{BUR_L} (0.5V typically), the drive stops. The drive will resume when the voltage of COMP pin rises back to V_{BUR_H} (0.6V typically). Otherwise, the internal GaN remains at off state to minimize the switching loss and reduce the standby power consumption. Transitions between modes are automatically accomplished by the controller depending on the feedback signal, V_{COMP}.

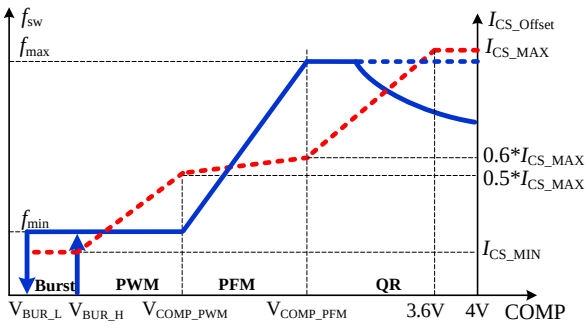

Fig.1 Frequency & Ipk Modulation

3. Other Functions and Features

3.1 Frequency Jittering

To achieve good EMI performance, frequency jittering method is integrated in JW15158K. Jittering with an amplitude of ΔF_{JIT} around the center value. The modulation cycle is determined by counting consecutive 32 switching cycles.

3.2 Lead Edge Blanking (LEB)

In order to avoid the premature termination of switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between CS pin and the input internal current comparator. The current comparator is disabled and can't turn off the internal GaN during the blanking time. Fig.2 shows the leading edge blanking time.

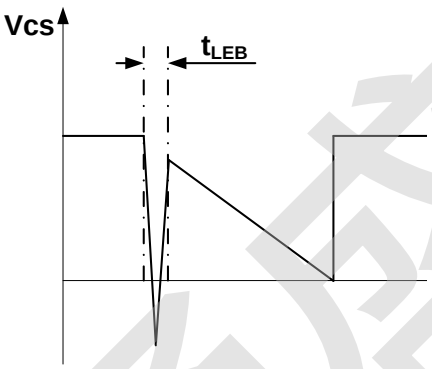

Fig.2 LEB Blanking

3.3 CCM Preventing

For JW15158K, when the primary-side peak current exceeds the value decided by the feedback signal V_{COMP}, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after a T_{S_MAX} to make sure the system operates in DCM.

3.4 X-Cap Discharge Function

Safety standards such as EN60950 and UL62368 require that any X-caps in EMI filters on the AC side of the bridge rectifier quickly discharge to a safe level when AC is disconnected. Standards require that the voltage across X-caps decay with a maximum time constant of 2s. Typically, this requirement is achieved by a resistive discharging element in parallel with X-caps. However, this resistance will cause a continuous power dissipation that impacts the standby power consumption.

In order to reduce standby power consumption, JW15158K incorporates a X-cap discharge circuit. This circuit periodically monitors the voltage across X-caps to detect any possibility that AC cord is unplugged, and then discharge the X-caps by internal HV discharging current source to a safe level within 2s. Figure 3 shows the X-cap discharge timing.

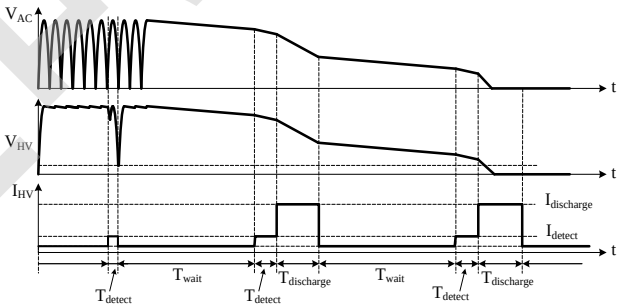

Figure. 3 X-cap Discharge Timing

3.5 VS Blanking Time

VS spikes are affected by the amplitudes of Ipk and inductance, so VS blanking time should be set to vary with Ipk. Ensure that the secondary side conduction time is greater than the VS blanking time t_{BLK}.

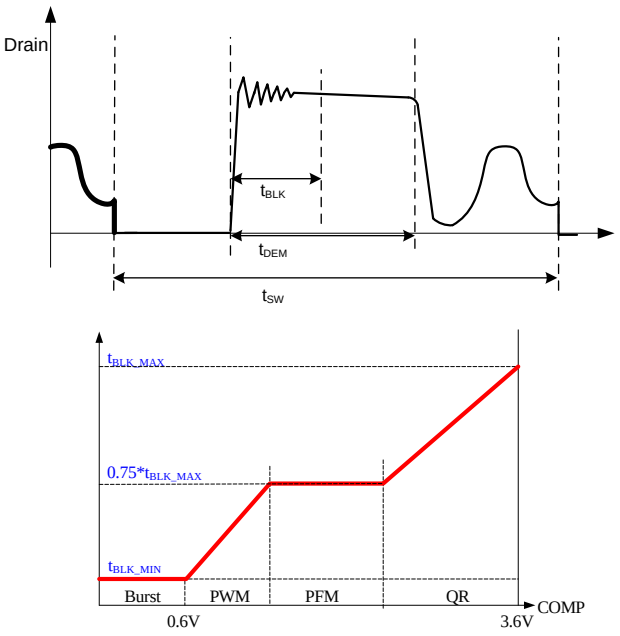

Fig.4 VS Blanking Time

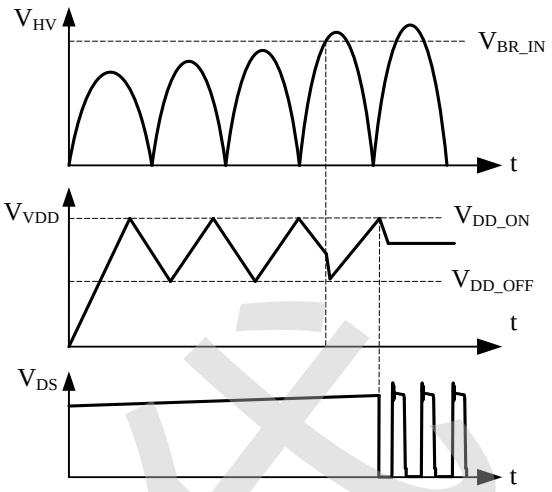

Fig.5 Brown-In at Drain Terminal

4. Protection

4.1 CS Pin Open Protection

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin, increasing the V_{CS}. If V_{CS} is above V_{CS_OVP} (2V typically), a CS pin open fault triggered. The controller shuts down, then VDD resets and fault restart cycle begins.

4.2 Input Brown-in and Brown-out

The JW15158K senses HV voltage to realize brown in function. When HV voltage is higher than V_{BR_IN} (112V typically), a 5mA pull down current will be applied to VDD pin to make VDD hit V_{DD_OFF}. When VDD reaches V_{DD_ON} again, the controller starts switching.

The controller is disabled when HV voltage is lower than V_{BR_OUT} (98V typically) for brown-out blanking time t_{BR_OUT}. The blanking time is set long enough to ignore a two cycle drop out. The timer starts counting once HV voltage drops below V_{BR_OUT}.

4.3 Output OVP (VS OVP)

The output over voltage protection is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds V_{VS_OVP} for three consecutive switching cycles, an VS_OVP fault is asserted, and then the device shuts down, the UVLO reset and re-start fault cycle begins.

4.4 OCP or OPP Selection Circuit

In some PD or QC applications, the maximum output current at different output voltage differs much. So OCP should be disabled, and the alternative OPP is enabled. JW15158K senses CS voltage at initial start to determine whether to use OCP or OPP function as Fig.6 shows. At the initial 100us, an OCP/OPP selection current I_{SEL} (100uA, typically) is applied to CS pin. If CS voltage exceeds a preset enable threshold V_{OCP_EN}, OPP is enabled and OCP is disabled. Otherwise, OPP is disabled and OCP is enabled.

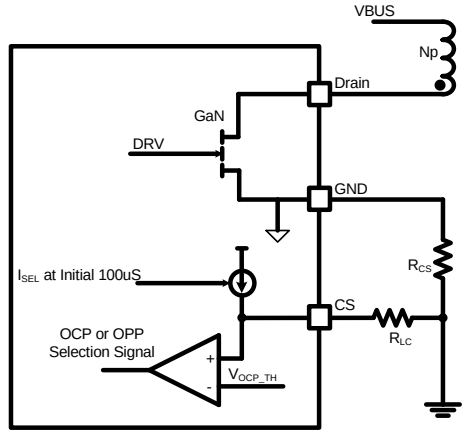

Fig.6 OCP or OPP Selection Circuit

4.5 OCP

If OCP is enabled, JW15158K compares estimated output average current and OCP threshold. The output average current is calculated at the primary side. When the primary switch turns off, the peak inductor current I_{pk} is sampled and hold for output current calculation.

As shown in Fig.7, it calculates output current based on secondary side current conduction time t_{ons} and primary side current information V_{CS}. If the calculated output current signal, I_{o_est} is higher than the internal OCP threshold V_{OCP} (0.2V typically) for an OCP blanking time t_{OCP_BLK}, IC enters OCP protection.

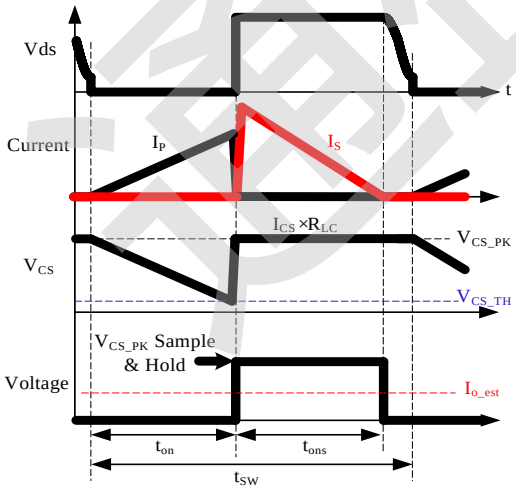

Fig.7 Output Current Estimation

So, the OCP point can be set as:

$$I_{OCP} = \frac{V_{OCP} \cdot \left(1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}\right)}{2R_{CS}} \cdot \frac{N_P}{N_S} \quad (1)$$

wherein, N_P is the turns number of primary winding, N_S is the turns number of secondary winding, R_{CS} is the current sensing resistance.

When an OCP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.6 OPP

If OPP is enabled, JW15158K compares estimated output power and OPP threshold. The output power is calculated at the primary side based on the estimated output average current in OCP and the output voltage according to VS voltage. So the output power can be expressed as:

$$P_{o\_est} = \frac{V_{CS\_PK} - V_{CS\_TH}}{2R_{CS}} \cdot \frac{N_P}{N_S} \cdot \frac{t_{ons}}{t_{SW}} \cdot \frac{V_S \cdot N_S}{N_{aux}} \cdot \frac{R_{DOWN} + R_{UP}}{R_{DOWN}} \quad (2)$$

And the OPP point can be set as:

$$P_{OPP} = \frac{V_{OPP} \cdot \left(1 - \frac{V_{CS\_TH}}{V_{CS\_PK}}\right)}{2R_{CS}} \cdot \frac{N_P}{N_{aux}} \cdot \frac{R_{DOWN} + R_{UP}}{R_{DOWN}} \quad (3)$$

wherein, N_{aux} is the turns number of auxiliary winding, N_P is the turns number of primary winding, R_{UP} and R_{DOWN} are the resistances of the outside resistor divider of VS pin.

If the calculated output power signal is higher than the internal OPP threshold V_{OPP} (0.8V typically) for an OPP blanking timer t_{OPP_BLK}, IC enters OPP protection. When an OPP fault is

asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.7 Over Load Protection

If the voltage on COMP pin continues exceeds the Over-Load protection threshold V_{OLP} more than an OLP blanking time t_{OLP_BLK}, an OLP fault is asserted. The device shuts down, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.8 VDD OVP

If the voltage on VDD pin continues exceeds the Over-Voltage protection threshold V_{DD_OVP} more than 100us, a VDD_OVP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.9 External OTP

An external NTC resistor (R_{NTC}) is coupled to OTP pin to program a thermal shutdown temperature. The OTP shutdown threshold is V_{OTP_IN} with an internal pull-up current I_{OTP} flowing through R_{NTC}. Once the thermistor is lower than V_{OTP_IN}/I_{OTP}, an OTP fault triggered, and the V_{OTP_IN} threshold is increased to V_{OTP_OUT} (0.5V typically). The OTP resistance need to increase to above V_{OTP_OUT}/I_{OTP} to leave OTP. If user needs to disable this function, a 30kΩ resistor can be used to ensure that the OTP can not be triggered.

4.10 Internal OTP

The internal over temperature protection threshold is T_{OTP} (140°C typically). If the junction temperature of the device reaches this threshold, the device shuts down. Since the OTP hysteresis is 30°C typically, when the junction temperature falls below 110°C, the device initiates the UVLO reset and re-starts fault cycle.

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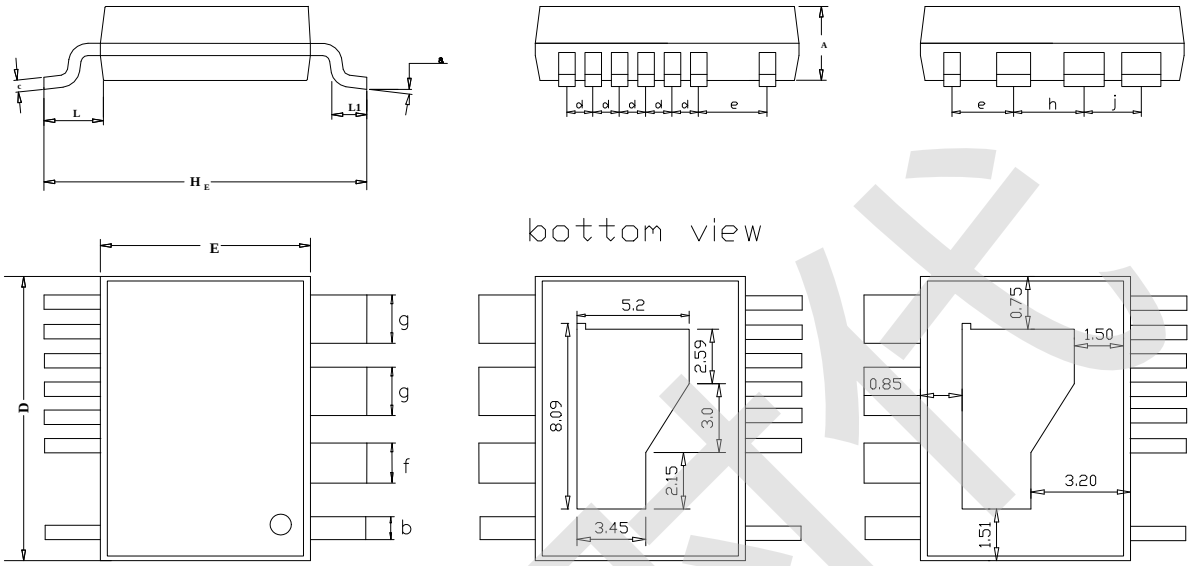
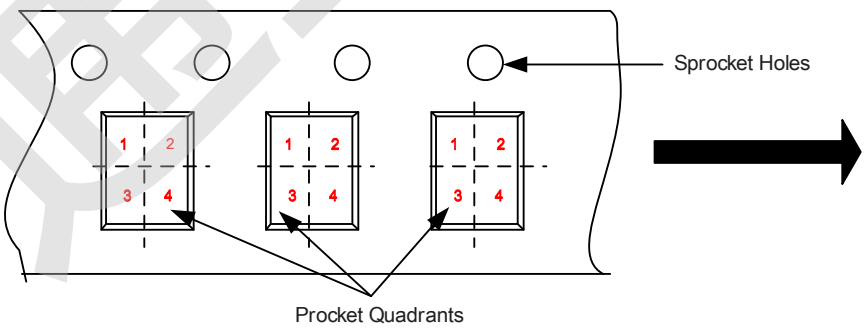
PACKAGE OUTLINE

ESOP10 UNIT: mm



Unit		A	C	D	E	HE	L	L1	a	b	d	e	f	g	h	j	∠
	max	1.7	0.30	10.1	7.7	10.4	1.5	0.8		0.45	1.32	2.59	1.25	1.96	3.34	2.35	
mm	typ	1.6	0.25	9.9	7.5	10.3	1.4	/	0.2 ref	0.40	1.27	2.54	1.20	1.91	3.29	2.30	
	min	1.5	0.20	9.7	7.3	10.2	1.3	0.4		0.35	1.22	2.49	1.15	1.86	3.24	2.25	7°
	max	67	12	398	303	409	59	31		18	52	102	49	77	131	93	
mil	typ	63	10	390	295	406	55	/	8 ref	16	50	100	47	75	130	91	
	min	59	8	382	287	402	51	16		14	48	98	45	73	128	89	

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
ESOP10	2

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