

Parameters Subject to Change Without Notice

DESCRIPTION

The JW[®]1532B is a high efficiency low cost off-line constant voltage regulator for Buck and Buck- Boost topology with 650V MOSFET.

JW1532B can output 18V/12V default voltage with few external components, which decreases the system cost. In light load condition, JW1532B operates in green mode, in which the inductor peak current and the switching frequency is lower than that of full load to improve the system efficiency and the reference voltage is decreased to ensure good load regulation.

JW1532B has multi-protection functions which largely enhance the safety and reliability of the system, including VDD under-voltage Lockout (UVLO), short circuit protection (SCP), pulse-by-pulse current limit, over load protection (OLP) and over-temperature protection (OTP).

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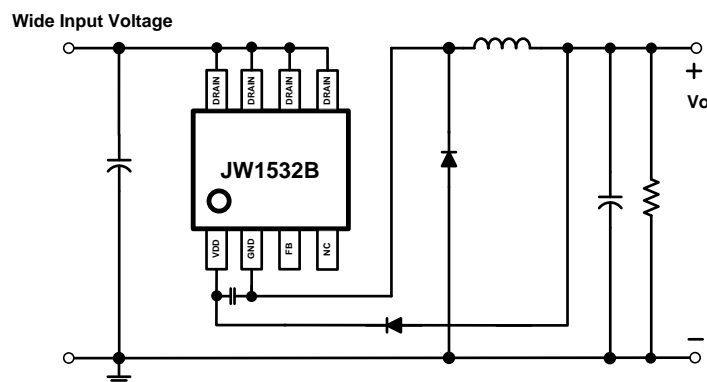
FEATURES

- Ultra low system BOM cost
- Integrated with 650V, low R_{dson} MOSFET
- 18V/12V default output voltage
- Support Buck and Buck-boost topology
- Peak current mode control
- Frequency Jittering for good EMC
- High efficiency over wide operating range
- Output voltage load regulation compensation
- VDD UVLO
- Short circuit protection
- Pulse-by-pulse current limit
- Over temperature protection
- SOP8 package

APPLICATIONS

- Home appliance
- Standby power
- Consumer electronics

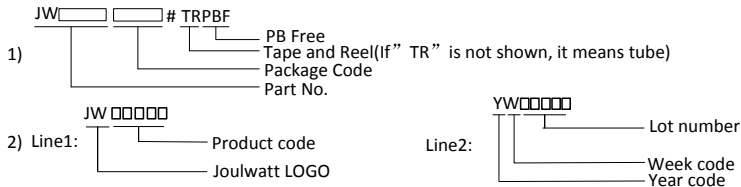
TYPICAL APPLICATION



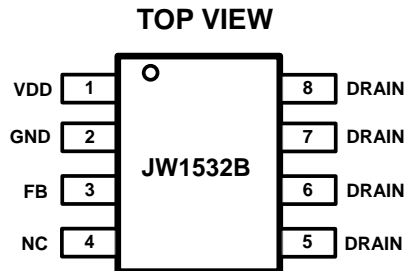
ORDER INFORMATION

DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
JW1532BSOPB#TRPBF	SOP8	JW1532B YW□□□□

Notes:



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

VDD Voltage to SOURCE.....	-0.3V to 30V
DRAIN Voltage to SOURCE.....	650V
FB/CS Voltage to GND.....	-0.3V to 6.5V
Junction Temperature ^{2) 3)}	150°C
Lead Temperature.....	260°C
Storage Temperature.....	-65°C to +150°C
ESD Susceptibility (Human Body Model)	2.5kV

RECOMMENDED OPERATING CONDITIONS

DRAIN Voltage.....600V
 Operating Junction Temp (T_J)-40°C to 125°C

Package	Recommended MAX Output Current (T _J =125°C) 4)
SOP8	500mA

THERMAL PERFORMANCE⁵⁾ θ_{JA} θ_{JC}

SOP8.....96.....45°C/W

Note:

- 1) Exceeding these ratings may damage the device.
- 2) JW1532B guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
- 3) The JW1532B includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 4) The maximum output current is recommended in the application according to chip junction temperature T_J=125°C (chip case temperature difference about 20°C). The maximum output current could be increased properly if the heat dissipation is better.
- 5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$T_A=25\text{ }^\circ\text{C}$, unless otherwise stated.						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
VDD Quiescent Current	I_Q	VDD=10V		50		μA
Operation Current	I_{OP}	VDD=10V			150	μA
VDD Charge Current	I_{CH}	VDD=5V			2	mA
VDD Startup Voltage	V_{DD_ST}			8.5		V
VDD Under Voltage Lockout	V_{DD_UVLO}			4.5		V
VDD Clamping Voltage	V_{CLP}			20		V
VDD Feedback Reference	V_{DDREF}	FB floating		18.4		V
		FB short to GND		12.4		V
Peak Current Limit	I_{PK}			0.8		A
Oscillator Frequency	f_{osc}			60		kHz
Frequency Jittering Range	$\Delta f/f_{OSC}$		-8		8	%
Frequency Jittering Period	T_{Jit}			15		ms
Maximum On Time	T_{ONMAX}			12		μs
Leading Edge Blanking Time	T_{LEB}			300	400	ns
MOS Breakdown Voltage	BV		650			V
MOS Rdson	Rdson	Vgs=10V		8		Ω
Over Thermal Protection Threshold ⁶⁾				150		$^\circ\text{C}$
Over Thermal Protection Recovery Hysteresis ⁶⁾				30		$^\circ\text{C}$

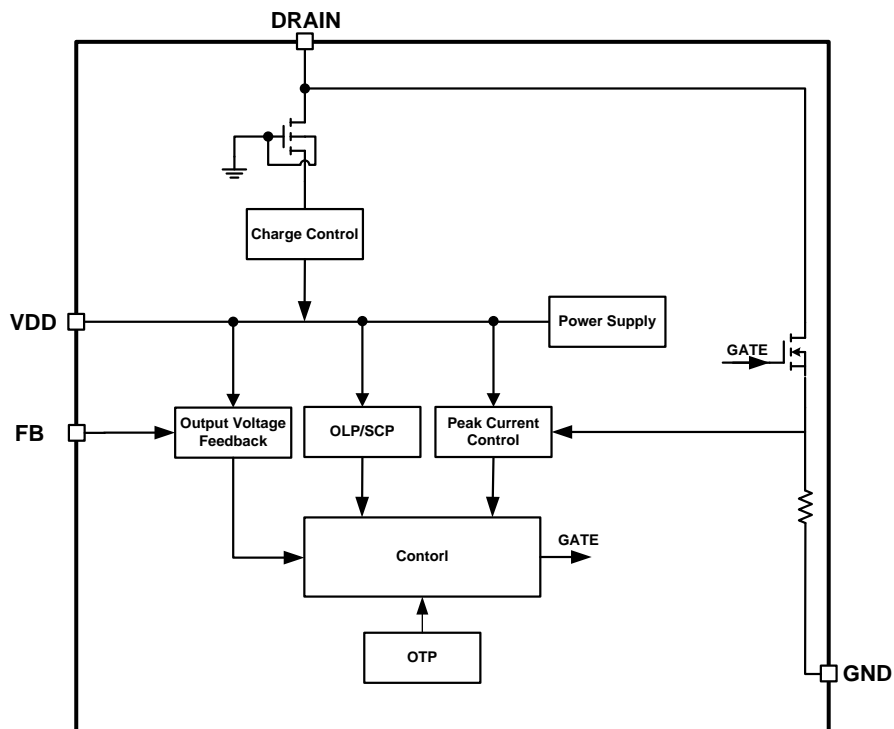
Note:

6) Guaranteed by design.

PIN DESCRIPTION

Pin SOP8	Name	Description
1	VDD	IC power supply and output voltage feedback
2	GND	IC ground
3	FB	Output voltage setup, FB floating-18V, FB short to GND-12V
4	NC	
5	DRAIN	Internal MOS drain and HV power supply
6	DRAIN	Internal MOS drain and HV power supply
7	DRAIN	Internal MOS drain and HV power supply
8	DRAIN	Internal MOS drain and HV power supply

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW1532B is a high efficiency low cost off-line constant voltage regulator for Buck and Buck-Boost topology.

Start Up

JW1532B can be supplied from MOS DRAIN directly. When the internal high voltage(HV) power source charges VDD up to the V_{DD_ST} , the gate driver starts to switch. VDD will be powered by output voltage in steady state. Once the voltage of VDD is lower than V_{DD_UVLO} , JW1532B stops switching.

Peak Current Control

JW1532B has the default peak current for 450mA output current. And it's also has the SCP limit peak current for abnormal state such as inductance short.

Constant Voltage Control

The output voltage is sensed by VDD pin and adjusted by internal control compensation loop automatically.

The switching frequency of JW1532B is fixed to f_{osc} with $\pm 8\%$ Jittering to improve the EMI performance.

Output voltage can be selected by FB pin setup. If FB is floating, output voltage is 18V, if the FB pin is short to GND, output voltage is 12V.

Green Mode

In light or no load condition, JW1532B operates

in DCM which means the OFF time is very long. JW1532B will reduce the peak current of the inductor to minimize the power loss. The longer T_{off} , the lower I_{PK} .

Short Circuit Protection (SCP)/ Over Load Protection (OLP)

In short circuit or over load condition, VDD can't be charged to V_{REF} . JW1532B will operate in auto-restart mode which is represented in the following description if $V_{DD} < V_{REF}$ for 120ms.

Auto-restart Mode

JW1532B will enter auto-restart mode if SCP/OLP/OTP is triggered. The chip stops switching and the HV power source is disconnected until VDD decreases to 4.5V. If VDD is charged to 4.5V for 24 times, the system restarts.

Over Temperature Protection

When internal temperature of the chip exceeds 150°C, JW1532B operates in auto-restart mode to help the chip cooling.

PCB Design

1. The VDD pin must be locally bypassed with a capacitor.
2. Make the area of the power loop as small as possible in order to reduce the EMI radiation.

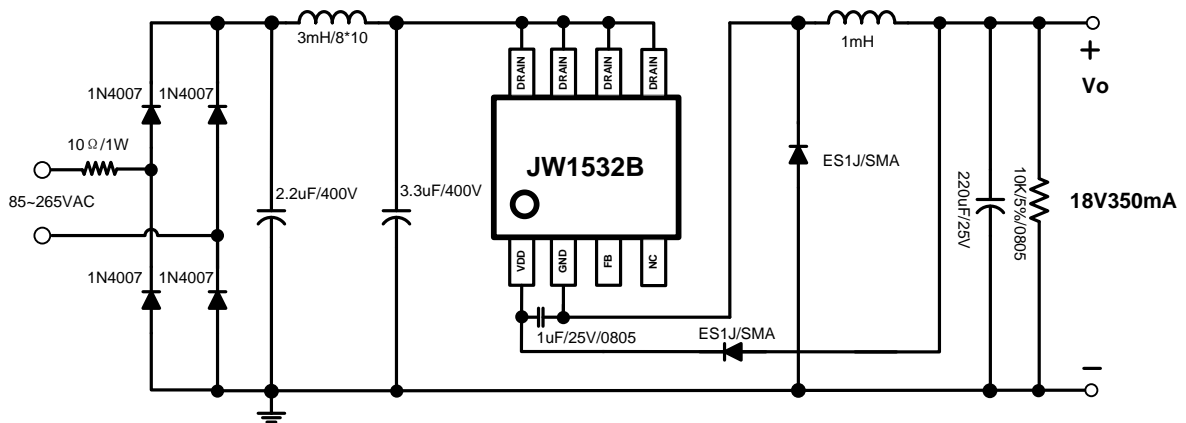
APPLICATION REFERENCE

The reference design is suitable for non-isolated buck power supply default 18V output, using JW1532B.

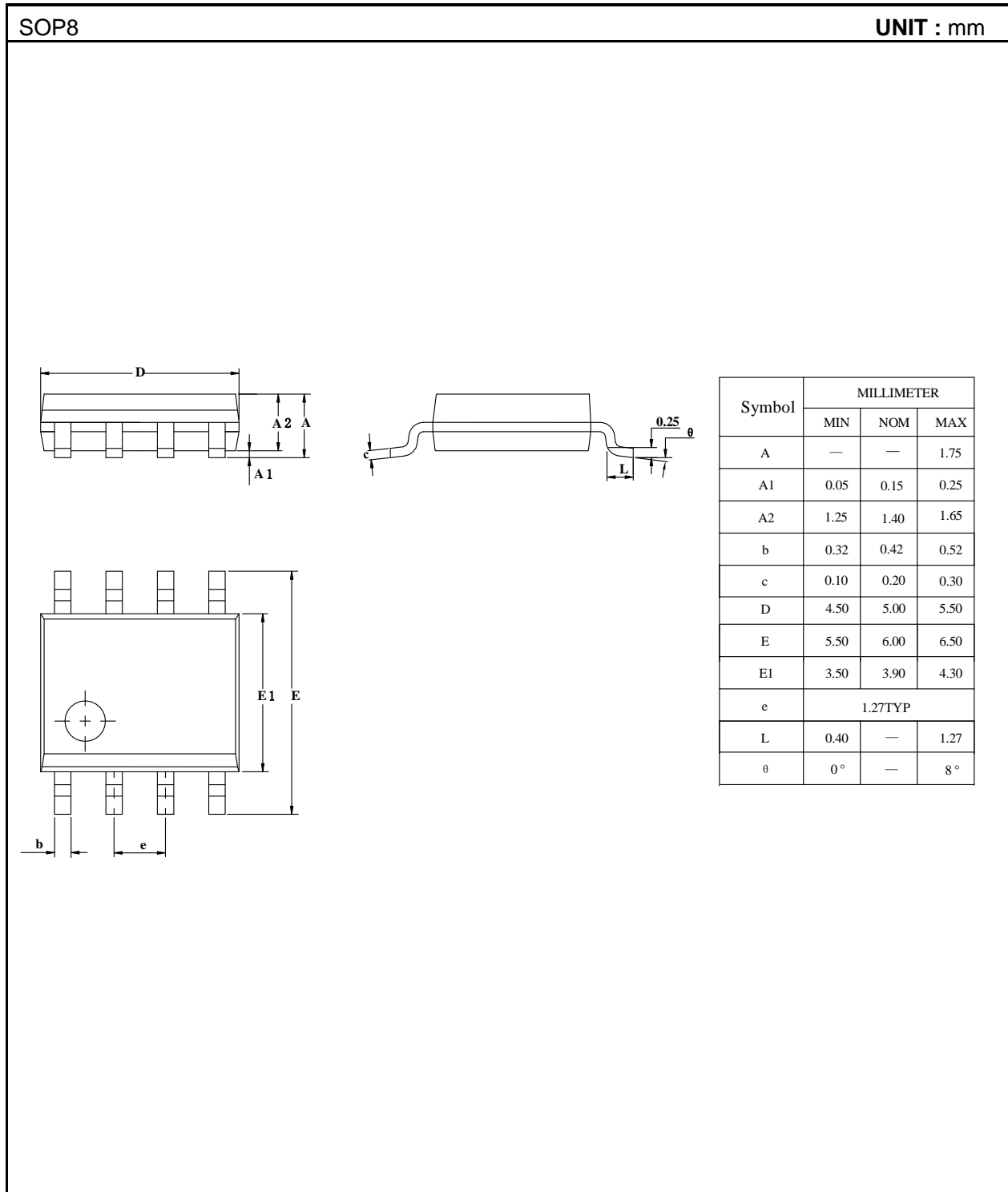
V_{IN}: 85~265VAC

V_{OUT}: 18V

I_{OUT}: 350mA



PACKAGE OUTLINE



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