JW3702

4-Switch Buck-Boost Charger Controller with I2C Interface

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®3702 is a synchronous 4-switch buck-boost controller capable of charging 1-4 cell Li-ion batteries with high light load efficiency and fast transient response. It can charge the battery from a wide range of input sources, such as USB adapter, high voltage USB PD sources and traditional adapters.

The JW3702 supports I2C serial communication interface to program a lot of parameters of the chip, offering a flexible solution for battery charging applications. An internal 10-bit ADC is provided to monitor the bus voltage, bus current, battery voltage, battery current and NTC resistor voltage, so user can monitor the system status in real time.

The device also supports OTG function to deliver power from battery to other portable devices through USB port. And the OTG voltage and current limit can be programmed by I2C interface.

The JW3702 guarantees robustness with battery/ OTG over-voltage protection, bus/ battery under-voltage protection, OTG/ battery over-current protection, charging timeout, watchdog and thermal shutdown.

The JW3702 is available in QFN4X4-32 package.

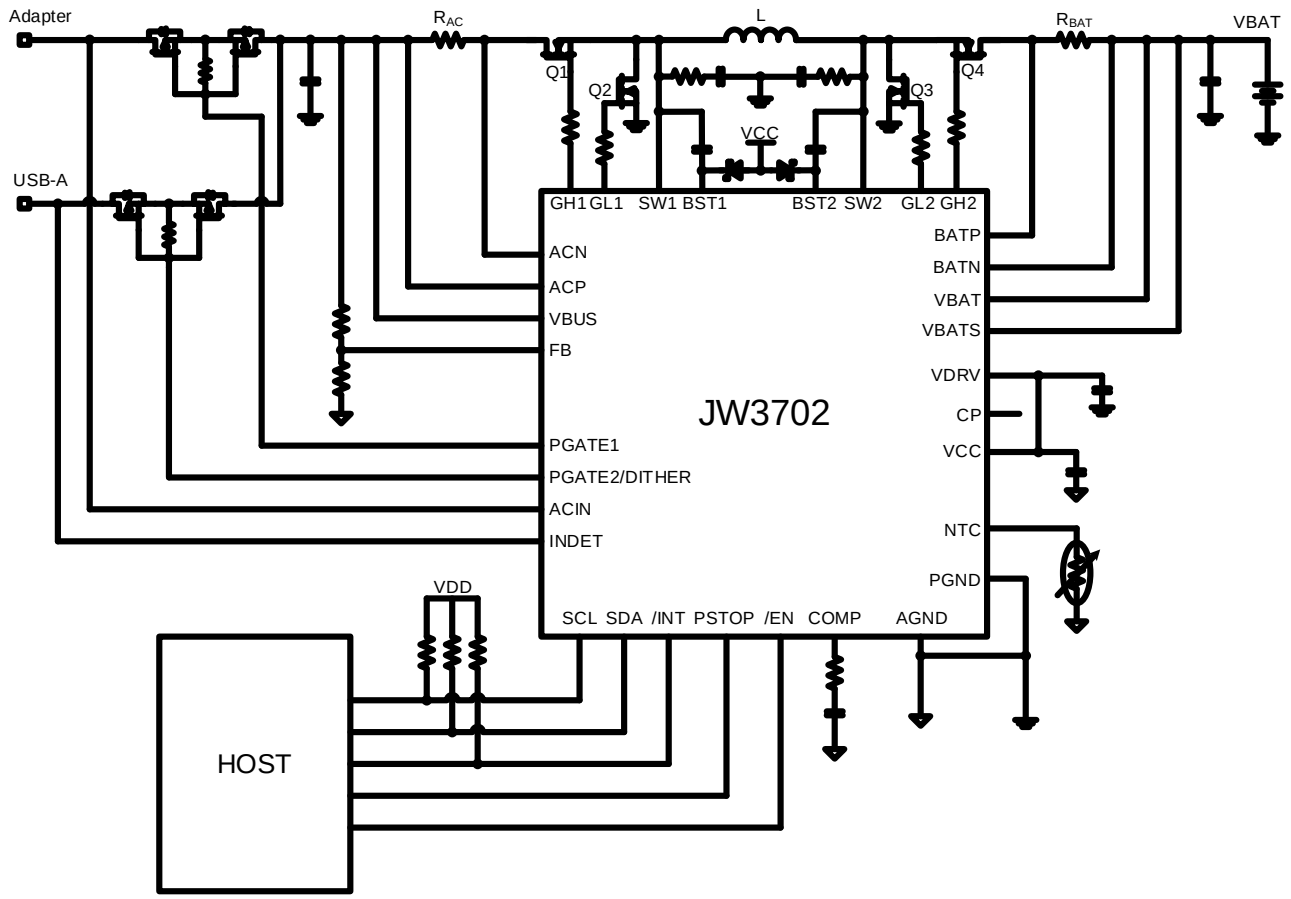
FEATURES

- Up to 28V breakdown voltage
- 3.0V to 24V input voltage range
- 2.4V to 24V OTG output voltage range
- Support 1-4 cell batteries charging and discharging
- 150kHz to 500kHz programmable switching frequency
- I2C interface supported
- Integrate 10-bit ADC to monitor bus voltage, bus current, battery voltage, battery current and NTC resistor voltage
- Integrate charge pump circuit to provide 6V drive voltage even with single cell application
- Safety
  - battery/OTG over-voltage protection
  - bus/battery under-voltage protection
  - OTG/battery over-current protection
  - charging timeout
  - watchdog protection
  - thermal shutdown
- Ultra-low quiescent current: 12uA (typical)
- Package: QFN4X4-32

APPLICATIONS

- Power bank
- USB Type-C PD
- USB-HUB
- Portable devices with rechargeable battery
- Industrial applications

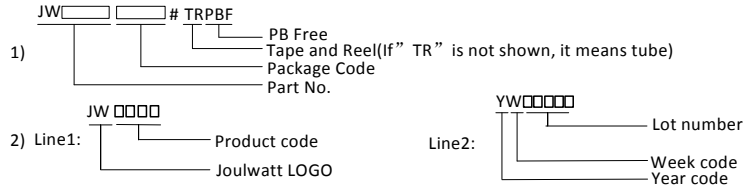
TYPICAL APPLICATION



ORDER INFORMATION

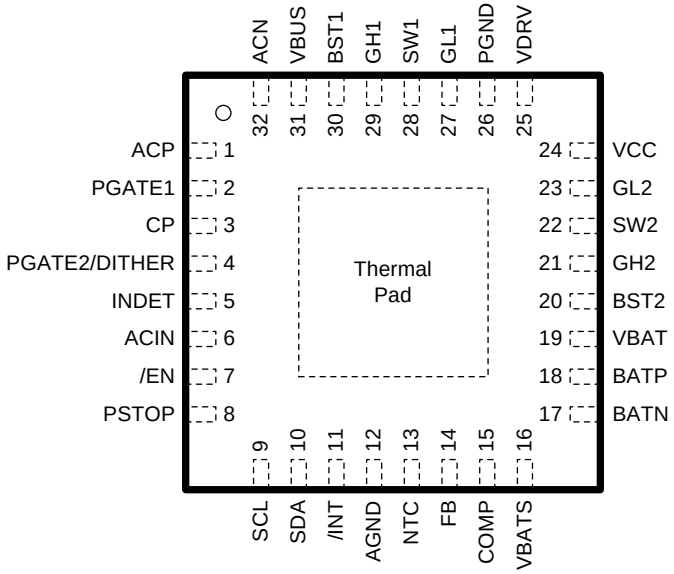
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW3702QFNK#TRPBF	QFN4X4-32	JW3702 YW□□□□□

Note：



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

INDET, ACIN, VBUS, ACP, ACN, VBAT, BATP, BATN, FB, VBATS .....-0.3V to 28V
SW1, SW2 .....-2.0V to 28V
/EN, PSTOP, PGATE1, PGATE2/DITHER .....-0.3V to 28V
BST1, BST2, GH1, GH2 .....-0.3V to 34V
BST1-SW1, BST2-SW2 ..... -0.3V to 7V
All Other Pins .....-0.3V to 7V
Junction Temperature[2)3)] .....-40ºC to 150ºC
Lead Temperature 260ºC
ESD Susceptibility (Human Body Model) .....±2kV

RECOMMENDED OPERATING CONDITIONS

Input Voltage VBUS .....3.0V to 24V
Battery Voltage VBAT .....3.0V to 24V
Operation Junction Temp (T_J) .....-40ºC to +125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
QFN4X4-32	37.2	26.1ºC/W

Note:

1) Exceeding these ratings may damage the device.

2) The JW3702 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) The JW3702 includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VBUS=10V, TA=25°C, unless otherwise stated						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Power supply						
Operation input voltage	V_{IN}		3.0		24	V
VBUS under-voltage lockout threshold	V_{BUS_UVLO}	V_{BUS} rising		3.0		V
		V_{BUS} falling		2.5		V
VBUS_UVLO deglitch time	$t_{BUS\_UVLO\_DEG}$	V_{BUS} rising to recover from VBUS_UVLO		250		ms
		V_{BUS} falling to trigger VBUS_UVLO		8		ms
AC_PRESENT threshold	V_{AC_PRE}	V_{ACIN} rising		3.0		V
		V_{ACIN} falling		2.5		V
AC_PRESENT deglitch time	$t_{AC\_PRE\_DEG}$	V_{ACIN} rising to set AC_PRESENT bit		250		ms
		V_{ACIN} falling to clear AC_PRESENT bit		8		ms
Battery under-voltage lockout threshold	V_{BAT_UVLO}	V_{BAT} rising, BATUVP_SEL=0b		3.0		V
		V_{BAT} falling, BATUVP_SEL=0b		2.5		V
VBAT_UVLO deglitch time	$t_{BAT\_UVLO\_DEG}$	V_{BAT} rising to recover from VBAT_UVLO		20		ms
		V_{BAT} falling to trigger VBAT_UVLO		200		ms
VCC output voltage	V_{CC}	/EN=L, V_{BUS}=10V, I_{VCC}=0A	5.9	6.0	6.1	V
VCC output current limit	I_{VCC}	/EN=L, V_{BUS}=10V		30		mA
Quiescent current into VBUS	I_{Q_VBUS}	/EN=L, PSTOP=H, AD_START=0, VBUS=10V		115		μA
Quiescent current into VBAT	I_{Q_VBAT}	/EN=L, PSTOP=H, AD_START=0, VBAT=24V, VBUS open		35		μA
Shutdown current into VBAT	I_{SD_VBAT}	/EN=H, VBAT=24V, VBUS open		12		μA
Charge mode						
Battery voltage regulation range	V_{BAT}		2.4		24	V

Battery voltage regulation accuracy	V_{BAT_ACC}	VBAT_FB_SEL=0b, as percentage of the value set in VBAT_SET register	-0.5		0.5	%
VBATS reference voltage for external setting	V_{BATS}	VBAT_FB_SEL=1b	1.194	1.2	1.206	V
The maximum compensation voltage when battery impedance compensation is enabled	V_{COMP_MAX}			125		mV
Input voltage regulation range in charge mode	V_{INDPM}		3.0		24	V
Input voltage regulation accuracy in charge mode	V_{INDPM_ACC}	VBUS_SCALE=0b, VINDPM_H=00h, VINDPM_L=FAh,		5		V
			-2		2	%
		VBUS_SCALE=0b, VINDPM_H=01h, VINDPM_L=F4h		10		V
			-2		2	%
		VBUS_SCALE=1b, VINDPM_H=00h, VINDPM_L=FAh		10		V
			-2		2	%
		VBUS_SCALE=1b, VINDPM_H=01h, VINDPM_L=F4h		20		V
			-2		2	%
Input current limit range in charge mode	I_{IN}	R_{AC}=10mΩ	0		12750	mA
Input current limit accuracy in charge mode	I_{IN_ACC}	R_{AC}=10mΩ, IBUS_SCALE=0b, IIN_LIMIT=50h		2000		mA
			-5		5	%
		R_{AC}=10mΩ, IBUS_SCALE=0b, IIN_LIMIT=A0h		4000		mA
			-5		5	%
		R_{AC}=10mΩ, IBUS_SCALE=1b, IIN_LIMIT=50h		4000		mA
			-5		5	%
		R_{AC}=10mΩ, IBUS_SCALE=1b, IIN_LIMIT=78h		6000		mA
			-5		5	%
Battery current limit range in charge mode	I_{BAT_CHG}	R_{BAT}=10mΩ	0		12750	mA
Battery current limit accuracy in charge mode	$I_{BAT\_CHG\_ACC}$	R_{BAT}=10mΩ, IBAT_SCALE=0b IBAT_CHG=50h		2000		mA
			-5		5	%
		R_{BAT}=10mΩ, IBAT_SCALE=0b		4000		mA

		IBAT_CHG=A0h	-5		5	%
		R_{BAT}=10mΩ, IBAT_SCALE=1b IBAT_CHG=50h		4000		mA
			-5		5	%
		R_{BAT}=10mΩ, IBAT_SCALE=1b IBAT_CHG=78h		6000		mA
			-5		5	%
Trickle charge threshold	V_{TRI}	VTRICKLE_TH=0b, as percentage of the setting battery voltage		70		%
		VTRICKLE_TH=1b, as percentage of the setting battery voltage		60		%
Deglitch time to get out of trickle mode	t_{TRI_DEG}	V_{BAT} rising to exceed V_{TRI}		30		ms
Trickle mode charge current	I_{TRI}	ICHG_SEL=0b, as percentage of the value set in IIN_LIMIT register.		10		%
		ICHG_SEL=1b, as percentage of the value set in IBAT_CHG register.		10		%
Charge termination current	I_{TER}	ITERM_SET=000b		100		mA
		ITERM_SET=010b		200		mA
		ITERM_SET=110b		400		mA
Battery full charge deglitch time	t_{FULL}			5		s
Battery re-charge threshold	V_{RECHG}	As percentage of the battery voltage regulation target.		95		%
Battery re-charge deglitch time	t_{RECHG}			30		ms
The step length of charge current increase	I_{STEP_CHG}	R_{AC}=10mΩ, R_{BAT}=10mΩ, IBUS_SCALE=1b, IBAT_SACLE=1b		50		mA
The step time of charge current increase	t_{STEP_CHG}			2		ms
Deglitch time to start charging	t_{CHG_DEG}	EN_OTG=0b, V_{BUS}>V_{BUS_UVLO}, from PSTOP=L to converter starting switching.		50		ms
OTG mode						
Output voltage regulation range	V_{OTG}		2.4		24	V

Output voltage regulation accuracy	V_{OTG_ACC}	VOTG_FB_SEL=0b, VOTG_H=00h, VOTG_L=FAh		5		V
			-2		2	%
		VOTG_FB_SEL=0b, VOTG_H=02h, VOTG_L=EEh		15		V
			-2		2	%
		VOTG_FB_SEL=1b, VOTG_H=00h, VOTG_L=FAh		10		V
			-2		2	%
FB reference voltage for external setting	V_{FB}	VOTG_FB_SEL=1b, VOTG_FB_H=02h, VOTG_FB_L=58h	1.178	1.2	1.222	V
Output current limit range in discharge mode	I_{OTG}	R_{AC}=10mΩ	0		12750	mA
Battery current limit accuracy in discharge mode	$I_{BAT\_DCHG\_ACC}$	R_{BAT}=10mΩ, IBAT_SCALE=0b, IBAT_DCHG=50h		2000		mA
			-5		5	%
		R_{BAT}=10mΩ, IBAT_SCALE=0b, IBAT_DCHG=A0h		4000		mA
			-5		5	%
		R_{BAT}=10mΩ, IBAT_SCALE=1b, IBAT_DCHG=50h		4000		mA
			-5		5	%
		R_{BAT}=10mΩ, IBAT_SCALE=1b, IBAT_DCHG=78h		6000		mA
			-5		5	%
The step length of output voltage increase	V_{STEP_OTG}	VBUS_SACLE=0b		20		mV
The step time of output voltage increase[5)]	t_{STEP_OTG}			100		μs
Deglitch time to start OTG[5)]	t_{CHG_DEG}	EN_OTG=1b, V_{BUS}<V_{BUS_UVLO}, from PSTOP=L to converter starting switching.		7		ms
Protection						
Battery over-voltage threshold	V_{BATOVP}	V_{BAT} rising, as percentage of the value set in VBAT_SET register		104		%
		V_{BAT} falling, as percentage of the value set in VBAT_SET register		102		%

BATOVP deglitch time	t_{BATOVP_DEG}	V_{BAT} rising, triggered by V_{BAT} exceeding 104% of setting value		20		ms
BATOVP recovery time	t_{BATOVP_REC}	VBAT falling to recover from BATOVP		20		ms
Inductor current limit threshold, peak in boost mode, valley in buck mode[5)]	I_{L_LIMIT}	IL_LIMIT=0b, R_{AC}=R_{BAT}=10mΩ		15		A
		IL_LIMIT=1b, R_{AC}=R_{BAT}=10mΩ		21		A
OTG output over-voltage threshold	V_{OTGOVP}	VOTG_FB_SEL=0b, V_{BUS} rising, as percentage of the value set in VOTG_H and VOTG_L registers		110		%
		VOTG_FB_SEL=1b, V_{BUS} rising, as percentage of the voltage set by FB pin		110		%
OTGOVP deglitch time	t_{OTGOVP}	V_{BUS} rising, triggered by V_{BUS} exceeding the 110% of the setting value		10		ms
VBUS under-voltage threshold in OTG mode to trigger OTGOCP	$V_{BUS\_OTG\_UVP}$	EN_OTGOCP=1b, V_{BUS} falling, as percentage of the value set in VOTG register		80		%
VBUS under-voltage deglitch time in OTG mode to trigger OTGOCP	$V_{BUS\_OTG\_UVP\_DEG}$	EN_OTGOCP=1b, VBUS falling to trigger OTGOCP		7		ms
Charge time-out period	$t_{CHG\_TIME\_OUT}$	CHG_TIMER_SET=01b		12		hr
		CHG_TIMER_SET=10b		24		hr
		CHG_TIMER_SET=11b		48		hr
Watchdog time-out period	$t_{WD\_TIME\_OUT}$	WDTMR_SET=00b		10		s
		WDTMR_SET=01b		60		s
		WDTMR_SET=11b		180		s
Output current from NTC pin	I_{NTC}			30		μA
NTC over-temperature threshold in charge mode, by sensing the voltage of NTC pin	$V_{NTC\_CHG\_H}$	NTC_CHG_H=00b, temperature rising, V_{NTC} falling		0.148 (45°C)		V
		NTC_CHG_H=00b, temperature falling, V_{NTC} rising		0.176 (40°C)		V
		NTC_CHG_H=01b, temperature rising, V_{NTC} falling		0.106 (55°C)		V

		NTC_CHG_H=01b, temperature falling, V_{NTC} rising		0.126 (50°C)		V
		NTC_CHG_H=10b, temperature rising, V_{NTC} falling		0.092 (60°C)		V
		NTC_CHG_H=10b, temperature falling, V_{NTC} rising		0.106 (55°C)		V
NTC under-temperature threshold in charge mode, by sensing the voltage of NTC pin	$V_{NTC\_CHG\_L}$	NTC_CHG_L=00b, temperature falling, V_{NTC} rising		0.818 (0°C)		V
		NTC_CHG_L=00b, temperature rising, V_{NTC} falling		0.662 (5°C)		V
		NTC_CHG_L=01b, temperature falling, V_{NTC} rising		1.018 (-5°C)		V
		NTC_CHG_L=01b, temperature rising, V_{NTC} falling		0.818 (0°C)		V
		NTC_CHG_L=10b, temperature falling, V_{NTC} rising		1.274 (-10°C)		V
		NTC_CHG_L=10b, temperature rising, V_{NTC} falling		1.018 (-5°C)		V
NTC over-temperature threshold in OTG mode, by sensing the voltage of NTC pin	$V_{NTC\_OTG\_H}$	NTC_OTG_H=00b, temperature rising, V_{NTC} falling		0.106 (55°C)		V
		NTC_OTG_H=00b, temperature falling, V_{NTC} rising		0.126 (50°C)		V
		NTC_OTG_H=01b, temperature rising, V_{NTC} falling		0.092 (60°C)		V
		NTC_OTG_H=01b, temperature falling, V_{NTC} rising		0.106 (55°C)		V
		NTC_OTG_H=10b, temperature rising, V_{NTC} falling		0.078 (65°C)		V
		NTC_OTG_H=10b, temperature falling, V_{NTC} rising		0.092 (60°C)		V
NTC under-temperature threshold in OTG mode, by sensing the voltage of NTC pin	$V_{NTC\_OTG\_L}$	NTC_OTG_L=00b, temperature falling, V_{NTC} rising		1.018 (-5°C)		V
		NTC_OTG_L=00b, temperature rising, V_{NTC} falling		0.818 (0°C)		V
		NTC_OTG_L=01b, temperature falling, V_{NTC} rising		1.274 (-10°C)		V
		NTC_OTG_L=01b, temperature rising, V_{NTC} falling		1.018 (-5°C)		V
		NTC_OTG_L=10b, temperature falling, V_{NTC} rising		2.034 (-20°C)		V

		NTC_OTG_L=10b, temperature rising, V_{NTC} falling		1.602 (-15°C)		V
NTC protection deglitch time	t_{NTC_DEG}	Time to trigger NTC protection		500		ms
NTC protection recovery time	t_{NTC_REC}	Time to recover from NTC protection		500		ms
Thermal shutdown threshold[5)]	T_{SHUT}			150		°C
Thermal recovery threshold[5)]	T_{REC}			130		°C
Thermal shutdown deglitch time[5)]	t_{SHUT_DEG}			100		μs
Thermal recovery deglitch time[5)]	t_{SHUT_REC}			12		ms
Driver						
Switch frequency	F_{SW}	PWM_FREQ=000b, EN_DITHER=0b		100		kHz
		PWM_FREQ=001b, EN_DITHER=0b		200		kHz
		PWM_FREQ=010b, EN_DITHER=0b		300		kHz
		PWM_FREQ=011b, EN_DITHER=0b		350		kHz
		PWM_FREQ=100b, EN_DITHER=0b		450		kHz
		PWM_FREQ=101b, EN_DITHER=0b		500		kHz
Gate drive turn-on resistance	R_{ON}			3		Ω
Gate drive turn-off resistance	R_{OFF}			1		Ω
Interface						
/EN pin input logic low threshold	V_{EN_L}				0.4	V
/EN pin input logic high threshold	V_{EN_H}		1.2			V
PSTOP pin input logic low threshold	V_{PSTOP_L}				0.4	V
PSTOP pin input logic high threshold	V_{PSTOP_H}		1.2			V
Sink current of PGATE1, PGATE2/DITHER pin	I_{PGATE_SINK}	PGATE1_CTRL=0b, PGATE2_CTRL=0b, EN_DITHER=0b		500		μA

I2C clock frequency	F_{I2C}				400	kHz
SDA/SCL line input logic low threshold	V_{SDA/SCL_L_IN}				0.4	V
SDA/SCL line input logic high threshold	V_{SDA/SCL_H_IN}		1.2			V
SDA line output logic low threshold	V_{SDA/SCL_L_O}				0.4	V
Interrupt pulse width (logic low)	t_{INT}			0.512		ms

Notes:

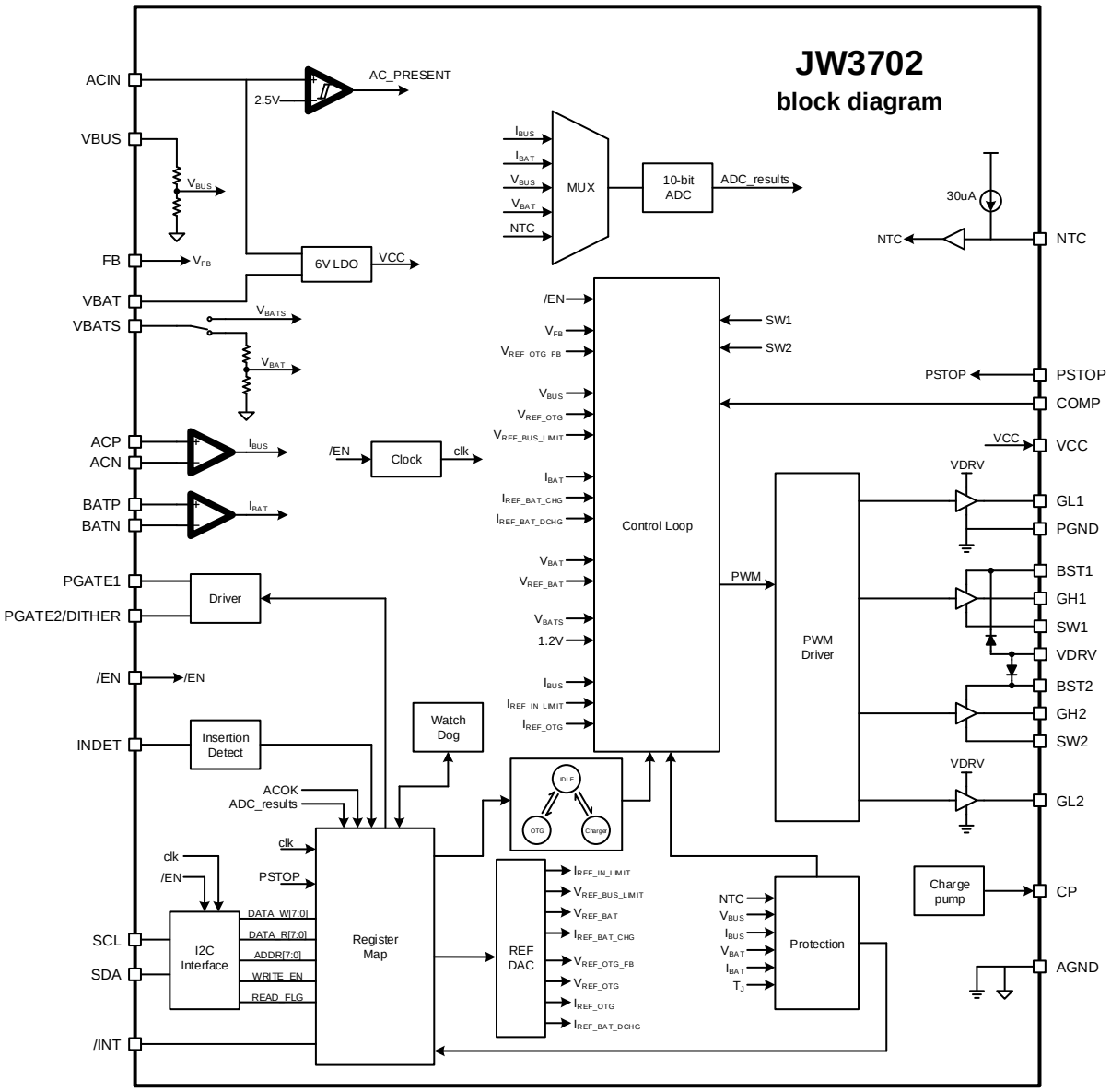
5) Guaranteed by design.

PIN DESCRIPTION

Pin No.	Name	Description
1	ACP	Input current sense resistor positive input.
2	PGATE1	PMOS gate driver 1 controlled by I2C.
3	CP	Driver for external charge pump circuit. User can use this driver to implement a charge pump between VCC and VDRV pins to generate a 6V driving voltage at VDRV pin
4	PGATE2/DITHER	PMOS gate driver 2 controlled by I2C. This pin can also be configured for frequency dithering function through I2C. Connect a ceramic capacitor from this pin to GND to set the dithering period. When this pin is configured for frequency dithering function, the PMOS gate driver function is disabled.
5	INDET	Load insertion detection pin. Connect this pin to a USB-A port to detect a load insertion event. When a load insertion event is detected, the chip sets INDET bit and outputs an /INT interrupt pulse to inform MCU.
6	ACIN	Adapter insertion detection pin. Connect this pin to a AC adapter input node or micro-USB port to detect an adapter insertion event. When an adapter insertion event is detected, the chip sets AC_PRESENT bit and outputs an /INT interrupt pulse to inform MCU.
7	/EN	Active low to enable the chip. When this pin is pulled high, the chip is disabled.
8	PSTOP	Active high to stop the power block of the chip. When this pin is pulled low the chip starts switching.
9	SCL	I2C clock input. Connect a 10kΩ pull up resistor according to I2C specification.
10	SDA	I2C data I/O. Connect a 10kΩ pull up resistor according to I2C specification.
11	/INT	Open drain output for interrupt indication. When any interrupt event is triggered, this pin sends a logic low pulse to inform the MCU.
12	AGND	Analog ground.
13	NTC	Connect a 10k 103-AT thermistor from this pin to GND for NTC protection.
14	FB	VBUS voltage feedback pin. Connect a resistor divider from VBUS to this pin to set the VBUS discharging voltage in external way.
15	COMP	Compensation pin. Connect an external compensation network between this pin and GND.
16	VBATS	Sense node for battery voltage. Connect this pin to battery if internal battery voltage setting is selected. Connect a resistor divider from VBAT to this pin if external battery voltage setting is selected.
17	BATN	Battery current sense resistor negative input.
18	BATP	Battery current sense resistor positive input.
19	VBAT	Power supply to the chip. Connect to the battery positive node.

20	BST2	Bootstrapped supplies to the high side floating drivers. Connect an 0.1μF ceramic capacitor from this pin to SW2.
21	GH2	High-side MOSFET(Q4) driver.
22	SW2	Switching node of battery side.
23	GL2	Low-side MOSFET(Q3) driver.
24	VCC	6V LDO output supplied from VBUS or VBAT for internal control circuits. Connect a 3.3μF ceramic capacitor from this pin to analog ground.
25	VDRV	Power supply for internal driver circuits. One way of getting the power supply is to connect this pin to VCC directly. Another way is to use CP driver to implement a charge pump between VCC and VDRV pin. With the charge pump, the chip can generate maximum 6V at VDRV pin for internal driver circuits.
26	PGND	Power ground.
27	GL1	Low-side MOSFET(Q2) driver.
28	SW1	Switching node of adapter side.
29	GH1	High-side MOSFET(Q1) driver.
30	BST1	Bootstrapped supplies to the high side floating drivers. Connect an 0.1μF ceramic capacitor from this pin to SW1.
31	VBUS	Power supply to the chip. Connect this pin to the VBUS rail.
32	ACN	Input current sense resistor negative input.
-	Thermal pad	PGND thermal pad. Analog ground and power ground star-connected at the thermal pad.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The JW3702 is a synchronous 4-switch I2C buck-boost controller designed for USB Type-C PD application, power bank, USB-HUB and portable devices with rechargeable battery.

The JW3702 can be powered by a wide range of input voltage varying from 3.0V to 24V, which is suitable for many power sources, such as USB Type-C PD ports, legacy USB ports, traditional AC-DC adapters, etc. It also supports USB On-The-Go (OTG) function to power up USB ports from battery, providing an output voltage range varying from 2.4V to 24V.

I2C interface is available for the chip to provide flexible system solutions, through which user can program the charging current, charging voltage, OTG voltage, OTG current limit, battery discharging current limit and other parameters easily.

Flexible Bidirectional Buck-Boost Controller

The JW3702 is a flexible bidirectional Buck-Boost controller. It utilizes proprietary single inductor current-mode control to guarantee smooth transition between buck and boost operation with better dynamic response.

External compensation makes the chip can obtain a good performance easily. The JW3702 operates in PFM mode at light load, in which switching frequency is continuously controlled in proportion to the load current, i.e. switch frequency is decreased when load current drops to increase power efficiency at light load by reducing switching-loss.

When charging, if the adapter voltage is lower than battery voltage，it is a boost controller. When the adapter voltage is higher than battery voltage, it is a buck controller, if the adapter voltage and battery voltage is very close, it is a buck-boost controller. The MOSFET operation in each mode is shown in the table below.

Mode	Q1	Q2	Q3	Q4
Buck	Switching	Switching	OFF	ON
Buck-Boost	Switching	Switching	Switching	Switching
Boost	ON	OFF	Switching	Switching

Table 1. MOSFET operation

Battery Charging

When EN_OTG bit in CTRL0 register is set to 0, and /EN, PSTOP pins are pulled to GND, the device works in charge mode. If no protection is triggered, the converter starts switching after 50ms deglitch time.

The JW3702 charges the battery in four phases: trickle charge, constant current charge, constant voltage charge and charge termination. The charge profile is shown in the figure below.

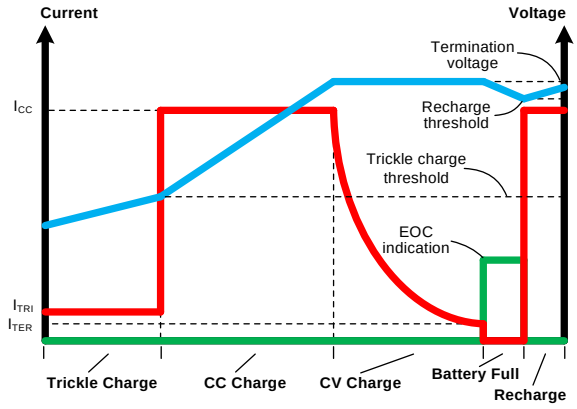


Figure 1. Charge profile

Trickle Charge

When the battery voltage is lower than 60% or 70% of the target full charge voltage (set by

VTRICLK_TH bit in CTRL1 register), the device charges the battery in trickle mode. In this phase, the charging current reduces to 1/10 of the value set in IIN_LIMIT register or IBAT_CHG register, decided by the value of ICHG_SEL bit in CTRL1 register. If ICHG_SEL is 0, the current limit at bus side is reduced to 1/10 of the value set in IIN_LIMIT register; if ICHG_SEL is 1, the current limit at battery side is reduced to 1/10 of the value set in IBAT_CHG register.

The trickle charge phase can be disabled by setting EN_TRICKLE bit in CTRL1 register to 0, if it is not needed.

Constant Current (CC) Charge

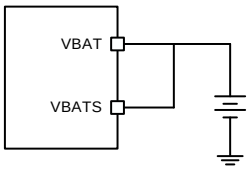
When the battery voltage is higher than the trickle charge threshold, the device charges the battery in constant current charge threshold. In this phase, the device charges the battery with the current limit set in IIN_LIMIT register and IBAT_CHG register. User can refer to the register map for detailed information.

When operating, the device always regulates the current which reaches its setting limit firstly. For example, if the current limit set in IIN_LIMIT is 2A, the current limit set in IBAT_CHG is 5A, and when input current reaches 2A, the battery current is only 3A, which is lower than its setting current limit 5A, the device will limit the input current at 2A.

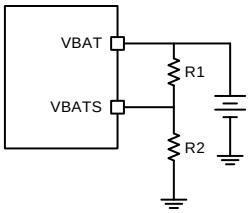
Constant Voltage (CV) Charge

When the battery voltage reaches full charge voltage, the device regulates the battery voltage and reduces the charge current automatically.

The battery voltage can be set in two methods. When the VBAT_FB_SEL bit in CTRL1 register is set to 0, the battery voltage is set internally. User can configure the cell numbers connected in series and battery voltage per cell in VBAT_SET register. When the battery voltage is set internally, the VBATS pin should be connected to the VBAT to sense the battery voltage, as shown in the figure below.



a. VBAT_FB_SEL bit = 0



b. VBAT_FB_SEL bit = 1

Figure 2. Battery voltage setting

When the VBAT_FB_SEL bit in CTRL1 register is set to 1, the battery voltage is set by external resistor divider network, as connected in figure 2. The reference of VBATS pin is fixed at 1.2V in this condition, so the setting battery voltage can be calculated by the formula below:

$$V_{BAT} = 1.2V \times (R1 + R2) / R2$$

Charge Termination

When battery voltage reaches setting voltage and the input/battery (decided by ICHG_SEL bit in CTRL1 register) current is lower than the charge termination current threshold for 5s, the charge process terminates.

The charge termination current can be set by ITERM_SET bits in CTRL1 register. And if ICHG_SEL bit = 0, the charge termination current is based on the bus current. When the charger works in CV mode and the bus current is lower than the setting threshold for 5s, charge terminates. If ICHG_SEL bit = 1, the charge

termination current is based on the battery current. When the charger works in CV mode and the battery current is lower than the setting threshold for 5s, charge terminates.

The charge termination phase can be disabled by set EN_TERM bit in CTRL1 register to 0. Then the chip will keep charging the battery to regulate the battery voltage at the setting value.

Recharge

When charge process terminates, the battery voltage may drop slowly due the leakage or operation current from the battery. Once the battery voltage drops below 95% of the setting voltage, the chip resumes switching to recharge the battery.

Battery Impedance Compensation

For high current charging application, the impedance of the battery can force the charging process to move from constant current to constant voltage too early, which may increase the charging time.

To solve the problem, the JW3702 supports battery impedance compensation function to speed up the charging cycle. During the charging process, the device allows the host to compensate the battery impedance by increasing the voltage regulation point based on actual battery current and the battery impedance. For safe operation, the allowed maximum compensation value is clamped at 125mV. The compensated battery voltage can be gotten by the equation below.

$V_{BAT\_CMP} = V_{BAT\_SET} + \min (I_{BAT} \times I_{RCOMP}, 125mV)$

Where V_{BAT_CMP} is the compensated battery voltage, V_{BAT_SET} is the setting battery voltage, I_{BAT} is the actual battery current, I_{RCOMP} is the resistance compensation value set by IRCOMP bits in VBAT_SET register.

Adaptive Input Current Limit

If the output current of the adapter is limited, it may crash when the current drawn by the charger is higher than its output current capability. The JW3702 supports adaptive input current limit function to solve problem.

The allowed minimum input voltage can be set in VINDPM_H and VINDPM_L registers. When the input voltage is pulled down to the setting threshold, due to the limited output current capability of the adapter, the chip reduces the charging current automatically to regulate the input voltage at the setting threshold and prevent the adapter from crashing.

USB On-The-GO (OTG) Function

The JW3702 supports OTG function to power up the USB ports from battery. When EN_OTG bit in CTRL0 register is set to 1, and /EN, PSTOP pins are pulled to GND, the device works in OTG mode. If no protection is triggered, the converter starts switching after $V_{BUS} < V_{BUS\_UVLO}$ for 7ms.

OTG Output Voltage Setting

When VOTG_FB_SEL bit in CTRL2 register is set to 0, the OTG output voltage is set internally. The output voltage can be set in VOTG_H and VOTG_L registers.

When VOTG_FB_SEL bit in CTRL2 register is set to 1, the OTG output voltage is set by external resistor divider network, as shown in the figure below.

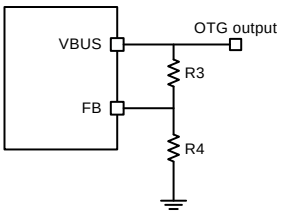


Figure 3. OTG output voltage setting (VOTG_FB_SEL bit = 1)

The output voltage can be calculated by the formula below:

$$V_{OTG} = V_{FB} \times (R3 + R4) / R4$$

Where V_{OTG} is the OTG output voltage, V_{FB} is the reference of FB pin. The reference of FB pin can be set in VOTG_FB_H and VOTG_FB_L registers and the default value is 1.2V.

OTG Current Limit Setting

When the device works in OTG mode, the output current limit and battery discharge current limit can be set in IOTG and IBAT_DCHG registers. When the output current or battery discharge current reaches the setting limit value, the device reduces the output voltage to limit the output current.

If EN_OTGOCP bit in CTRL2 register is set to 1, the device stops switching and sets the OTGOC bit in STATUS1 register, once the output voltage drops below $V_{BUS\_OTG\_UVP}$ threshold due to output or battery discharge current limit. This function can be disabled by setting EN_OTGOCP to 0, if so, the device can keep switching with limited current set in IOTG and IBAT_DCHG registers, even if the output voltage drops below the $V_{BUS\_OTG\_UVP}$ threshold. But the OTGOC bit will still be set to inform the host.

Soft Start

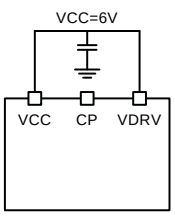
The JW3702 features soft start function to avoid any current or voltage inrush during the start process.

When the device works in charge mode, it will increase input and battery charging current limit from 0 to the setting value with rate of 1LSB/2ms, during the start process. The LSB is the minimum step of the current set in IIN_LIMIT and IBAT_CHG registers, which can be set in SCALE register. And when the charging phase changes from trickle mode to CC mode or user increases the charging current by I2C command, the charging current also increases from the current value to the target value with the rate of 1LSB/2ms.

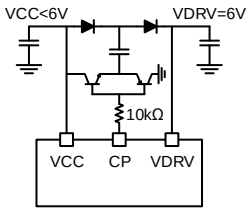
When the device works in OTG mode, a soft start will also be implemented during the start process. If VOTG_FB_SEL bit in CTRL2 register is set to 0, the device will increase the output voltage from 0 to the setting value with the rate of 1LSB/100us. The LSB is the minimum step of the OTG voltage set in VOTG_H and VOTG_L registers, which can be set in SCALE register. If VOTG_FB_SEL bit in CTRL2 register is set to 1, the device will increase the reference of FB pin from 0 to the setting value with the rate of 2mV/100us. Also, when user increases the output voltage by I2C command, the device also increases the voltage from current value to the target value step by step with the rate described above.

A soft process will also be implemented, when the chip resume switching from protection.

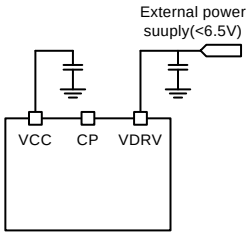
Driver Supply



a. Connect VCC to VDRV directly



b. Use charge pump to power VDRV



c. Use external power supply

Figure 4. Supply for VDRV pin

The driver circuit of JW3702 is powered by VDRV pin. In most applications, this pin can be connected to VCC pin directly to get 6V driver voltage, as shown in Figure 4-a.

However, for single cell applications, the voltage of VCC pin may be lower than 6V, if VDRV pin is connected to VCC directly, the driver voltage of the MOSDETs will be lower than 6V, which may decrease the system efficiency due to higher R_{DS_ON} of the MOSFETs. To provide 6V driver voltage in this application, the JW3702 offers a charge pump circuit at CP pin. As connected in Figure 4-b, with the integrated charge pump circuit, the JW3702 can still generate a 6V driver voltage at the VDRV pin to drive the external MOSFETs.

Also, user can connect the VDRV pin to an external power supply (<6.5V) as shown in Figure 4-c, to power the driver circuit.

Power Path Management

The JW3702 offers power path management function at PGATE1 and PGATE2 pins. As connected in the figure below, the two pins can be used to drive the load switches between adapter input and USB output.

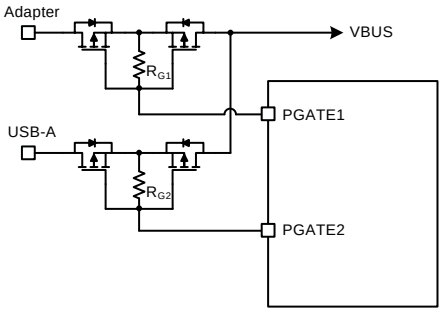


Figure 5. PGATE1/PGATE2 connection

Both pins are open drain outputs, and their behavior is controlled by PGATE1_CTRL and PGATE2_CTRL bits in CTRL3 register. When PGATE1_CTRL(PGATE2_CTRL) bit is set to 1, the PGATE1(PGATE2) pin outputs high impedance to turn off the load switch. When PGATE1_CTRL (PGATE2_CTRL) bit is set to 0, the PGATE1(PGATE2) pin is pulled low with maximum 500μA sink current to turn on the load switch. If the gate resistor of the load switch is R_{G1}/R_{G2} as shown in Figure 5, the maximum V_{GS} voltage can be expressed as,

$$V_{GS.max} = R_{Gx} \times 500\mu A$$

Where $V_{GS.max}$ is the maximum V_{GS} voltage, R_{Gx} represents R_{G1}/R_{G2}.

Frequency Dithering

The JW3702 offers frequency dithering function, which can be enabled by EN_DITHER bit in CTRL0 register. When the function is enabled, the frequency of the converter will vary within ±5% range of the setting value in CTRL0 register. For example, if the switching frequency of the converter is set to 500kHz, the actual frequency will change from 475kHz to 525kHz gradually, and then back to 475kHz, back and forth. The time it varies from the lowest

frequency to the highest frequency is determined by the capacitor connected from PGATE2/DITHER pin to GND, as shown in the figure below.

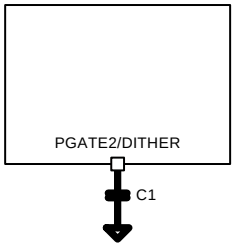


Figure 6. Frequency dithering connection

The time can be calculated as,

$$T_{DITHER}\,(\mu s) = 105 \times C1(nF)$$

For example, if the frequency dithering capacitor C1 is set to 10nF, the dithering time is 1050μs.

When the frequency dithering function is activated, the PMOS gate driver at PGATE2 pin is disabled.

Phone Insert Indication

When INDET pin is connected to the USB-A port as shown in the typical application circuit, the chip can detect the phone insert event. When a phone is inserted, the chip sets INDET bit in STATUS0 register. And if the interrupt of INDET is enabled, an interrupt pulse at /INT pin will be generated to inform the host.

Adapter Attachment / Detachment Indication

When ACIN pin is connected to the adapter input port as shown in the typical application circuit, the JW3702 can detect the adapter attachment/detachment.

When the voltage of ACIN pin rises above V_{AC_PRE} rising threshold, the AC_PRESENT bit in STATUS register is set to 1; when the voltage of ACIN pin falls below V_{AC_PRE} falling threshold, the AC_PRESENT bit is cleared.

ADC for System Monitor

The JW3702 integrates a 10-bit high precision ADC to monitor the system status, including bus voltage, bus current, battery voltage, battery current and NTC resistor voltage. Each channel can be enabled or disabled in ADC_SET register independently. When ADC_START bit in ADC_SET register is set to 1, the ADC module starts to sample each channel continuously.

The LSB of the bus voltage, bus current, battery voltage and battery current can be set by the corresponding bits in SCALE register. However, for NTC resistor voltage channel, the LSB is fixed at 2mV, and the full range is 2.046V. User can refer to the register map for detailed information.

Bus Discharge

To discharge the residual voltage in the bus, the chip offers bus discharge function to discharge the bus for 100ms with 50mA current.

The discharging is activated when the following conditions are valid:

- Chip enters into IDLE mode
- Decrease OTG voltage by I2C
- The voltage of FB pin is higher than its setting reference by 3% in OTG mode, when VOTG_FB_SEL=1b
- OTGOVP is triggered

Also, user can discharge the bus at any time by writing 1 to BUS_DCHG bit in CTRL3 register.

IDLE Mode

When PSTOP pin pulled high and /EN is pulled

low, the chip enters into IDLE mode. In this mode, the chip stops switching, and all modules except I2C, phone insert indication, adapter insert indication, bus discharge, are disabled for lower current consumption.

ADC module can still be enabled if ADC_START bit is set to 1, if so, the chip will consume extra quiescent current in IDLE mode.

Shutdown Mode

When /EN pin is pulled high, the chip enters into shutdown mode, in which the device stops switching and disables all the modules for minimum quiescent current. In this mode, all the registers are reset to the default value.

Protection

The JW3702 guarantees robustness with comprehensive protection, including battery/ OTG over-voltage protection, bus/ battery under-voltage protection, OTG / battery over-current protection, charging timeout, watchdog and thermal shutdown.

All the protections triggered in charge mode can be resumed automatically, when the protection conditions are removed. However, all the protections triggered in OTG mode are latched, and can be resumed by writing 1 to the corresponding status bits, when the protection conditions are removed.

Bus Under-Voltage Protection (BUSUVP)

The bus under-voltage protection is only available in charge mode (EN_OTG bit = 0b, PSTOP = Low).

If the bus voltage falls below the V_{BUS_UVLO} falling threshold, the chip stops switching and sets VBUSUVP_CHG bit in STATUS0 register to 1. If the bus voltage rises above the V_{BUS_UVLO} rising threshold, the chip resumes switching and clears VBUSUVP_CHG bit automatically.

When the chip gets out of charge mode, the BUSUVP_CHG bit will be cleared automatically.

Battery Over-Voltage Protection (BATOVP)

In charge mode, if the battery voltage rises above 104% of the setting value, the chip stops switching and sets BATOVP bit in STATUS0 register to 1. If the battery voltage falls below 102% of the setting value, the protection is removed and BATOVP is cleared automatically.

When the chip enters into IDLE mode, the protection is removed automatically and the BATOVP bit is cleared as well.

OTG Over-Voltage Protection (OTGOVP)

When the OTG output voltage exceeds 110% of the setting value, the chip stops switching and sets OTGOVP bit in STATUS1 register to 1. Once the OTGOVP is triggered, the protection is latched. The protection can be removed by writing 1 to OTGOVP bit.

When the chip gets out of OTG mode, the protection is removed automatically and OTGOVP bit is cleared as well.

OTG Over-Current Protection (OTGOCP)

When OTG output voltage drops below 80% of the setting value due to current limit, the OTGOC bit in STATUS1 register will be set to 1.

If EN_OTGOCP bit in CTRL2 register is set to 1, the chip stops switching, and the protection is latched. The OTGOC bit can be cleared by a writing 1 command. Once the OTGOC bit is cleared, the chip resumes switching.

If EN_OTGOCP bit in CTRL2 register is set to 0, the chip will keep switching with limited current set in IOTG and IBAT_DCHG registers. And

when the OTG voltage rises above the 80% of the setting value, the OTGOC bit is cleared automatically.

When the chip exits OTG mode, the OTGOCP protection is removed automatically and OTGOC bit is cleared as well.

Battery Empty Protection (BAT_EMPTY)

The battery empty protection threshold can be set by BATUVP_SEL bit in CTRL2 register. If BATUVP_SEL bit=0, the threshold is fixed at 2.5V (falling)/ 3.0V (rising). If BATUVP_SEL bit=1, the threshold is 2.5V (falling)/ 3.0V (rising) per cell.

The battery empty protection is only available in OTG mode. When the battery falls below the setting threshold, the chip stops switching and sets BAT_EMPTY bit in STATUS1 register to 1. Once BAT_EMPTY is triggered, the protection is latched. When the battery voltage rises above the setting threshold, the protection can be removed by writing 1 to BAT_EMPTY bit.

When the chip gets out of OTG mode, the protection is removed automatically and BAT_EMPTY bit is cleared as well.

NTC Protection (NTC_FAULT)

The NTC protection of JW3702 is realized by its integrated ADC, so if NTC protection is needed, the AD_START and EN_ADC_NTC bits in ADC_SET register must be set to 1.

A 10kΩ 103-AT thermistor is needed to be connected between NTC pin and GND for NTC protection. The thresholds of NTC protection can be set in NTC_SET register.

When the NTC resistor voltage is outside of the setting temperature thresholds, the chip stops switching and sets NTC_FAULT bit in STATUS1 register to 1. If the chip is in charge mode, it can resume switching and clear the NTC_FAULT bit, when the NTC voltage is within the thresholds again. However, if the chip is in OTG mode, the protection is latched. When the NTC voltage is within the thresholds, it will not resume switching automatically, until a writing 1 command to NTC_FAULT bit.

When the chip enters into IDLE mode, the protection is removed automatically, and NTC_FAULT bit is cleared as well.

Charging Timeout (CHG_TIMEOUT)

When working in charge mode, the JW3702 uses an internal timer to terminate the charging process, once the time it stays in charge mode exceeds the value set by CHG_TIMER_SET bits in CTRL3 register.

Once the chip enters into charge mode, the timer starts working. When the timer is expired, the chip stops switching and sets CHG_TIMEOUT bit in STATUS1 register to 1.

When the charge timer is expired, it can be reset by writing 1 to CHG_TIMER_RESET bit in CTRL3 register. Once the charge timer is reset, the CHG_TIMEOUT bit is cleared automatically and the chip resumes switching.

When the chip exits charge mode, the timer stops and is reset automatically, and the CHG_TIMEOUT bit is cleared as well.

Watchdog Timer (WD_TIMEOUT)

The JW3702 offers a watchdog timer to ensure the reliability of I2C communication. To reset the watchdog timer, the host has to write 1 to WD_RESET bit in CTRL2 register periodically. The maximum delay between consecutive I2C write to WD_RESET bit can be set by WDTMR_SET bit in CTRL2 register.

Once the watchdog timer is expired, the chip

stops switching and sets WD_TIMEOUT bit in STATUS1 register to 1. The protection can be removed by a writing 1 command to WD_RESET bit.

The watchdog timer only works in charge or OTG mode. When the chip enters into IDLE mode, the timer stops and is reset. However, the WD_TIMEOUT bit in STATUS1 register will not be cleared automatically, if it is set to 1 in charge or OTG mode.

Thermal Shutdown (TSHUT)

When the junction temperature of the JW3702 rises above 150°C, the device enters into thermal shutdown mode, in which it stops switching and sets TSHUT bit in STATUS1 register to 1. If the device is in charge mode, it can resume switching, when the junction temperature drops below 130°C. If the device is in OTG mode, the TSHUT protection is latched. When the temperature drops below 130°C, it will not resume switching automatically, until a writing 1 command to the TSHUT bit.

When the chip enters into IDLE mode, the protection is removed automatically, and TSHUT bit is cleared as well.

I2C Interface

The JW3702 integrates an I2C interface to provide flexible solutions for different applications. The JW3702 always works as a salve module with a 7-bit address 74h (1110_100xb). The integrated I2C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

To ensure the reliability of the communication, after the chip is powered up or /EN pin is toggled from high to low, the host must wait for at least 1ms before sending any I2C command.

Start and Stop Conditions

A HIGH to LOW transition on SDA line while SCL is HIGN defines a START condition, and a LOW to HIGH transition on SDA line while SCL is HIGH defines a STOP condition.

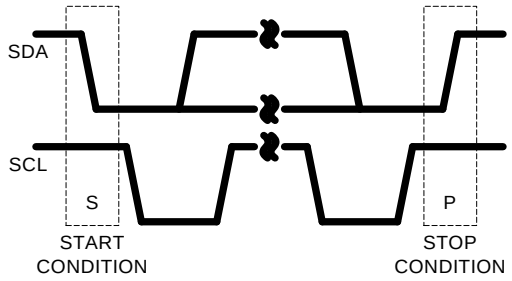


Figure 7. START and STOP conditions

The START and STOP conditions can only be sent by the master.

Data Validity

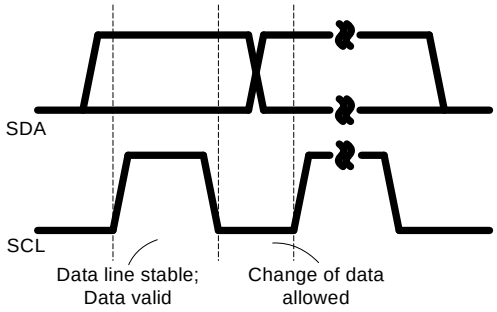


Figure 8. Data validity

The data on SDA line must be stable during the HIGH period of the SCL, unless a START or STOP condition generated. The HIGH or LOW state of SDA line can only change when the clock signal on SCL line is LOW.

Byte Format

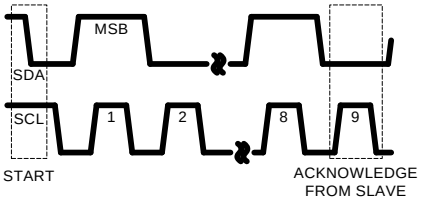


Figure 9. Data transfer on the I2C bus

Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after each byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte can be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a salve address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

Single Read and Write

The device supports single read and write.

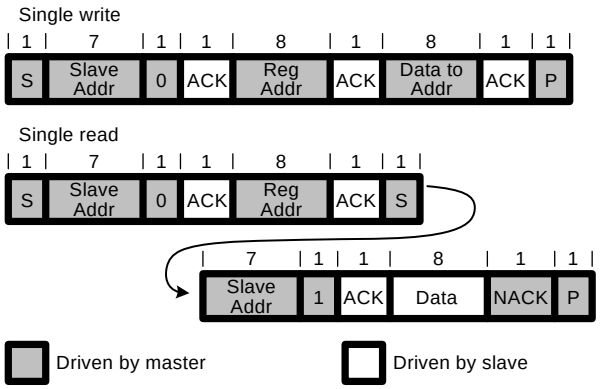


Figure 10. Single read and single write

Multi-Read and Multi-Write

The device supports multi-read and multi-write.

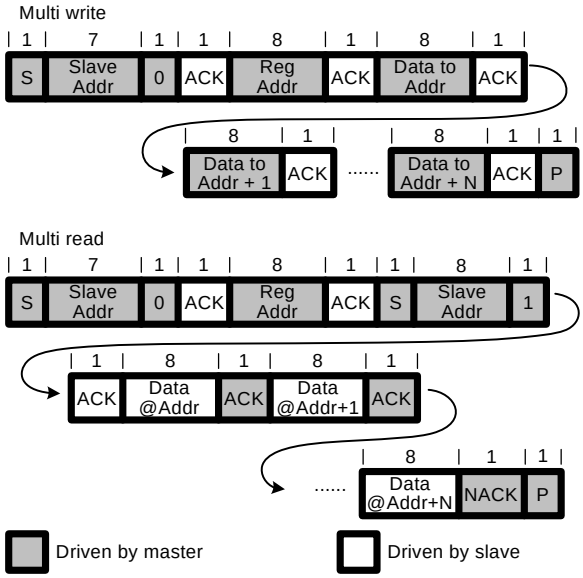


Figure 11. Multi read and multi write

Write/Read 2-Byte I2C Commands

A few parameters of the JW3702 combine two 8-bit registers together to form a complete value. For these registers, the read/write should follow a specific sequence. These register includes a few configuration registers and all the ADC result registers.

For the configuration register listed below,

- VINDPM_H and VINDPM_L
- VOTG_H and VOTG_H
- VOTG_FB_H and VOTG_FB_L

The LSB register must be written after the MSB register. After the LSB register is written, the MSB and LSB registers will be updated at the same time. For example, the VINDPM_L register must be written after the VINDPM_H register. And the two registers will be updated at the same time, after VINDPM_L register is written.

And for ADC result registers listed below,

- ADC_VBUS_L and ADC_VBUS_H
- ADC_IBUS_L and ADC_IBUS_H
- ADC_VBAT_L and ADC_VBAT_H
- ADC_IBAT_L and ADC_IBAT_H
- ADC_NTC_L and ADC_NTC_H

The MSB register will be buffered automatically after the corresponding LSB register is read. When the host reads the MSB register then, the device will return the buffered value. So, to get the correct ADC results, the host must read the MSB register after the LSB register.

For these registers, a multi-read or multi-write command is recommended to be used.

Write Restriction

A few bits in some registers can only be written in IDLE mode (PSTOP=High, /EN=Low). These bits include:

- EN_OTG, PWM_FREQ bits in CTRL0 register
- VBAT_FB_SEL bit in CTRL1 register
- VOTG_FB_SEL in CTRL2 register
- RESET_REG bit in CTRL3 register

Any write command to these bits in charge/OTG mode will be ignored automatically, and the bits keep unchanged.

Interrupt

When any bit in STATUS0 and STATUS1 registers changes from 0 to 1, the chip sends an active low, 0.512ms pulse at /INT pin to inform the host, as shown in the figure below.

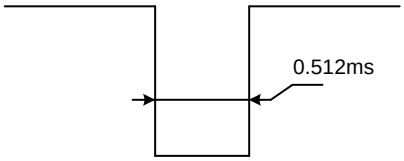


Figure 12. Interrupt pulse at /INT pin

User can disable the interrupt output of any bit by setting its corresponding bit in INT_EN0 / INT_EN1 register to 0. When the enable bit is cleared, the corresponding status bit is still set, but the chip does not send an interrupt pulse at /INT pin.

Register Map

I2C ADDR	REGISTER NAME	TYPE	DESCRIPTION
0x00	VBAT_SET	R/W	Battery parameters configuration
0x01	VINDPM_H	R/W	10-bit VINDPM voltage setting
0x02	VINDPM_L	R/W	
0x03	IIN_LIMIT	R/W	8-bit input current limit setting
0x04	IBAT_CHG	R/W	8-bit battery charge current setting
0x05	VOTG_H	R/W	10-bit OTG output voltage setting
0x06	VOTG_L	R/W	
0x07	VOTG_FB_H	R/W	10-bit FB reference voltage setting
0x08	VOTG_FB_L	R/W	
0x09	IOTG	R/W	8-bit OTG output current limit setting
0x0A	IBAT_DCHG	R/W	8-bit battery discharge current limit setting
0x0B	CTRL0	R/W	Control register 0
0x0C	CTRL1	R/W	Control register 1
0x0D	CTRL2	R/W	Control register 2
0x0E	CTRL3	R/W	Control register 3
0x0F	NTC_SET	R/W	NTC threshold setting
0x10	ADC_SET	R/W	ADC setting
0x11	SCALE	R/W	Scale setting
0x12	ADC_VBUS_L	R	10-bit ADC value of bus voltage
0x13	ADC_VBUS_H	R	
0x14	ADC_IBUS_L	R	10-bit ADC value of bus current
0x15	ADC_IBUS_H	R	
0x16	ADC_VBAT_L	R	10-bit ADC value of battery voltage
0x17	ADC_VBAT_H	R	
0x18	ADC_IBAT_L	R	10-bit ADC value of battery current
0x19	ADC_IBAT_H	R	
0x1A	ADC_NTC_L	R	10-bit ADC value of NTC pin voltage
0x1B	ADC_NTC_H	R	
0x1C	STATUS0	R	System status register 0
0x1D	STATUS1	R	System status register 1
0x1E	INT_EN0	R/W	Interrupt enable register 0
0x1F	INT_EN1	R/W	Interrupt enable register 1
0xFE	ID	R	Device ID register

VBAT_SET Register (I2C Address = 0x00) [reset = 01h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-6	IRCOMP	R/W	00b	Battery impedance compensation set. 00b: 0mΩ (default at POR) 01b: 20mΩ 10b: 40mΩ 11b: 80mΩ
5-3	CSEL	R/W	000b	Battery cell selection. 000b: 1S battery (default at POR) 001b: 2S battery 010b: 3S battery 011b: 4S battery 100b-111b:reserved
2-0	VCELL	R/W	001b	Battery voltage setting for each cell. 000b: 4.1V 001b: 4.2V (default at POR) 010b: 4.25V 011b: 4.3V 100b: 4.35V 101b: 4.4V 110b: 4.45V 111b: 4.5V

VINDPM_H Register (I2C Address = 0x01) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	VINDPM_H	R/W	00b	The highest 2-bit of input voltage limit setting. The input voltage limit can be calculated by the formula below: If VBUS_SCALE=0b, V_{INDPM} = (VINDPM_L + VINDPM_H × 256) × 20mV, If VBUS_SCALE=1b, V_{INDPM} = (VINDPM_L + VINDPM_H × 256) × 40mV, The default value of V_{INDPM} is 4.5V (VINDPM_H=00h, VINDPM_L=E1h, VBUS_SCALE=0b). The VINDPM_H and VINDPM_L registers are updated at the same time after VINDPM_L register is written.

VINDPM_L Register (I2C Address = 0x02) [reset = E1h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	VINDPM_L	R/W	11100001b	The lowest 8-bit of input voltage limit setting. The input voltage limit can be calculated by the formula below: If VBUS_SCALE=0b, V_{INDPM} = (VINDPM_L + VINDPM_H × 256) × 20mV, If VBUS_SCALE=1b, V_{INDPM} = (VINDPM_L + VINDPM_H × 256) × 40mV, The default value of V_{INDPM} is 4.5V (VINDPM_H=00h, VINDPM_L=E1h, VBUS_SCALE=0b). The VINDPM_H and VINDPM_L registers are updated at the same time after VINDPM_L register is written.

IIN_LIMIT Register (I2C Address = 0x03) [reset = 3Ch]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	IIN_LIMIT	R/W	00111100b	8-bit input current limit setting. When using a 10mΩ current sense resistor, the input current limit can be calculated by the formula below: If IBUS_SCALE = 0b, I_{IN_LIMIT} = IIN_LIMIT × 25mA If IBUS_SCALE = 1b, I_{IN_LIMIT} = IIN_LIMIT × 50mA In charge mode, if IIN_LIMIT=00h, the chip stops switching. The default value is 3A (IBUS_SCALE = 1b).

IBAT_CHG Register (I2C Address = 0x04) [reset = 3Ch]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	IBAT_CHG	R/W	00111100b	8-bit charge current setting at battery side. When using a 10mΩ current sense resistor, the charge current can be calculated by the formula below: If IBAT_SCALE = 0b, I_{BAT_CHG} = IBAT_CHG × 25mA If IBAT_SCALE = 1b, I_{BAT_CHG} = IBAT_CHG × 50mA In charge mode, if IBAT_CHG=00h, the chip stops switching. The default value is 3A (IBAT_SCALE = 1b).

VOTG_H Register (I2C Address = 0x05) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	VOTG_H	R/W	00b	The highest 2-bit of OTG voltage setting. The OTG voltage can be calculated by the formula below: If VBUS_SCALE=0b, V_{OTG} = (VOTG_L + VOTG_H × 256) × 20mV, If VBUS_SCALE=1b, V_{OTG} = (VOTG_L + VOTG_H × 256) × 40mV, The default value of the OTG voltage is 5V (VOTG_H=00h, VOTG_L=FAh, VBUS_SCALE=0b). The maximum value of the OTG voltage is 24V. The VOTG_H and VOTG_L registers are updated at the same time after VOTG_L register is written.

VOTG_L Register (I2C Address = 0x06) [reset = FAh]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	VOTG_L	R/W	11111010b	The lowest 8-bit of OTG voltage setting. The OTG voltage can be calculated by the formula below: If VBUS_SCALE=0b, V_{OTG} = (VOTG_L + VOTG_H × 256) × 20mV, If VBUS_SCALE=1b, V_{OTG} = (VOTG_L + VOTG_H × 256) × 40mV, The default value of the OTG voltage is 5V (VOTG_H=00h, VOTG_L=FAh, VBUS_SCALE=0b). The VOTG_H and VOTG_L registers are updated at the same time after VOTG_L register is written.

VOTG_FB_H Register (I2C Address = 0x07) [reset = 02h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	VOTG_FB_H	R/W	10b	The highest 2-bit of the reference on FB pin for external OTG voltage programming: When VOTG_FB_SEL=1b, the OTG voltage is programmed by FB pin. The reference on this pin can be calculated as: V_{OTG_FB} = (VOTG_FB_L + VOTG_FB_H × 256) × 2mV The default value of FB reference is 1.2V. The VOTG_FB_H and VOTG_FB_L registers are updated at the same time after VOTG_FB_L register is written.

VOTG_FB_L Register (I2C Address = 0x08) [reset = 58h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	VOTG_FB_L	R/W	01011000b	The lowest 8-bit of the reference on FB pin for external OTG voltage programming: When VOTG_FB_SEL=1b, the OTG voltage is programmed by FB pin. The reference on this pin can be calculated as: V_{OTG_FB} = (VOTG_FB_L + VOTG_FB_H × 256) × 2mV The default value of FB reference is 1.2V. The VOTG_FB_H and VOTG_FB_L registers are updated at the same time after VOTG_FB_L register is written.

IOTG Register (I2C Address = 0x09) [reset = 3Ch]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	IOTG	R/W	00111100b	8-bit OTG output current limit setting. When using a 10mΩ current sense resistor, the output current limit can be calculated as: If IBUS_SCALE = 0b, I_{OTG_LIMIT} = IOTG × 25mA If IBUS_SCALE = 1b, I_{OTG_LIMIT} = IOTG × 50mA In OTG mode, if IOTG=00h, the chip stops switching. The default value is 3A (IBUS_SCALE=1b).

IBAT_DCHG Register (I2C Address = 0x0A) [reset = 3Ch]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	IBAT_DCHG	R/W	00111100b	8-bit battery discharge current limit setting. When using a 10mΩ current sense resistor, the current limit can be calculated as: If IBAT_SCALE = 0b, I_{BAT_DCHG} = IBAT_DCHG × 25mA If IBAT_SCALE = 1b, I_{BAT_DCHG} = IBAT_DCHG × 50mA In OTG mode, if IBAT_DCHG=00h, the chip stops switching. The default value is 3A (IBAT_SCALE=1b).

CTRL0 Register (I2C Address = 0x0B) [reset = 20h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	EN_OTG	R/W	0b	Enable OTG function. 0b: Disable OTG. The chip works in charge mode. (default at POR) 1b: Enable OTG. The chip works in OTG mode. This bit can only be modified in IDLE mode. Any write to this bit in charge/OTG mode will be ignored automatically.
6-4	PWM_FREQ	R/W	010b	Switching frequency setting. 000b: 100kHz 001b: 200kHz 010b: 300kHz (default at POR) 011b:350kHz 100b: 450kHz 101b: 500kHz 110b~111b: reserved The PWM_FREQ bits can only be modified in IDLE mode. Any write to PWM_FREQ bits in charge/OTG mode will be ignored automatically.
3	EN_FCCM	R/W	0b	Force CCM mode control. 0b: Disable FCCM. The chip works in PFM mode under light load condition. (default at POR) 1b: Enable FCCM. The chip works in force CCM mode under light load condition.
2	Reserved	R/W	0b	Reserved.

1	EN_DITHER	R/W	0b	Frequency dithering function enable. 0b: Disable frequency dithering function. The PGATE2/DITHER pin is used as PMOS gate control. (default at POR) 1b: Enable frequency dithering function. The PGATE2/DITHER pin is used to set frequency dithering.
0	Reserved	R/W	0b	Reserved. Don't overwrite this bit.

CTRL1 Register (I2C Address = 0x0C) [reset = 19h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	VBAT_FB_SEL	R/W	0b	Battery voltage setting control. 0b: Internal setting. The battery voltage is set by VBAT_SET register. (default at POR) 1b: External setting. The battery voltage is set by external resistor divider network. This bit can only be modified in IDLE mode. Any write to this bit in charge/OTG mode will be ignored automatically.
6	ICHG_SEL	R/W	0b	Charging current selection. 0b: Select bus current as charging current. The trickle current and termination current is based on bus current. (default at POR) 1b: Select battery current as charging current. The trickle current and termination current is based on battery current.
5	VTRICKLE_TH	R/W	0b	Trickle charge threshold setting. 0b: Set the trickle charge threshold as 70% of setting battery voltage. (default at POR) 1b: Set the trickle charge threshold as 60% of setting battery voltage.
4	EN_TRICKLE	R/W	1b	Trickle charge phase control. 0b: Disable trickle charge phase. 1b: Enable trickle charge phase. (default at POR)

3-1	ITERM_SET	R/W	100b	Charge termination current threshold setting. When ICHG_SEL=0b, the termination current is based on bus current; when ICHG_SEL=1b, the termination current is based on battery current The current threshold is based on 10mΩ current sense resistor. 000b: 100mA 001b: 150mA 010b: 200mA 011b: 250mA 100b: 300mA (default at POR) 101b: 350mA 110b: 400mA 111b: 450mA
0	EN_TERM	R/W	1b	Charge auto-termination control. 0b: Disable auto-termination. When the battery voltage reaches the setting value, and the charge current drops below the setting threshold for 5s, the charge process will not terminate automatically. The charger keeps switching to regulate the battery voltage at the setting value. (default at POR) 1b: Enable auto-termination. When the battery voltage reaches the setting value, and the charge current drops below the setting threshold for 5s, the charge process terminates automatically.

CTRL2 Register (I2C Address = 0x0D) [reset = 60h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	VOTG_FB_SEL	R/W	0b	OTG output voltage setting control. 0b: Internal OTG voltage setting. The OTG voltage is set by VOTG_H and VOTG_L registers. (default at POR) 1b: External OTG voltage setting. The OTG voltage is set by resistor divider network at FB pin. This bit can only be modified in IDLE mode. Any write to this bit in charge/OTG mode will be ignored automatically.
6-5	WDTMR_SET	R/W	11b	Watchdog timer setting. Set maximum delay between consecutive I2C write to WD_RESET bit. If device does not receive a write 1 command to the WD_RESET bit within the watchdog time period, the device stops switching. 00b: 10s 01b: 60s 10b: 180s 11b: Disabled (default at POR)
4	WD_RESET	R/W	0b	Watchdog reset. Write 1 to this bit to reset the watchdog timer. When watchdog is expired, the protection can also be removed by a writing 1 command to this bit. 0b: Ignored (default at POR) 1b: Reset the watchdog timer
3	EN_OTGOCP	R/W	0b	Enable OTG over-current protection. 0b: Disable OTG over-current protection. (default at POR) 1b: Enable OTG over-current protection.
2	BATUVP_SEL	R/W	0b	Battery under-voltage threshold selection. 0b: The battery under-voltage threshold is set as a fixed value, rising: 3.0V, falling: 2.5V. (default at POR) 1b: The battery under-voltage threshold is decided by the number of battery cells, rising: 3.0V/cell, falling: 2.5V/cell.
1	IL_LIMIT	R/W	0b	Inductor current limit setting. Peak in boost mode, valley in buck mode, 10mΩ current sense resistor. 0b: 15A (default at POR) 1b: 21A
0	Reserved	R/W	0b	Reserved. Don't overwrite this bit.

CTRL3 Register (I2C Address = 0x0E) [reset = 31h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-6	CHG_TIMER_SET	R/W	00b	Charging timeout threshold setting. 00b: Disabled (default at POR) 01b: 12hr 10b: 24hr 11b: 48hr
5	PGATE1_CTRL	R/W	1b	PGATE1 pin control. 0b: Logic low output to turn on the load switch on power path. The maximum sink current at PGATE1 pin is 500μA. 1b: Open drain output to turn off the load switch on power path. (default at POR)
4	PGATE2_CTRL	R/W	1b	PGATE2 pin control. 0b: Logic low output to turn on the load switch on power path. The maximum sink current at PGATE2 pin is 500μA. 1b: Open drain output to turn off the load switch on power path. (default at POR)
3	BUS_DCHG	R/W	0b	Write 1 to this bit to discharge bus for 100ms with 50mA current. 0b: Ignored. (default at POR) 1b: Discharge the bus for 100ms with 50mA current.
2	RESET_REG	R/W	0b	Reset registers. Write 1 to this bit to reset all the register to the default value. 0b: Ignored. (default at POR) 1b: Reset all the registers to the default value. The bit can only be written in IDLE mode. Any write to this bit in charge/OTG mode will be ignored automatically.
1	CHG_TIMER _RESET	R/W	0b	Charge timer reset. Write 1 to this bit to reset the charge timer. When charging timeout is triggered, the protection can be removed by a writing 1 command to this bit. 0b: Ignored. (default at POR) 1b: Reset the charge timer.
0	Reserved	R/W	1b	Reserved. Don't overwrite this bit.

NTC_SET Register (I2C Address = 0x0F) [reset = 55h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-6	NTC_CHG_H	R/W	01b	NTC high threshold in charge mode 00b: 45°C 01b: 55°C (default at POR) 10b: 60°C 11b: Disabled
5-4	NTC_CHG_L	R/W	01b	NTC low threshold in charge mode 00b: 0°C 01b: -5°C (default at POR) 10b: -10°C 11b: Disabled
3-2	NTC_OTG_H	R/W	01b	NTC high threshold in OTG mode 00b: 55°C 01b: 60°C (default at POR) 10b: 65°C 11b: Disabled
1-0	NTC_OTG_L	R/W	01b	NTC low threshold in OTG mode 00b: -5°C 01b: -10°C (default at POR) 10b: -20°C 11b: Disabled

ADC_SET Register (I2C Address = 0x10) [reset = 7Ch]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	AD_START	R/W	0b	Start ADC conversion. If NTC protection is needed. This bit must be set to 1, when PSTOP is pulled logic low. 0b: Stop ADC conversion. (default at POR) 1b: Start ADC conversion.
6	EN_ADC_VBUS	R/W	1b	0b: Disable VBUS ADC. 1b: Enable VBUS ADC. (default at POR)
5	EN_ADC_IBUS	R/W	1b	0b: Disable IBUS ADC. 1b: Enable IBUS ADC. (default at POR)
4	EN_ADC_VBAT	R/W	1b	0b: Disable VBAT ADC. 1b: Enable VBAT ADC. (default at POR)

3	EN_ADC_IBAT	R/W	1b	0b: Disable IBAT ADC. 1b: Enable IBAT ADC. (default at POR)
2	EN_ADC_NTC	R/W	1b	If NTC protection is needed. This bit must be set to 1, when PSTOP is pulled logic low. 0b: Disable NTC ADC. 1b: Enable NTC ADC. (default at POR)
1-0	Reserved	R/W	00b	Reserved. Don't overwrite these bits.

SCALE Register (I2C Address = 0x11) [reset = 50h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	VBUS_SCALE	R/W	0b	Bus voltage scale setting. This bit influences the results of VINDPM setting, VOTG setting and VBUS ADC sampling. User can refer to the corresponding registers for detailed information. 0: Choose smaller LSB for VINDPM setting, VOTG setting and VBUS ADC sampling. (default at POR) 1: Choose larger LSB for VINDPM setting, VOTG setting and VBUS ADC sampling.
6	IBUS_SCALE	R/W	1b	Bus current scale setting. This bit influences the results of IIN_LIMIT setting, IOTG setting and IBUS ADC sampling. User can refer to the corresponding registers for detailed information. 0: Choose smaller LSB for IIN_LIMIT setting, IOTG setting and IBUS ADC sampling. 1: Choose larger LSB for IIN_LIMIT setting, IOTG setting and IBUS ADC sampling. (default at POR)
5	VBAT_SCALE	R/W	0b	Battery voltage scale setting. This bit influences the results VBAT ADC sampling. User can refer to the corresponding registers for detailed information. 0: Choose smaller LSB for VBAT ADC sampling. (default at POR) 1: Choose larger LSB for VBAT ADC sampling.
4	IBAT_SCALE	R/W	1b	Battery current scale setting. This bit influences the results of IBAT_CHG setting, IBAT_DCHG setting and IBAT ADC sampling. User can refer to the corresponding registers for detailed information. 0: Choose smaller LSB for IBAT_CHG setting, IBAT_DCHG setting and IBAT ADC sampling. 1: Choose larger LSB for IBAT_CHG setting, IBAT_DCHG setting and IBAT ADC sampling. (default at POR)
3-0	Reserved	R/W	0000b	Reserved. Don't overwrite these bits.

ADC_VBUS_L Register (I2C Address = 0x12) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	ADC_VBUS_L	R	00000000b	The lowest 8-bit of the ADC value of VBUS voltage. If VBUS_SCALE=0b, full range: 20.46V, LSB: 20mV. If VBUS_SCALE=1b, full range: 24.00V, LSB: 40mV. The host must read ADC_VBUS_L register before ADC_VBUS_H register to get the right result.

ADC_VBUS_H Register (I2C Address = 0x13) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	ADC_VBUS_H	R	00b	The highest 2-bit of the ADC value of VBUS voltage. If VBUS_SCALE=0b, full range: 20.46V, LSB: 20mV. If VBUS_SCALE=1b, full range: 24.00V, LSB: 40mV. The host must read ADC_VBUS_L register before ADC_VBUS_H register to get the right result.

ADC_IBUS_L Register (I2C Address = 0x14) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	ADC_IBUS_L	R	00000000b	The lowest 8-bit of the ADC value of IBUS current. If IBUS_SCALE=0b, full range: 6393.75mA, LSB: 6.25mA. If IBUS_SCALE=1b, full range: 12787.5mA, LSB: 12.5mA. The host must read ADC_IBUS_L register before ADC_IBUS_H register to get the right result.

ADC_IBUS_H Register (I2C Address = 0x15) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	ADC_IBUS_H	R	00b	The highest 2-bit of the ADC value of IBUS current. If IBUS_SCALE=0b, full range: 6393.75mA, LSB: 6.25mA. If IBUS_SCALE=1b, full range: 12787.5mA, LSB: 12.5mA. The host must read ADC_IBUS_L register before ADC_IBUS_H register to get the right result.

ADC_VBAT_L Register (I2C Address = 0x16) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	ADC_VBAT_L	R	00000000b	The lowest 8-bit of the ADC value of VBAT voltage. If VBAT_SCALE=0b, full range: 20.46V, LSB: 20mV. If VBAT_SCALE=1b, full range: 24.00V, LSB: 40mV. The host must read ADC_VBAT_L register before ADC_VBAT_H register to get the right result.

ADC_VBAT_H Register (I2C Address = 0x17) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	ADC_VBAT_H	R	00b	The highest 2-bit of the ADC value of VBAT voltage. If VBAT_SCALE=0b, full range: 20.46V, LSB: 20mV. If VBAT_SCALE=1b, full range: 24.00V, LSB: 40mV. The host must read ADC_VBAT_L register before ADC_VBAT_H register to get the right result.

ADC_IBAT_L Register (I2C Address = 0x18) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	ADC_IBAT_L	R	00000000b	The lowest 8-bit of the ADC value of IBAT current. If IBAT_SCALE=0b, full range: 6393.75mA, LSB: 6.25mA. If IBAT_SCALE=1b, full range: 12787.5mA, LSB: 12.5mA. The host must read ADC_IBAT_L register before ADC_IBAT_H register to get the right result.

ADC_IBAT_H Register (I2C Address = 0x19) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	ADC_IBAT_H	R	00b	The highest 2-bit of the ADC value of IBAT current. If IBAT_SCALE=0b, full range: 6393.75mA, LSB: 6.25mA. If IBAT_SCALE=1b, full range: 12787.5mA, LSB: 12.5mA. The host must read ADC_IBAT_L register before ADC_IBAT_H register to get the right result.

ADC_NTC_L Register (I2C Address = 0x1A) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	ADC_NTC_L	R	00000000b	The lowest 8-bit of the ADC value of NTC pin voltage. Full range: 2.046V, LSB: 2mV. The host must read ADC_NTC_L register before ADC_NTC_H register to get the right result.

ADC_NTC_H Register (I2C Address = 0x1B) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R	000000b	Reserved
1-0	ADC_NTC_H	R	00b	The highest 2-bit of the ADC value of NTC pin voltage. Full range: 2.046V, LSB: 2mV. The host must read ADC_NTC_L register before ADC_NTC_H register to get the right result.

STATUS0 Register (I2C Address = 0x1C) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	AC_PRESENT	R	0b	Adapter attachment indication. When the ACIN voltage rises above 2.5V, this bit is set to 1 after 250ms deglitch time. When ACIN falls below 2.3V, this bit is cleared. 0b: An illegal adapter is not inserted. (default at POR) 1b: An illegal adapter is inserted.
6	Reserved	R	0b	Reserved
5	INDET	R	0b	Load insert indication. 0b: A load insertion event is not detected. (default at POR) 1b: A load insertion event is detected. Write 1 to clear this bit.
4	Reserved	R	0b	Reserved
3	BUSUVP_CHG	R	0b	Bus under-voltage protection in charge mode. When the protection conditions are removed or the chip gets out of charge mode, this bit is cleared automatically. 0b: No fault. (default at POR) 1b: BUSUV_CHG is triggered.

2	BATOVP	R	0b	Battery over-voltage protection. In charge mode, when the battery voltage exceeds 104% of the setting value, this bit is set to 1. When the battery voltage drops below 102% of the setting value, this bit is cleared automatically. 0b: No fault. (default at POR) 1b: BATOVP is triggered.
1	BAT_FULL	R	0b	Battery full indication. When battery voltage reaches the setting value and charge current is less than the threshold set in ITERM_SET bits (CTRL1 register), this bit is set to 1. When the battery voltage drops to the recharge threshold, this bit is cleared. The behavior of this bit is not affected by EN_TERM bit in CTRL1 register. Even EN_TERM bit is set to 0, this bit will be set to 1, when the corresponding conditions are met. When chip gets out of charge mode, this bit is cleared automatically. 0b: Battery not full. (default at POR) 1b: Battery full.
0	RE_CHG	R	0b	Re-charge indication. When BAT_FULL bit is cleared, due to the battery voltage lower than the recharge threshold, this bit is set to 1. This bit can be cleared by a writing 1 command. 0: Re-charge is not triggered. (default at POR) 1: Re-charge is triggered.

STATUS1 Register (I2C Address = 0x1D) [reset = 00h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	OTGOVP	R	0b	OTG over-voltage protection. When OTG output voltage exceeds 110% of the setting value, this bit is set to 1 and the protection is latched. Writing 1 to this bit can clear OTGOVP latch. When the chip exits OTG mode, this bit is cleared automatically. 0b: No fault. (default at POR) 1b: OTGOVP is triggered.

6	OTGOC	R	0b	OTG over-current indication. When the OTG output voltage drops to 80% of the setting value, this bit is set to 1. If EN_OTGOCP=1b (CTRL2 register), the chip stops switching and the protection is latched. Writing 1 to this bit can clear OTGOCP latch. If EN_OTGOCP=0b (CTRL2 register), the chip will keep switching with limited current set in IOTG and IBAT_DCHG registers. Once the OTG voltage rises above 80% of the setting value, this bit is cleared automatically. When the chip exits OTG mode, this bit is cleared automatically. 0b: No fault. (default at POR) 1b: OTGOC is triggered.
5	BAT_EMPTY	R	0b	Battery under-voltage protection. When the battery voltage drops below the threshold set in BATUVP_SEL bits (CTRL2 register) in OTG mode, this bit is set to 1 and the protection is latched. When the battery voltage rises above the threshold, write 1 to this bit to clear BAT_EMPTY latch. When the chip exits OTG mode, this bit is cleared automatically. 0b: No fault. (default at POR) 1b: BAT_EMPTY is triggered.
4	CHG_TIMEOUT	R	0b	Charge timeout. When the time this chip stays in charge mode exceeds the value set in CHG_TIMER_SET bits (CTRL3 register), it stops switching and this bit is set to 1. When the charge timer is reset (a writing 1 command to CHG_TIMER_RESET bit in CTRL3 register), this bit is cleared automatically. When the chip exits charge mode, this bit is cleared automatically. 0b: No fault. (default at POR) 1b: CHG_TIMEOUT is triggered.
3	WD_TIMEOUT	R	0b	Watchdog timeout. When watchdog timer is not reset before it is expired, this bit is set to 1 and the chip stops switching. When watchdog timer is expired, the protection can be removed by a writing 1 command to WD_RESET bit in CTRL2 register. And once the protection is removed, this bit is cleared automatically as well. 0b: No fault. (default at POR) 1b: WD_TIMEOUT is triggered.

2	TSHUT	R	0b	Thermal shutdown. When the junction temperature the chip rises above 150°C, this bit is set to 1. If the chip works in charge mode, the bit is cleared automatically, when the junction temperature drops below 130°C. If the chip works in OTG mode, the protection is latched. When the junction temperature drops below 130°C, write 1 to this bit to clear TSHUT latch. When the chip gets out of charge/OTG mode, this bit is cleared. 0b: No fault. (default at POR) 1b: TSHUT is triggered.
1	NTC_FAULT	R	0b	NTC fault. When the NTC pin voltage is outside of the setting thresholds in NTC_SET register, this bit is set to 1. If the chip works in charge mode, the bit is cleared automatically, when the NTC pin voltage is within the thresholds again. If the chip works in OTG mode, the protection is latched. When the NTC pin voltage is within the thresholds, write 1 to this bit to clear NTC_FAULT latch. When the chip gets out of charge/OTG mode, this bit is cleared. 0b: No fault. (default at POR) 1b: NTC_FAULT is triggered
0	Reserved	R	0b	Reserved

INT_EN0 Register (I2C Address = 0x1E) [reset = FFh]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7	AC_PRESENT _INT_EN	R/W	1b	0b: AC_PRESENT interrupt is disabled. 1b: AC_PRESENT interrupt is enabled. (default at POR)
6	Reserved	R/W	1b	Reserved.
5	INDET_INT_EN	R/W	1b	0b: INDET interrupt is disabled. 1b: INDET interrupt is enabled. (default at POR)
4	Reserved	R/W	1b	Reserved.
3	BUSUVP_CHG _INT_EN	R/W	1b	0b: BUSUVP_CHG interrupt is disabled. 1b: BUSUVP_CHG interrupt is enabled. (default at POR)
2	BATOVP _INT_EN	R/W	1b	0b: BATOVP interrupt is disabled. 1b: BATOVP interrupt is enabled. (default at POR)
1	BAT_FULL _INT_EN	R/W	1b	0b: BAT_FULL interrupt is disabled. 1b: BAT_FULL interrupt is enabled. (default at POR)
0	RE_CHG _INT_EN	R/W	1b	0b: RE_CHG interrupt is disabled. 1b: RE_CHG interrupt is enabled. (default at POR)

INT_MASK1 Register (I2C Address = 0x1F) [reset = 00h]

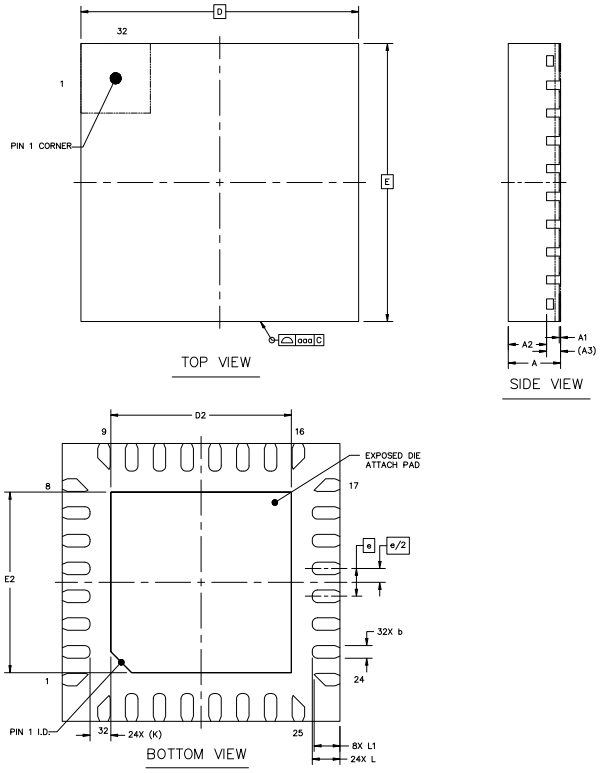
Bit	FIELD	TYPE	RESET	DESCRIPTION
7	OTGOVP _INT_EN	R/W	1b	0b: OTGOVP interrupt is disabled. 1b: OTGOVP interrupt is enabled. (default at POR)
6	OTGOC _INT_EN	R/W	1b	0b: OTGOC interrupt is disabled. 1b: OTGOC interrupt is enabled. (default at POR)
5	BAT_EMPTY _INT_EN	R/W	1b	0b: BAT_EMPTY interrupt is disabled. 1b: BAT_EMPTY interrupt is enabled. (default at POR)
4	CHG_TIMEOUT _INT_EN	R/W	1b	0b: CHG_TIMEOUT interrupt is disabled. 1b: CHG_TIMEOUT interrupt is enabled. (default at POR)
3	WD_TIMEOUT _INT_EN	R/W	1b	0b: WD_TIMEOUT interrupt is disabled. 1b: WD_TIMEOUT interrupt is enabled. (default at POR)
2	TSHUT_INT_EN	R/W	1b	0b: TSHUT interrupt is disabled. 1b: TSHUT interrupt is enabled. (default at POR)
1	NTC_FAULT _INT_EN	R/W	1b	0b: NTC_FAULT interrupt is disabled. 1b: NTC_FAULT interrupt is enabled. (default at POR)
0	Reserved	R/W	1b	Reserved. Don’t overwrite this bit.

ID Register (I2C Address = 0xFE) [reset = 04h]

Bit	FIELD	TYPE	RESET	DESCRIPTION
7-0	DEVICE_ID	R	00000100b	8-bit device ID.

PACKAGE OUTLINE

QFN4X4-32 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	- - -	0.55	- - -
A3	0.203REF		
D	4.00BSC		
E	4.00BSC		
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
k	0.30REF		
b	0.15	0.20	0.25
e	0.40BCS		
L	0.30	0.40	0.50
L1	0.272	0.372	0.472

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