# JW5255

**5A, 5.5V, 1MHz, 60uA $I_Q$**

**Synchronous Step-Down Converter**

## DESCRIPTION

The JW®5255 is a monolithic buck switching regulator based on constant on-time (COT) control for fast transient response. Operating with an input range of 2.5V-5.5V, the JW5255 delivers 5A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, the regulator operates in low frequency to maintain high efficiency.

The JW5255 guarantees robustness with hiccup output short-circuit protection, FB short-circuit protection, start-up current run-away protection, input under voltage lockout and thermal protection.

The JW5255 is available in 10-pin DFN3X3-10 package, which provides a compact solution with minimal external components.



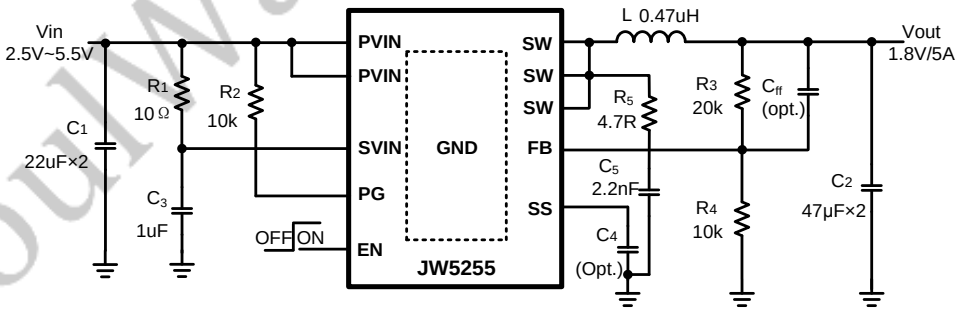
## FEATURES

- 2.5V to 5.5V operating input range
- Up to 5A output current
- Up to 94% peak efficiency
- High efficiency at light load
- Adjustable soft-start
- 1MHz switching frequency
- Input under voltage lockout
- Short circuit protection
- Thermal protection
- Power good indication
- Available in DFN3×3-10 package

## APPLICATIONS

- 5V or 3.3V Point of Load Conversion
- LCD TV
- Notebook PC
- Storage Equipment
- GPU/DDR Power Supply

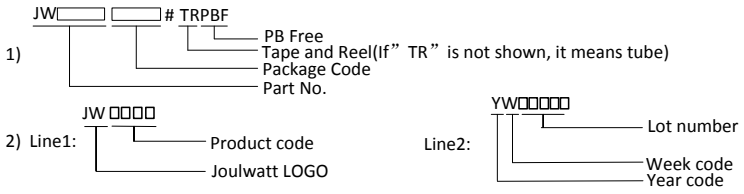
## TYPICAL APPLICATION



## ORDER INFORMATION

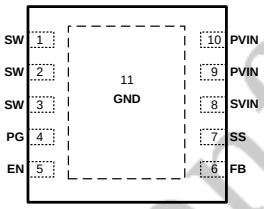
| DEVICE[1)] | PACKAGE | TOP MARKING[2)] |
|---|---|---|
| JW5255DFN#TRPBF | DFN3×3-10 | JW5255<br>YW□□□□□ |

**Notes:**




## PIN CONFIGURATION

**TOP VIEW**




**DFN3x3-10**

## ABSOLUTE MAXIMUM RATING[1)]

PVIN,SVIN,SS,FB,EN,PG Pin .....-0.3V to 6V
SW Pin .....-0.3V(-2.2V for 10ns) to 6V(6.4V for 10ns)
Junction Temperature.[2)] .....150ºC
Lead Temperature .....260ºC
Storage Temperature .....-65ºC to +150ºC

## RECOMMENDED OPERATING CONDITIONS

Input Voltage VIN .....2.5V to 5.5V
Output Voltage Vout.....0.6V to VIN
Operating Junction Temperature…..... -40ºC to 125ºC

## THERMAL PERFORMANCE[3)]

| | $\theta_{JA}$ | $\theta_{Jc}$ |
|---|---|---|
| DFN3×3-10 | 60 | 8ºC/W |

**Note:**

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
2) The JW5255 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

*VIN=5V, $T_A$=25℃, unless otherwise stated.*

| Item | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ Under Voltage Lockout Threshold | $V_{IN\_UVLO}$ | $V_{IN}$ rising | 2.3 | 2.4 | 2.5 | V |
| $V_{IN}$ Under Voltage Lockout Hysteresis[4)] | $V_{IN\_UVLO\_HYST}$ | $V_{IN}$ falling | | 200 | | mV |
| Shutdown Current | $I_{SHDN}$ | $V_{IN}$=5.5V, $V_{EN}$ 0V | | 0.1 | 1 | μA |
| Quiescent Current | $I_Q$ | $V_{EN}$=5V, $I_{OUT}$=0A, $V_{FB}$=0.7V | | 60 | 90 | μA |
| Regulated Feedback Voltage | $V_{FB}$ | 2.5V<$V_{IN}$<5.5V | 0.591 | 0.6 | 0.609 | V |
| PFET On Resistance[4)] | $R_{DSON\_P}$ | $V_{IN}$=3.6V, $I_{SW}$=200mA | | 40 | | mΩ |
| NFET On Resistance[4)] | $R_{DSON\_N}$ | $V_{IN}$=3.6V, $I_{SW}$=-200mA | | 30 | | mΩ |
| PFET Leakage Current | $I_{LEAK\_P}$ | $V_{IN}$=5.5V, $V_{EN}$=0V, $V_{SW}$=0V | | | 1 | uA |
| NFET Leakage Current | $I_{LEAK\_N}$ | $V_{IN}$=5.5V, $V_{EN}$=0V, $V_{SW}$=5.5V | | | 1 | uA |
| PFET Current Limit[4)] | $I_{LIM\_TOP}$ | | | 9 | | A |
| NFET Current Limit[4)] | $I_{LIM\_BOT}$ | | | 6 | | A |
| Switch Frequency | $F_{SW}$ | $I_{OUT}$=2A | | 1.0 | | MHz |
| Minimum On Time[4)] | $T_{ON\_MIN}$ | | | 60 | | ns |
| Maximum Duty Cycle[4)] | $D_{MAX}$ | | | | 100 | % |
| EN Rising threshold voltage | $V_{EN\_H}$ | $V_{EN}$ rising, FB=0.3V | | 1.2 | 1.35 | V |
| EN Falling threshold voltage | $V_{EN\_L}$ | $V_{EN}$ falling, FB=0.3V | 0.9 | 1 | | V |
| POK High Threshold | $V_{POKH}$ | $V_{FB}$ rising | 655 | 675 | 695 | mV |
| POK Low Threshold | $V_{POKL}$ | $V_{FB}$ falling | 500 | 525 | 550 | mV |
| Soft-start Time[4)] | $t_{ss}$ | Css=100nF | | 6 | | ms |
| | | Without Css | | 1 | | ms |
| Thermal Shutdown Threshold[4)] | $T_{SHDN}$ | | | 150 | | ℃ |
| Thermal Shutdown Hysteresis[4)] | $T_{HYST}$ | | | 20 | | ℃ |

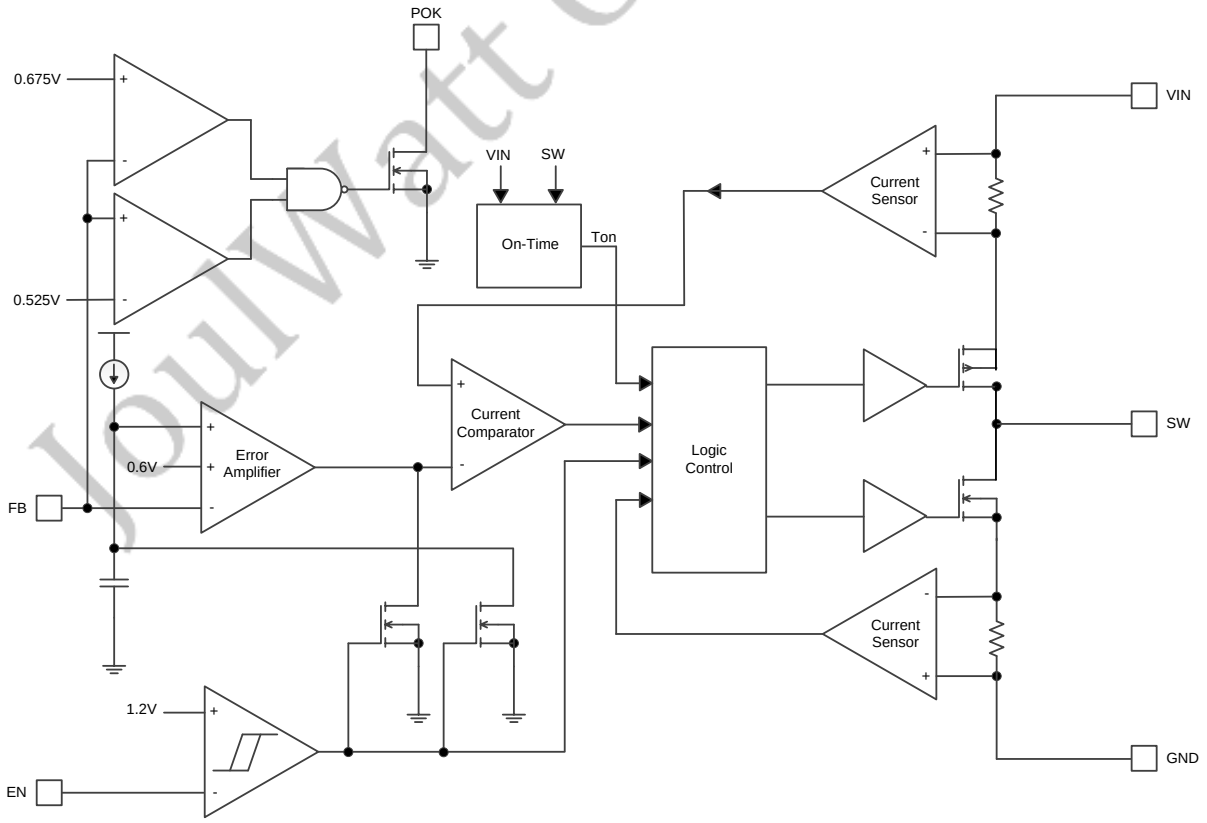
**Note:**

4) Guaranteed by design

## PIN DESCRIPTION

| Pin DFN3×3-10 | Name | Description |
|---|---|---|
| 1,2,3 | SW | SW is the switching node that supplies power to the output, and the three pins must be connected together，Connect the output LC filter from SW to the output load. |
| 4 | PG | Open drain output. Connect a 10KΩ resistor from POK to input. POK is high when $V_{FB}$ is within +/-12.5% of $V_{REF}$. |
| 5 | EN | Drive EN pin high to turn on the regulator and low to turn off the regulator. |
| 6 | FB | Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB. |
| 7 | SS | Soft start programming pin. Connect a capacitor from this pin to ground to program the soft start time. |
| 8 | SVIN | Signal power input pin. Decouple this pin to GND pin with at least 1uF ceramic capacitor. |
| 9.10 | PVIN | Power input pin. VIN supplies power to the IC. Connect a 2.5V to 5.5V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. |
| 11 | GND | Ground pin. |

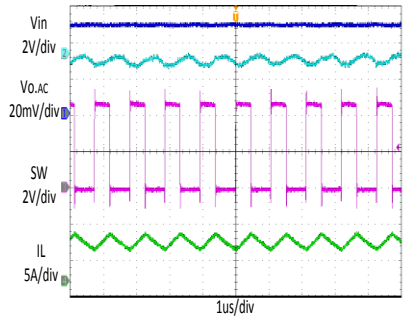
## BLOCK DIAGRAM



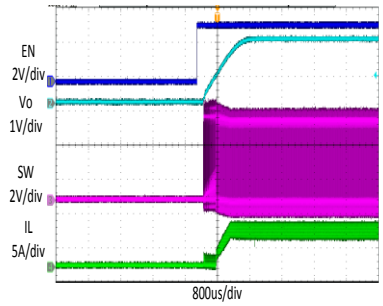
# TYPICAL PERFORMANCE CHARACTERISTICS

**Vin =5V, Vout = 1.8V, L = 0.47μH, Cout = 2*47μF，TA = +25°C, unless otherwise noted**

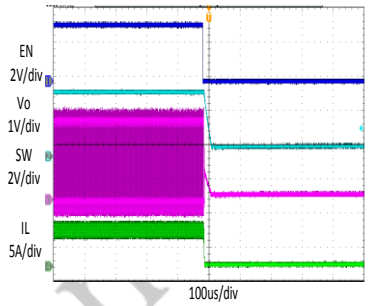
**Steady State Test**
5A LOAD



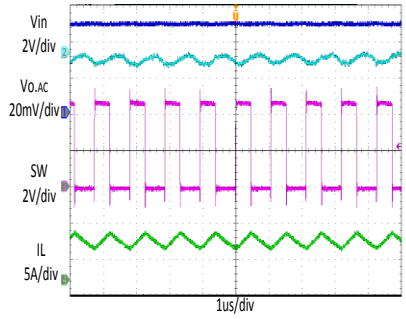

**Startup through Enable**
5A LOAD



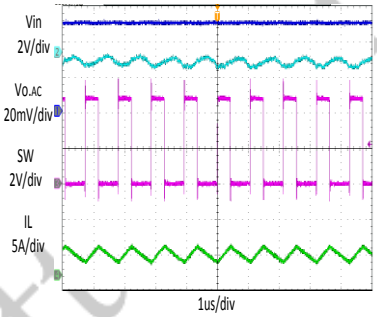

**Shutdown through Enable**
5A LOAD



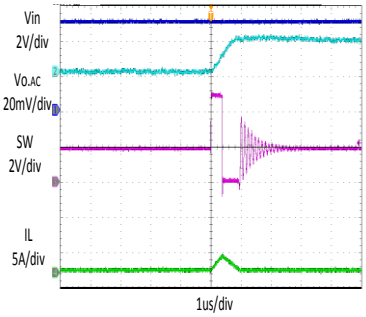

**Heavy Load Operation**
5A LOAD



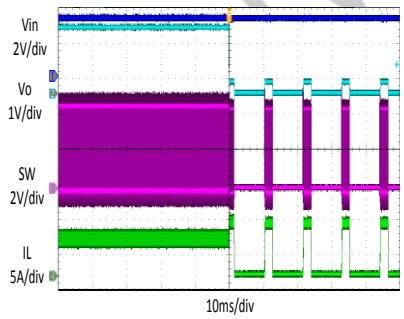

**Medium Load Operation**
2.5A LOAD



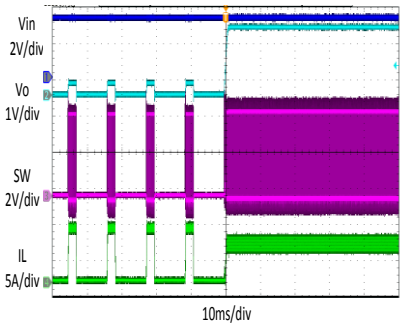

**Light Load Operation**
0A LOAD



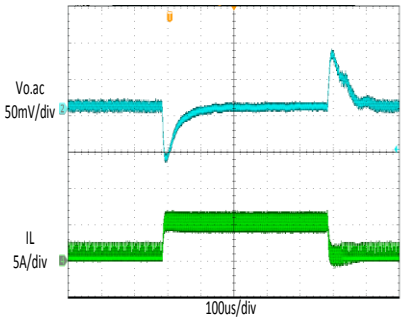

**Short Circuit Protection**
Iout=5A→ Short




**Short Circuit Recovery**
Iout= Short→5A




**Load Transient**
Cff=220pF
0.5A LOAD → 5A LOAD → 0.5A LOAD



## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Vin=5V, Vout=1.2V/1.8V/3.3V, L=0.47uH, Cout=2*47uF, TA = +25°C, unless otherwise noted**

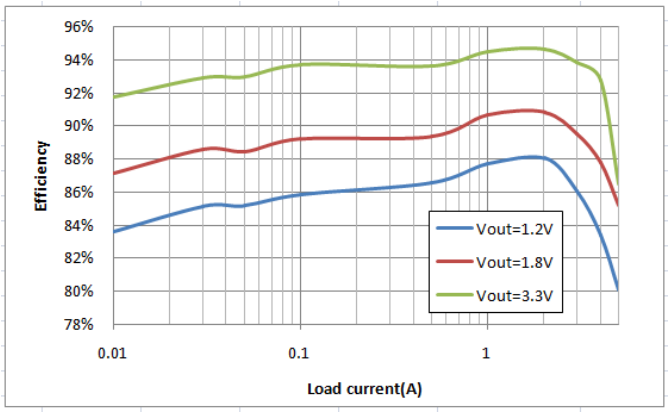



Figure 1. Efficiency vs Load Current

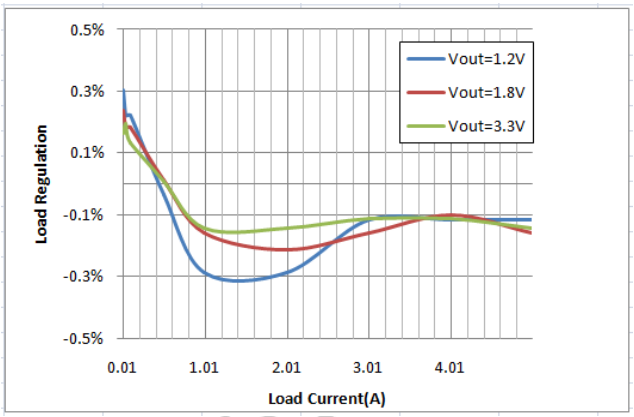



Figure 2. Output Voltage Regulation vs Load Current

## FUNCTIONAL DESCRIPTION

The JW5255 is a constant on-time control, synchronous, step-down regulator. It regulates input voltages from 2.5V~5.5V down to an output voltage as low as 0.6V, and is capable of supplying up to 5A of load current.

### Constant On-time Control

The JW5255 utilizes constant on-time control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier.
Output of the internal error amplifier is compared with the switch current measured internally to control the output current limit.

### PFM Mode

The JW5255 operates in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

### Shut-Down Mode

The JW5255 operates in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the JW5255 drops below 1uA.

### Power Switches

P-channel and N-channel MOSFET switches are integrated on the JW5255 to down convert the input voltage to the regulated output voltage.

### Short Circuit Protection

When output is shorted to ground, the switching frequency is reduced to prevent the inductor current from increasing beyond PFET current limit. If short circuit condition holds for more than 1024 cycles, both PFET and NFET are forced off and can be enabled again after 8mS. This procedure is repeated as long as short circuit condition is not removed.

### FB Short Circuit Protection

When FB is shorted to ground and holds for more 16 cycles, NFET will be turned off after inductor current drops to zero, and then both PFET and NFET are latched off. When short circuit condition is removed, it can be recovery.

### Thermal Protection

When the temperature of the JW5255 rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 130°C can the regulator becomes active again.

## APPLICATION INFORMATION

### Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_4}{R_4 + R_3}$$

where $V_{FB}$ is the feedback voltage and $V_{OUT}$ is the output voltage.

Choose $R_4$ around 10kΩ, and then $R_3$ can be calculated by:

$$R_3 = R_4 \left( \frac{V_{OUT}}{0.6V} - 1 \right)$$

Too large resistance and the following table lists the recommended values.

### Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where $I_{LOAD}$ is the load current, $V_{OUT}$ is the output voltage, $V_{IN}$ is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where $C_1$ is the input capacitance value, $f_S$ is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 2*22uF ceramic capacitor is recommended in typical application.

### Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left( R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_2} \right)$$

where $C_2$ is the output capacitance value and $R_{ESR}$ is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 47uF~ 2*47uF ceramic capacitor is recommended in typical application.

### Inductor

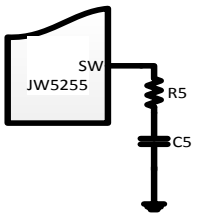
The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, $f_S$ is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

## Snubber Circuit

In order to minimize the SW negative spike voltage, a resistor in series with a capacitor circuit is recommended between SW pin and GND pin. Choose R5 around 4.7Ω and C5 around 2.2nF.




## PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5255 (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put a 0.1uF input ceramic capacitor as close to the IC as possible to eliminate the interference from the input source.
3. Put the feedback trace as far away from the inductor and noisy power traces as possible.
4. The ground plane on the PCB should be as large as possible for better heat dissipation.

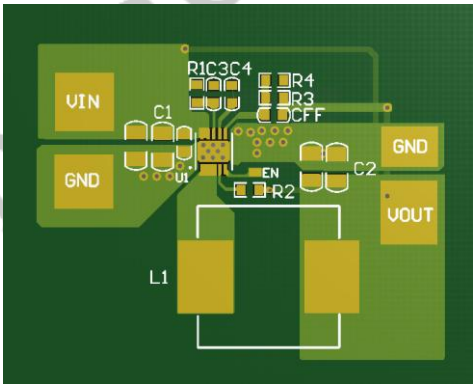
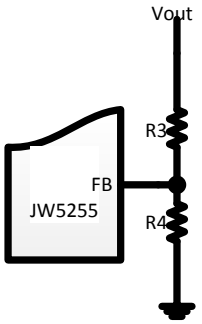



Figure1. PCB Layout Recommendation

## External Components Suggestions：

| Vout(V) | R4(kΩ) | R3(kΩ) | Inductor L(uH) | Cout(uF) |
|---|---|---|---|---|
| 1 | 15 | 10 | 0.47~0.68 | 2*47 |
| 1.2 | 20 | 20 | 0.47~0.68 | 2*47 |
| 1.8 | 10 | 20 | 0.47~1 | 47~2*47 |
| 2.5 | 11 | 34.8 | 0.47~1 | 47~2*47 |
| 3.3 | 11 | 49.9 | 0.47~1 | 47~2*47 |



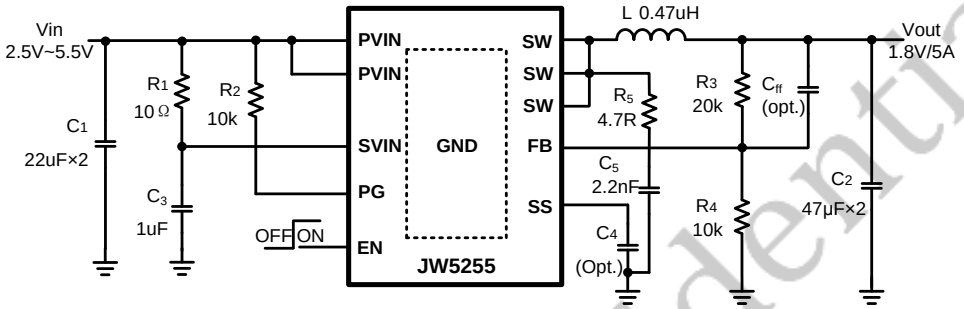
# REFERENCE DESIGN

## Reference 1:

$V_{IN}$ : 2.5V ~ 5.5 V

$V_{OUT}$: 1.8V

$I_{OUT}$ : 0~5A

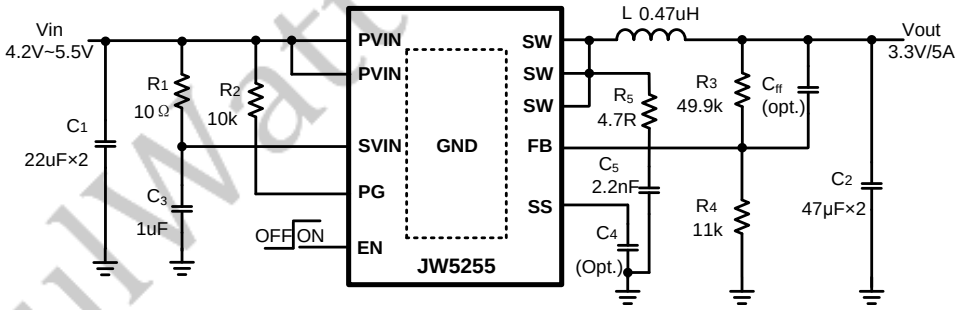



## Reference 2:

$V_{IN}$ : 4.2V ~ 5.5V

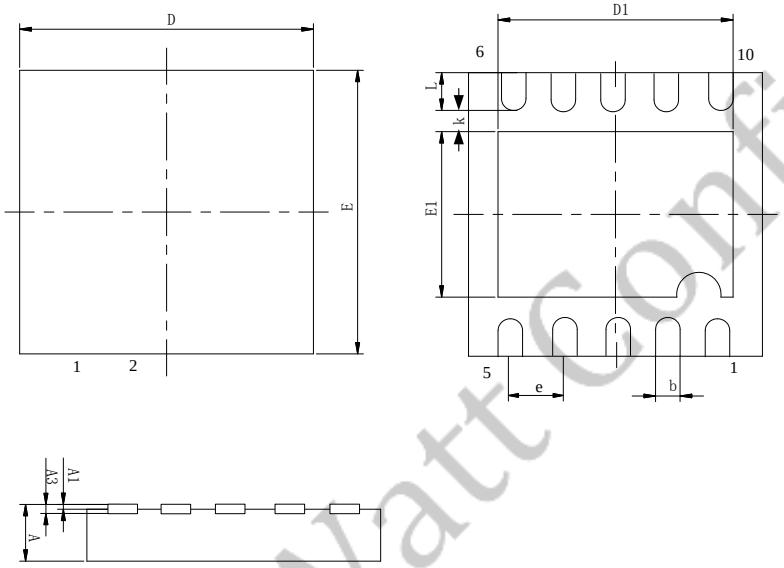
$V_{OUT}$: 3.3V

$I_{OUT}$ : 0~5A



## PACKAGE OUTLINE

DFN3x3-10 UNIT: mm




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | — | 0.05 |
| A3 | 0.203REF | | |
| D | 2.80 | 3.00 | 3.20 |
| E | 2.80 | 3.00 | 3.20 |
| D1 | 2.30 | 2.40 | 2.50 |
| E1 | 1.60 | 1.70 | 1.80 |
| k | 0.20 | — | 0.30 |
| b | 0.20 | 0.25 | 0.30 |
| e | 0.50BCS | | |
| L | 0.32 | — | 0.48 |

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