

JW5255A

5A, 5.5V, 1MHz, 60uA I_Q Synchronous Step-Down Converter

DESCRIPTION

The JW[®]5255A is a monolithic buck switching regulator based on constant on-time (COT) control for fast transient response. Operating with an input range of 2.5V-5.5V, the JW5255A delivers 5A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, the regulator operates in low frequency to maintain high efficiency.

The JW5255A guarantees robustness with hiccup output short-circuit protection, FB short-circuit protection, start-up current run-away protection, input under voltage lockout and thermal protection.

The JW5255A is available in 10-pin DFN3X3-10 package, which provides a compact solution with minimal external components.

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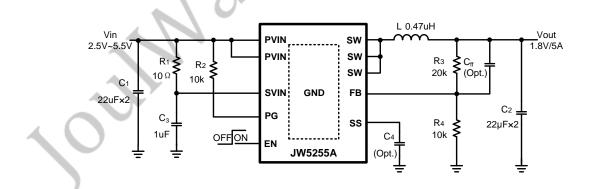
FEATURES

- 2.5V to 5.5V operating input range
- Up to 5A output current
- Up to 94% peak efficiency
- High efficiency at light load
- Adjustable soft-start
- 1MHz switching frequency
- Input under voltage lockout
- Short circuit protection
- Thermal protection
- Power good indication
- Available in DFN3x3-10 package

APPLICATIONS

- 5V or 3.3V Point of Load Conversion
- LCD TV
- Notebook PC
- Storage Equipment
- GPU/DDR Power Supply

TYPICAL APPLICATION



ORDER INFORMATION

		PACKAGE	TOP MARKING ²⁾	ENVIRONMENTAL ³⁾
	JW5255ADFN#TR	DFN3×3-10	JW5255	Green
	JW 5255ADFIN#TK	DEN2×2-10	YWDDDDD	Green
Notes:				
1) JW[] 2) Line1:	Tape and Reel (If TR is not Package Code Part No. JW DDD Product code Joulwatt LOGO	YW 00000		.2
3) All Jouly	vatt products are packaged with Pb-free and Halo	gen-free materials and compliant	to RoHS standards.	
		TOP VIEW	j PVIN	
		sw 2 11 9	i pvin i svin i ss	
ABSO	LUTE MAXIMUM RAT	SW 2 11 9 SW 3 GND 8 PG 4 17 EN 5 C 6 DFN3x3-10	i pvin i svin i ss	
	LUTE MAXIMUM RAT	SW 2 11 SW 3 GND 8 PG 4 6 EN 5 CONTRACTOR 6 DFN3x3-10	PVIN SVIN SS	0.3V
VIN,S∖ ₩ Pin	/IN,SS,FB,EN,PG Pin	SW 2 11 9 SW 3 GND 9 PG 4 77 EN 5 77 DFN3x3-10	I PVIN SVIN SS FB	
VIN,S\ SW Pin unction	/IN,SS,FB,EN,PG Pin Temperature ²⁾	SW 2 11 SW 3 GND 9 PG 4 77 EN 5 77 DFN3x3-10	Г РVIN SVIN SS FB 0.3V(-3V for 10	ns) to 6V(7.5V for 10 150
PVIN,S\ SW Pin lunction .ead Te	/IN,SS,FB,EN,PG Pin	SW 2 11 SW 3 GND 8 PG 4 2 EN 5 2 DFN3x3-10	PVIN SVIN SS FB 	ns) to 6V(7.5V for 10 150

RECOMMENDED OPERATING CONDITIONS³⁾

Input Voltage VIN	2.5V to 5.5V
Output Voltage Vout	0.6V to VIN
Operating Junction Temperature	40°C to 125°C

THERMAL PERFORMANCE⁴⁾

 θ_{JA} θ_{Jc}

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

- 2) The JW5255A includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN=5V, T_A =25 °C, unless otherwise stated.						
ltem	Symbol	Condition	Min.	Тур.	Max.	Units
V _{IN} Under Voltage Lockout Threshold	V _{IN_UVLO}	V _{IN} rising	2.3	2.4	2.5	V
V _{IN} Under Voltage Lockout Hysteresis ⁵⁾	$V_{\text{IN}_\text{UVLO}_\text{HYST}}$	V _{IN} falling		200		mV
Shutdown Current	I _{SHDN}	V_{IN} =5.5V, V_{EN} 0V		0.1	1	μA
Quiescent Current	lq	V _{EN} =5V, I _{OUT} =0A, V _{FB} =0.7V		60	90	μA
Regulated Feedback Voltage	V _{FB}	2.5V <v<sub>IN<5.5V</v<sub>	0.591	0.6	0.609	V
PFET On Resistance ⁵⁾	R _{DSON_P}	V _{IN} =3.6V, I _{SW} =200mA		40	5	mΩ
NFET On Resistance ⁵⁾	R _{DSON_N}	V _{IN} =3.6V, I _{sw} =-200mA	0	30		mΩ
PFET Leakage Current	I _{LEAK_P}	V _{IN} =5.5V, V _{EN} =0V, V _{SW} =0V	6		1	uA
NFET Leakage Current	I _{LEAK_N}	V _{IN} =5.5V, V _{EN} =0V, V _{SW} =5.5V	5		1	uA
PFET Current Limit ⁵⁾	I _{LIM_TOP}			9		А
NFET Current Limit ⁵⁾	I _{LIM_BOT}			6		А
Switch Frequency	F _{sw}	I _{OUT} =2A		1.0		MHz
Minimum On Time ⁵⁾	T _{ON_MIN}	7		60		ns
Maximum Duty Cycle ⁵⁾	D _{MAX}				100	%
EN Rising threshold voltage	V _{EN_H}	V _{EN} rising, FB=0.3V		1.2	1.35	V
EN Falling threshold voltage	V _{EN_L}	V _{EN} falling, FB=0.3V	0.9	1		V
POK High Threshold	V _{POKH}	V _{FB} rising	655	675	695	mV
POK Low Threshold	V _{POKL}	V _{FB} falling	500	525	550	mV
Soft-start Time ⁵⁾	t _{ss}	Css=100nF		6		ms
		Without Css		1		ms
Thermal Shutdown Threshold ⁵⁾	T _{SHDN}			150		°C
Thermal Shutdown Hysteresis ⁵⁾	T _{HYST}			20		°C

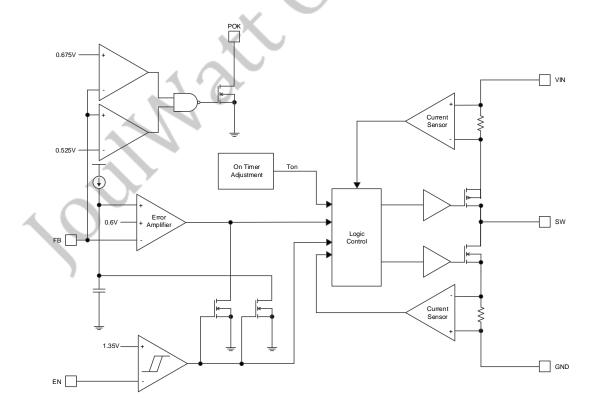
Note:

5) Guaranteed by design

PIN DESCRIPTION

Pin DFN3×3-10	Name	Description
1,2,3	SW	SW is the switching node that supplies power to the output, and the three pins must be
1,2,5	011	connected together, Connect the output LC filter from SW to the output load.
4	PG	Open drain output. Connect a $10 K\Omega$ resistor from POK to input. POK is high when V_{FB} is
4	PG	within 525mV to 675mV.
5	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
6	FD	Output feedback pin. FB senses the output voltage and is regulated by the control loop to
6	FB	0.6V. Connect a resistive divider at FB.
7		Soft start programming pin. Connect a capacitor from this pin to ground to program the
7	SS	soft start time.
8	SVIN	Signal power input pin. Decouple this pin to GND pin with at least 1uF ceramic capacitor.
		Power input pin. VIN supplies power to the IC. Connect a 2.5V to 5.5V supply to VIN and
9.10	PVIN	bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the
		IC.
11	GND	Ground pin.

BLOCK DIAGRAM



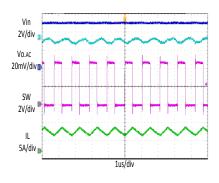
TYPICAL PERFORMANCE CHARACTERISTICS

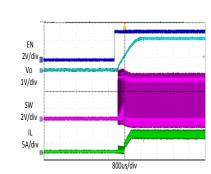
Vin =5V, Vout = 1.8V, L = 0.47µH, Cout = 2*22µF, TA = +25°C, unless otherwise noted

5A LOAD

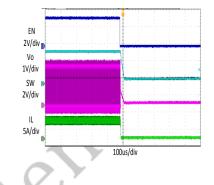
Startup through Enable

Steady State Test 5A LOAD

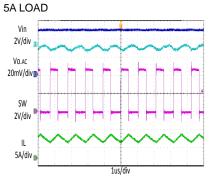




Shutdown through Enable 5A LOAD

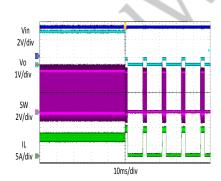


Heavy Load Operation

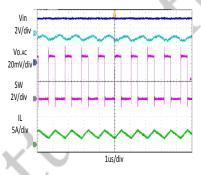


Short Circuit Protection

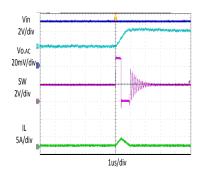
lout=5A→ Short



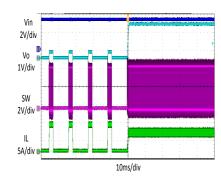
Medium Load Operation 2.5A LOAD



Light Load Operation

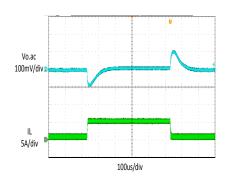


Short Circuit Recovery lout= Short→5A



Load Transient

Cff=150pF 0.5A LOAD \rightarrow 5A LOAD \rightarrow 0.5A LOAD

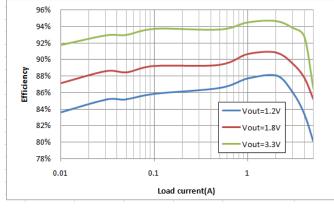


Vout=1.2V

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

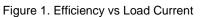
Vin=5V, Vout=1.2V/1.8V/3.3V, L=0.47uH, Cout=2*22uF, TA = +25°C, unless otherwise noted

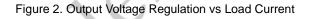
0.5%



0.1%

0.3% Vout=1.8V Vout=3.3V Load Regulation -0.1% -0.3% -0.5% 0.01 1.01 2.01 3.01 4.01 Load Current(A)





FUNCTIONAL DESCRIPTION

The JW5255A is a constant on-time control, synchronous, step-down regulator. It regulates input voltages from 2.5V~5.5V down to an output voltage as low as 0.6V, and is capable of supplying up to 5A of load current.

Constant On-time Control

The JW5255A utilizes constant on-time control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier.

Output of the internal error amplifier is compared with the switch current measured internally to control the output current limit.

PFM Mode

The JW5255A operates in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

Shut-Down Mode

The JW5255A operates in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the JW5255A drops below 1uA.

Power Switches

P-channel and N-channel MOSFET switches are integrated on the JW5255A to down convert the input voltage to the regulated output voltage.

Short Circuit Protection

When output is shorted to ground, the switching frequency is reduced to prevent the inductor current from increasing beyond PFET current limit. If short circuit condition holds for more than 1024 cycles, both PFET and NFET are forced off and can be enabled again after 8mS. This procedure is repeated as long as short circuit condition is not removed.

FB Short Circuit Protection

When FB is shorted to ground and holds for more 16 cycles, NFET will be turned off after inductor current drops to zero, and then both PFET and NFET are latched off. When short circuit condition is removed, it can be recovery.

Thermal Protection

When the temperature of the JW5255A rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 130°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$v_{FB} = v_{OUT} \cdot \frac{R_4}{R_4 + R_3}$$

where VFB is the feedback voltage and VOUT is the output voltage.

Choose R4 around $10k\Omega$, and then R3 can be calculated by:

$$R_3 = R_4 \left(\frac{V_{OUT}}{0.6V} - 1\right)$$

Too large resistance and the following table lists the recommended values.

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where ILOAD is the load current, VOUT is the output voltage, VIN is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$c_{1} = \frac{I_{LOAD}}{f_{s} \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C1 is the input capacitance value, fs is the switching frequency, $\bigtriangleup V \mbox{IN}$ is the input ripple

voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 2*22uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_{\text{s}} \cdot L} \cdot \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \cdot \left(R_{\text{ESR}} + \frac{1}{8 \cdot f_{\text{s}} \cdot C_2}\right)$$

where C₂ is the output capacitance value and RESR is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 44uF~ 88uF ceramic capacitor is recommended in typical application.

Inductor

4

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_{s} \cdot \Delta I_{L}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where VIN is the input voltage, VOUT is the output voltage, fs is the switching frequency, and \triangle IL is the peak-to-peak inductor ripple current.

Snubber Circuit

If the PCB layout is not ideal, in order to minimize the SW spike voltage, a resistor in series with a capacitor circuit is recommended between SW pin and GND pin. Choose R5 around 4.7Ω and C5 around 2.2nF.

SW JW5255A RS

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following

the guidelines as reference.

- Place the input decoupling capacitor as close to JW5255A (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
- Put a 0.1uF input ceramic capacitor as close to the IC as possible to eliminate the interference from the input source.
- 3. Put the feedback trace as far away from the inductor and noisy power traces as possible.
- 4. The ground plane on the PCB should be as large as possible for better heat dissipation.

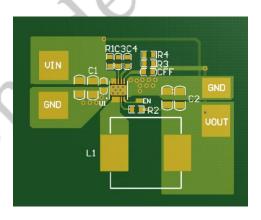


Figure 1. PCB Layout Recommendation

External Components Suggestions:

Vout(V)	R4(kΩ)	R3(kΩ)	Inductor L(uH)	Cff(pF)	Cout(uF)
1	15	10	0.47~0.68	0~220	66~88
1.2	20	20	0.47~0.68	0~220	66~88
1.8	10	20	0.47~1	0~150	44~88
2.5	11	34.8	0.47~1	0~120	44~88
3.3	11	49.9	0.47~1	0~120	44~88

Voµt

R3

R4€

FB JW5255A Cff(Opt.)

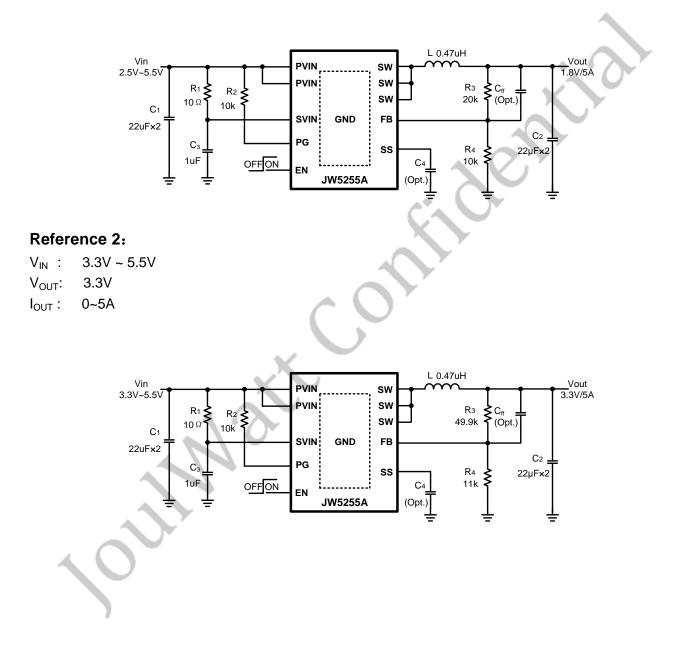


REFERENCE DESIGN

Reference 1:

 V_{IN} : 2.5V ~ 5.5 V V_{OUT} : 1.8V

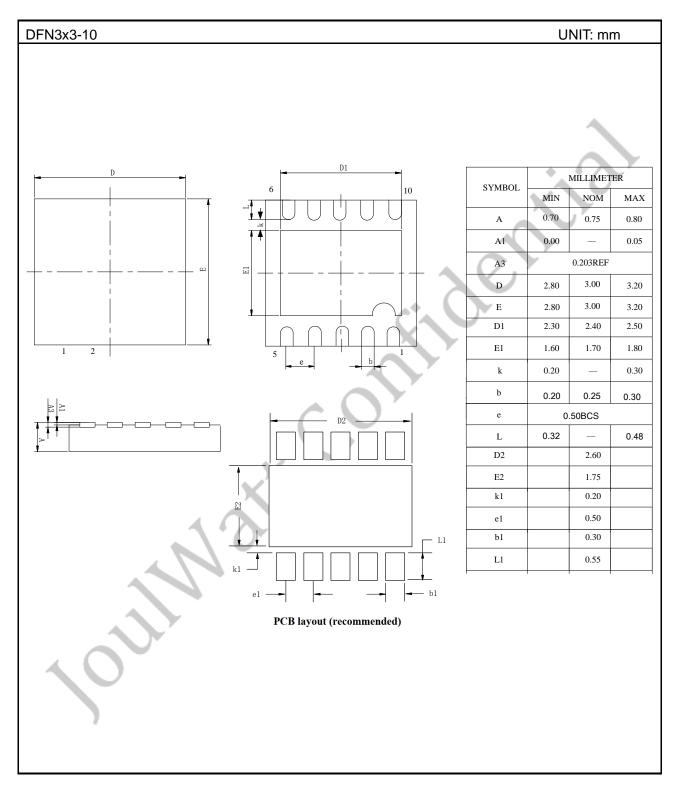
I_{OUT} : 0~5A



TAPE AND REEL INFORMATION

Carrier Tape	UNIT: mm
DFN3X3-10:	
Reel 1 pin the minimum quantity.	
FIC.	

PACKAGE OUTLINE



IMPORTANT NOTICE

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