JW5305/JW5305F

18V/5A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®5305 and JW®5305F are monolithic buck switching regulators based on I2 architecture for fast transient response. Operating with an input range of 4.5V~18V, JW5305 and JW5305F deliver 5A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode.

JW5305 and JW5305F guarantees robustness with output short protection, thermal protection, current run-away protection, and input under voltage lockout.

JW5305 and JW5305F are available in ESOP8 package, which provide a compact solution with minimal external components.

FEATURES

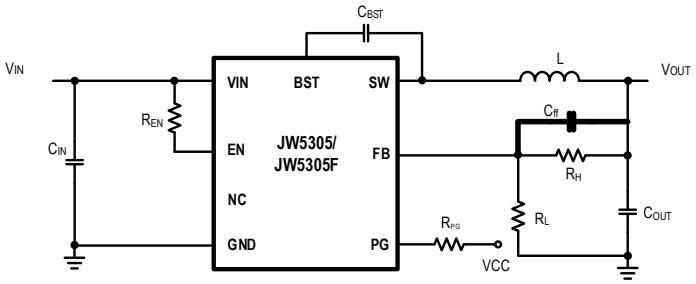
- 4.5V to 18V operating input range
  5A output current
- 580kHz switching frequency
- 1% feedback voltage accuracy
- Internal soft-start
- Power good indicator
- PFM operation at light load (JW5305)
  FCCM operation at light load (JW5305F)
- Output short protection
- Thermal protection
- Available in ESOP8 package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

TYPICAL APPLICATION

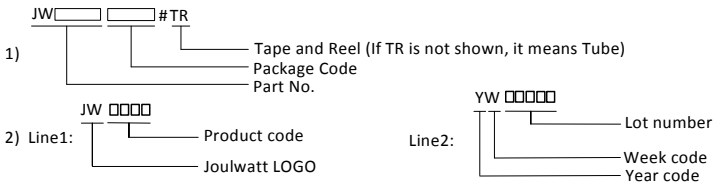
18V/5A Step Down Regulator



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW5305ESOP#TR	ESOP8	JW5305 YW□□□□□	Green
JW5305FESOP#TR	ESOP8	JW5305F YW□□□□□	Green

Notes:



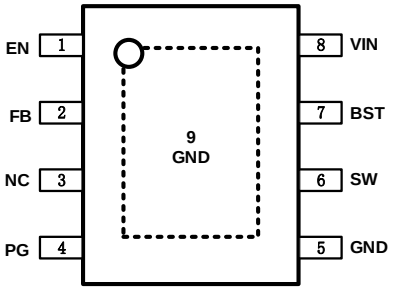
3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

DEVICE INFORMATION

DEVICE	Operation Mode at light load	Function	Package
JW5305ESOP#TR	PFM	-	ESOP8
JW5305FESOP#TR	FCCM	-	ESOP8

PIN CONFIGURATION

TOP VIEW



ESOP8

ABSOLUTE MAXIMUM RATING[1)]

VIN, EN Pin..... -0.3V to 20V
SW Pin .....-0.3V(-4V for 10ns) to 20V(22V for 5ns)
BST Pin ..... SW-0.3V to SW+5V
All other Pins ..... -0.3V to 6V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC
ESD Susceptibility (Human Body Model)..... 2kV
ESD Susceptibility (Charged Device Model).....500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN 4.5V to18V
Output Voltage VOUT .....0.765V to VIN-3V
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
ESOP8	42	2.5ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW5305 and JW5305F includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

VIN=12V, TA=-40℃~125℃，Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising	4	4.2	4.45	V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			300		mV
Shutdown Current	I_{SD}	V_{EN}=0V			1	μA
Quiescent Current	I_Q	V_{EN}=5V, V_{FB}=1.2V		130	200	μA
Feedback Voltage	V_{FB}	4.5V≤V_{IN}≤18V TA=25℃	757	765	773	mV
		TA = -40 to 125℃	751	765	779	mV
Top Switch Resistance[5)]	$R_{DS(ON)T}$			45		mΩ
Bottom Switch Resistance[5)]	$R_{DS(ON)B}$			30		mΩ
Top Switch Leakage Current[5)]	I_{LEAK_TOP}	V_{IN}=18V, V_{EN}=0V, V_{SW}=0V			1	μA
Bottom Switch Leakage Current[5)]	I_{LEAK_BOT}	V_{IN}=18V, V_{EN}=0V, V_{SW}=18V			1	μA
Bottom Switch Current Limit	I_{LIM_BOT}		5.5	7.5	9	A
Negative Current Limit	I_{LIM_NEG}	JW5305F		-3		A
Minimum On Time[5)]	T_{ON_MIN}			120		ns
Minimum Off Time[5)]	T_{OFF_MIN}	V_{FB}=0.4V		200		ns
Switching Frequency	Fs		493	580	667	kHz
EN rising Threshold	V_{EN_H}		1.15	1.35	1.55	V
EN falling Threshold	V_{EN_L}		0.9	1.1	1.3	V
Power Good Upper Threshold	PG_{TH_Upper}	FB rising	120%	124%	128%	V_{REF}
Power Good Lower Threshold	PG_{TH_lower}	FB rising	87%	90%	94%	V_{REF}
		FB falling	82%	85%	89%	V_{REF}
Power Good Sink Current	$I_{\_PG}$	PG=0.5V	0.6			mA
Soft-start Time[5)]	t_{ss}			1.2		ms
Thermal Shutdown[5)]	T_{TSD}			160		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			40		°C

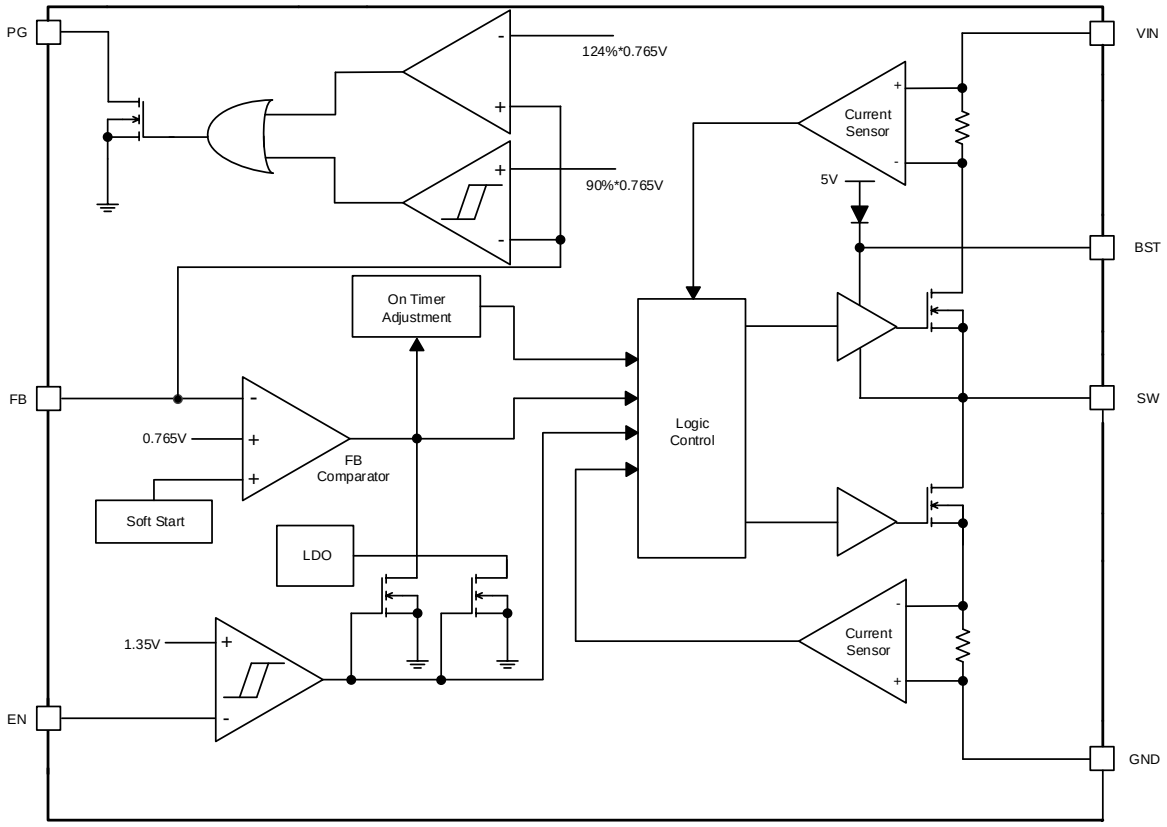
Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin ESOP8	Name	Description
1	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
2	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.765V. Connect a resistive divider at FB.
3	NC	
4	PG	Power good monitor output. This is an open-drain output so a resistor should be connected at this pin to the VOUT node or other power rail.
5	GND	Power ground pin
6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
7	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
8	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
9	GND	Power ground pin

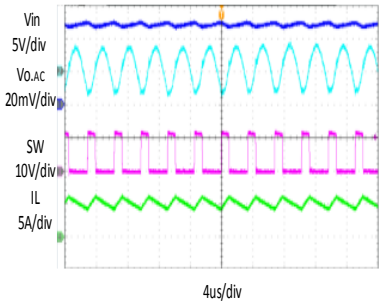
BLOCK DIAGRAM



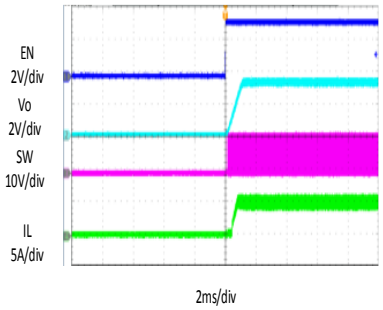
TYPICAL PERFORMANCE CHARACTERISTICS (PFM Mode)

V_{IN}=12V, V_{OUT} = 3.3V, L = 2.2μH, C_{OUT}= 44μF, Cff=51pF，TA = +25°C, unless otherwise noted

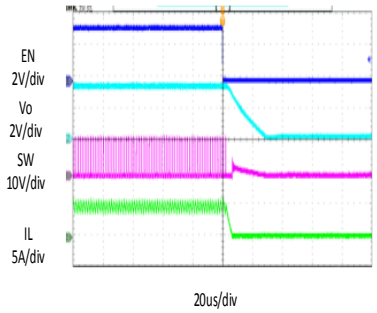
Steady State Test
V_{IN}=12V, V_{OUT}=3.3V
I_{OUT}=5A



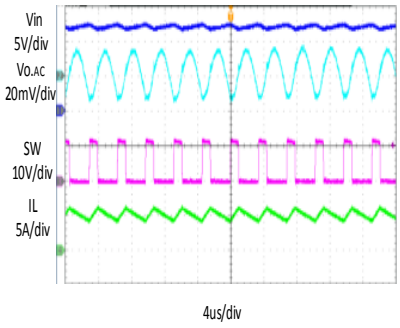
Startup through Enable
V_{IN}=12V, V_{OUT} =3.3V
I_{OUT} =5A(Resistive load)



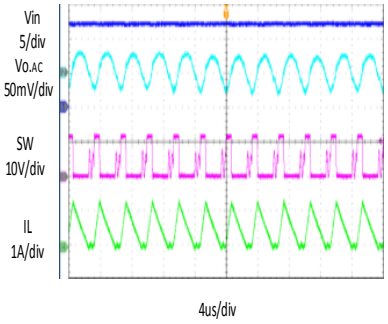
Shutdown through Enable
V_{IN}=12V, V_{OUT} =3.3V
I_{OUT} =5A (Resistive load)



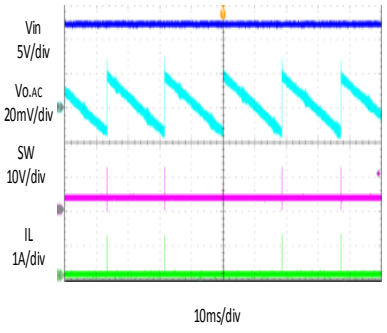
Heavy Load Operation
5A LOAD



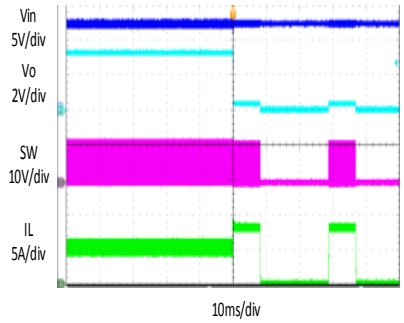
Medium Load Operation
0.5A LOAD



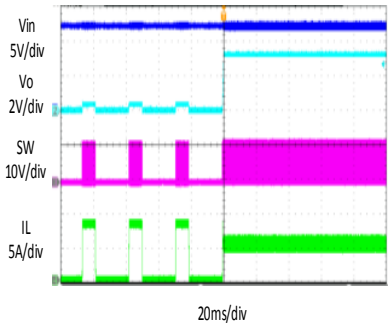
Light Load Operation
0 A LOAD



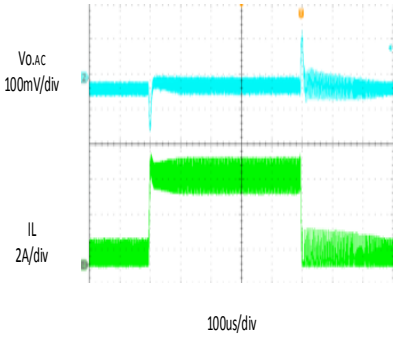
Short Circuit Protection
V_{IN}=12V, V_{OUT} 3.3V
I_{OUT} =5A- Short



Short Circuit Recovery
V_{IN}=12V, V_{OUT} =3.3V
I_{OUT} = Short-5A



Load Transient
0.5A LOAD → 5A LOAD → 0.5A LOAD



TYPICAL PERFORMANCE CHARACTERISTICS (PFM Mode)

V_{IN} =12V, V_{OUT} = 3.3V, L = 2.2μH, C_{OUT} = 44μF, TA = +25°C, unless otherwise noted

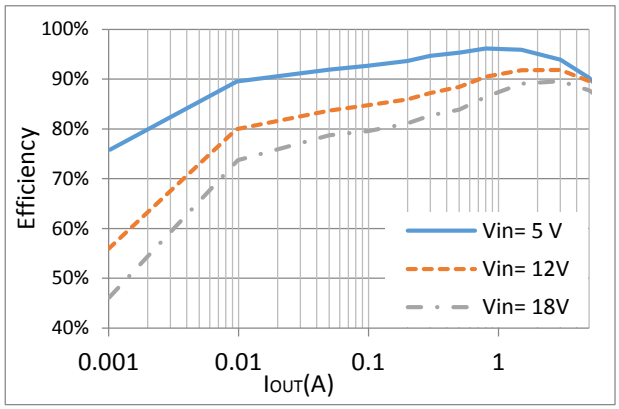


Figure 1. Efficiency vs IOUT

(VOUT =3.3V, L=2.2uH)

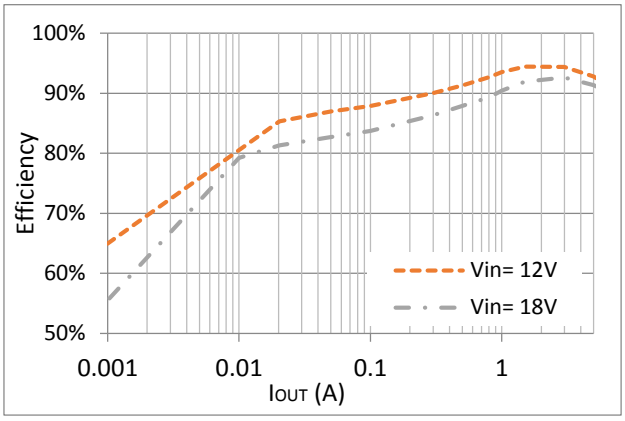


Figure 2. Efficiency vs IOUT

(VOUT =5V, L=3.3uH)

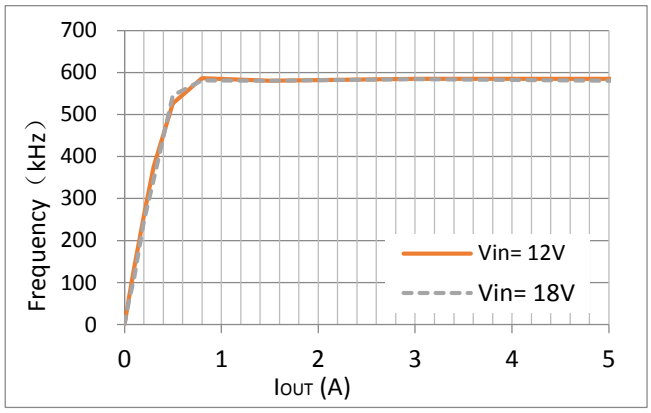


Figure 3. Frequency vs IOUT

(VOUT =3.3V, L=2.2uH)

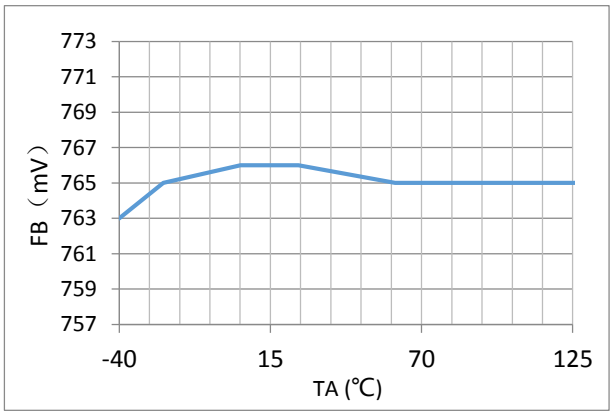


Figure 4. FB Voltage vs Ambient temperature

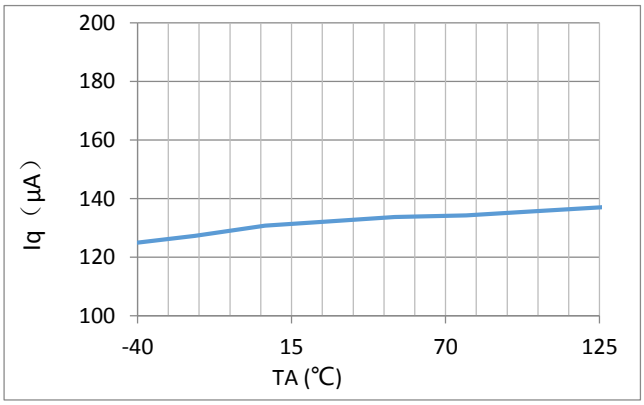


Figure 5. Quiescent Current vs Ambient temperature

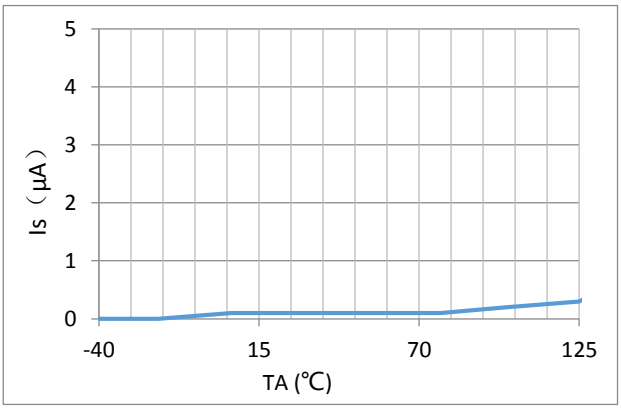


Figure 6. Shutdown Current vs Ambient temperature

FUNCTIONAL DESCRIPTION

JW5305 and JW5305F are synchronous step-down regulators based on I2 control architecture. It regulates input voltages from 4.5V to 18V down to an output voltage as low as 0.765V, and is capable of supplying up to 5A of load current.

Shut-Down Mode

JW5305 and JW5305F shut down when voltage at EN pin is driven below 0.3V. The entire regulator is off and the supply current consumed by JW5305 or JW5305F drops below 1uA.

Power Switch

N-Channel MOSFET switches are integrated on the JW5305 and JW5305F to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 5V rail when SW is low.

PFM Mode/FCC Mode

Different operation mode at light load is design in JW5305 and JW5305F. PFM mode is integrated on JW5305 and FCCM mode is integrated on JW5305F. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples. In FCC mode, switch frequency keeps constant to prevent low frequency interference.

Internal Soft-start.

Soft-start makes output voltage rising smoothly follow an internal SS voltage until SS voltage is higher than the internal reference voltage. It can prevent overshoot of output voltage when startup. The soft-start time is typically 1.2ms.

VIN Under-Voltage Protection

A resistive divider can be connected between VIN and ground, with the central tap connected to EN, so that when VIN drops to the pre-set value, EN drops below 1.1V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current.
A valley current limit is designed in JW5305 and JW5305F so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 7ms. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 7ms, then no switching is allowed and the regulator enters hiccup mode for 21ms. After the 21ms the regulator will try to start-up again. If the short condition still exists after 7ms, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

Power Good

The power good function is activated after soft start has finished. When the output voltage becomes within 90% of the target value, internal comparators detect power good state and the power good signal becomes high. The power good output, PG is an open drain output. If the FB voltage goes under 15% of the target value, the power good signal becomes low. When the output voltage goes higher than 24% of the target value, the power good signal becomes low.

The resistance value which is connected between PG and V_{OUT} is required from 15kΩ to 150kΩ.

Thermal Protection

When the temperature of the device rises above 160°C, it is forced into thermal shut-down. Only when core temperature drops below 120°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_L}{R_L + R_H}$$

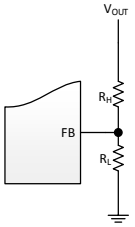
where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_L around 16kΩ, and then R_H can be calculated by:

$$R_H = R_L \cdot \left(\frac{V_{OUT}}{0.765} - 1 \right)$$

Too large resistance and the following table lists the recommended values.

V_{OUT}(V)	R_L(kΩ)	R_H(kΩ)
1	22.1	6.8
1.2	28	16
1.5	16	15.4
2.5	20.5	46.4
3.3	22.1	73.2
5	22.1	124



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_S \cdot \Delta VI_N} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

2*10uF/25V~3*10uF/25V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 44uF

ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

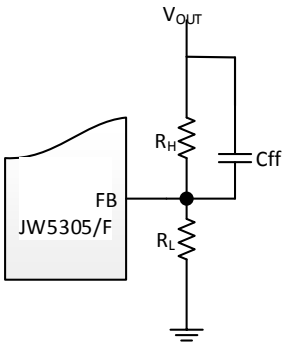
where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

Feedforward Capacitor

In order to improve the stability and the performance at load transient, a feedforward capacitor should be in parallel to the upper divider resistor. Choose Cff around 51pF.



PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5305/F (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.
4. Keep the switching node SW short to prevent excessive capacitive coupling
5. Make VIN, VOUT and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

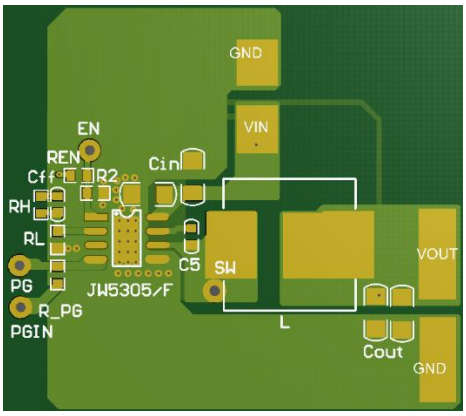
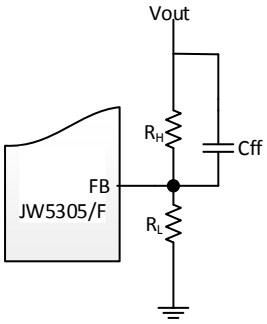


Figure 7. JW5305/F_ESOP8 PCB Layout Recommendation

External Components Suggestion:

V_{OUT}(V)	R_L (kΩ)	R_H (kΩ)	Cff (pF)	L(uH)	C_{OUT}(uF)
1	22.1	6.8	51	1	44
1.2	28	16	51	1	44
1.5	16	15.4	51	1	44
2.5	20.5	46.4	51	1.5	44
3.3	22.1	73.2	51	2.2	44
5	22.1	124	20	3.3	44



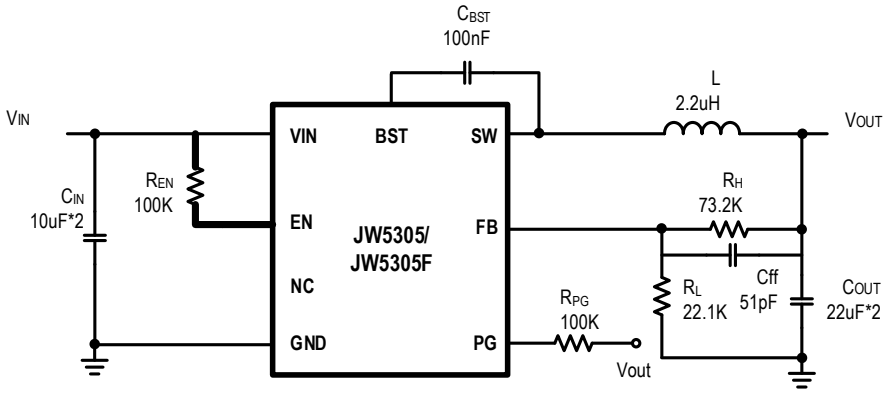
REFERENCE DESIGN

Reference 1:

V_{IN} : 12V

V_{OUT}: 3.3V

I_{OUT}: 0~5A

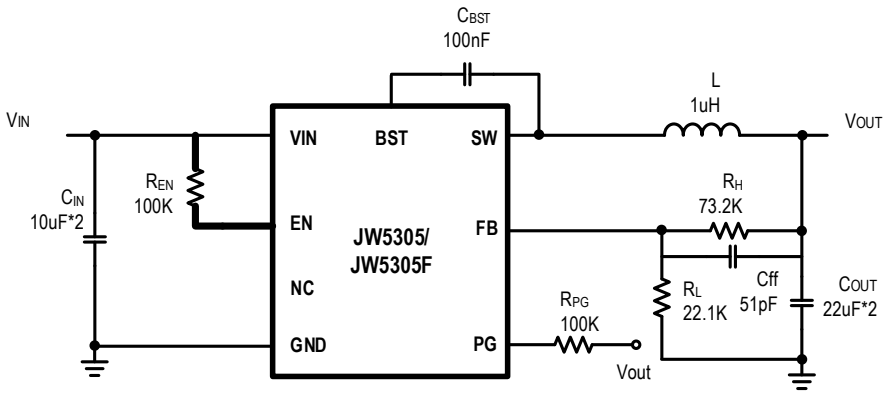


Reference 2:

V_{IN} : 5V

V_{OUT}: 3.3V

I_{OUT} : 0~5A

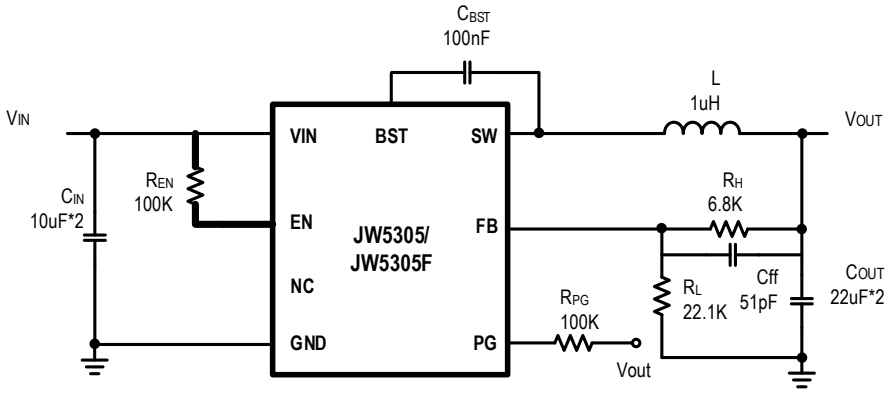


Reference 3:

VIN : 12V

V_{OUT}: 1V

I_{OUT} : 0~5A

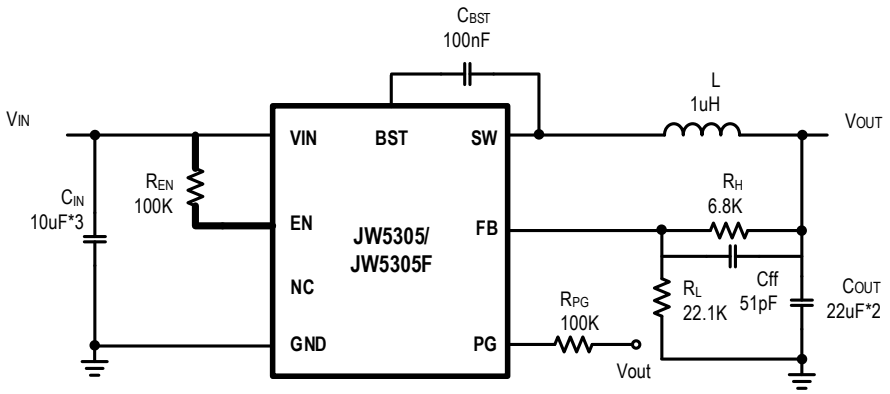


Reference 4:

VIN : 5V

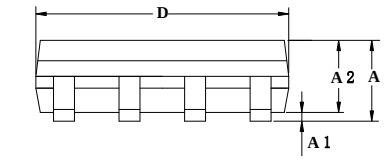
V_{OUT}: 1V

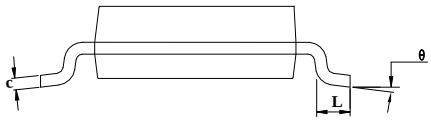
I_{OUT}: 0~5A

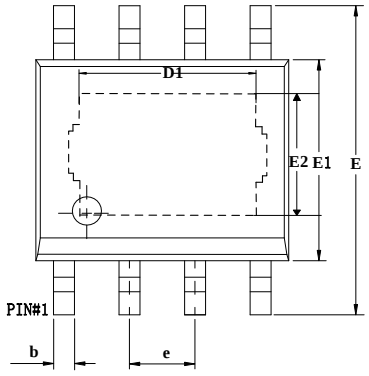


PACKAGE OUTLINE

ESOP8 UNIT: mm

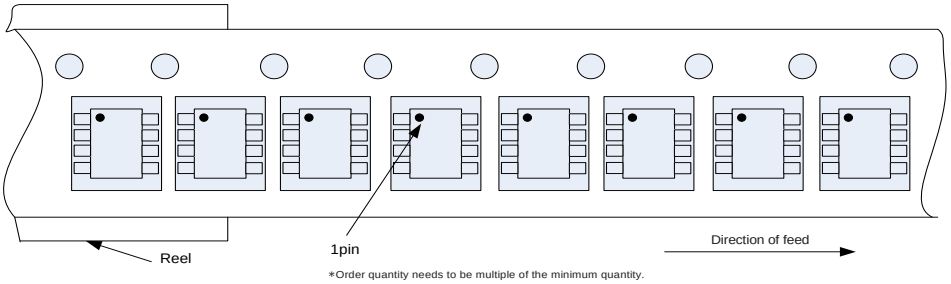






Symbol	MILLIMETER		
	MIN	NOM	MAX
A	1.30	—	1.70
A1	0.00	—	0.10
A2	1.35	—	1.55
b	0.33	—	0.51
c	0.17	—	0.25
D	4.70	—	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
D1	3.05	—	3.25
E2	2.16	—	2.36
e	1.27BSC		
L	0.40	—	1.27
θ	0 °	—	8 °

ESOP8:



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