

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW[®]7726C is a synchronous rectifier controller, used for the secondary side rectification of isolation topologies, such as Active Clamp Flyback and CCM/QR/DCM Flyback. By driving an external MOSFET, JW7726C is able to significantly improve the efficiency comparing with the conventional Diode rectifier.

When JW7726C senses V_{ds} of MOSFET less than -140mV, it turns on the MOSFET. Once the V_{ds} is greater than -3mV, JW7726C turns off the MOSFET.

JW7726C supports multiple operation modes, such as DCM, CrCM, CCM and Quasi-Resonant. By implementing the Joulwatt proprietary technology, JW7726C is able to handle CCM operation.

JW7726C is available in SOT23-6 package.

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FEATURES

- Supports Active Clamp Flyback, DCM, Quasi-Resonant, and CCM Flyback
- Support High-side and Low-side Rectification
- Output Voltage Directly Supply VCC
- Low Quiescent Current
- Fast Driver Capability for CCM Operation
- SOT23-6 Package

APPLICATIONS

- Active clamp Flyback and Flyback converters
- Adaptor
- LCD and PDP TV

TYPICAL APPLICATION

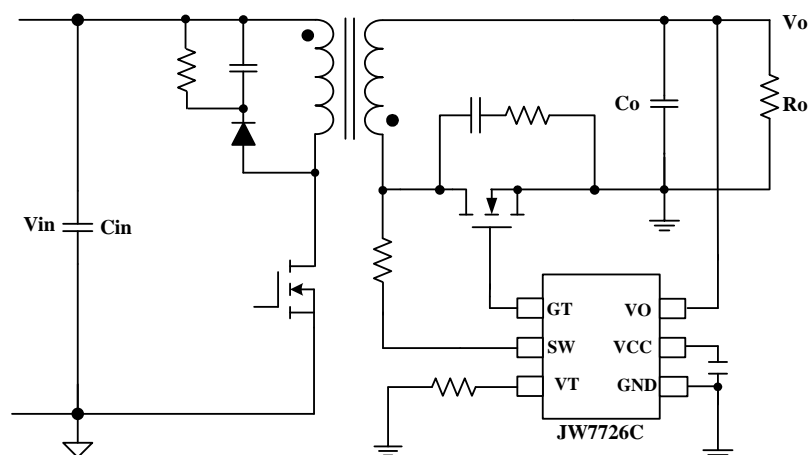


Figure A: JW7726C Typical Application for low-side.

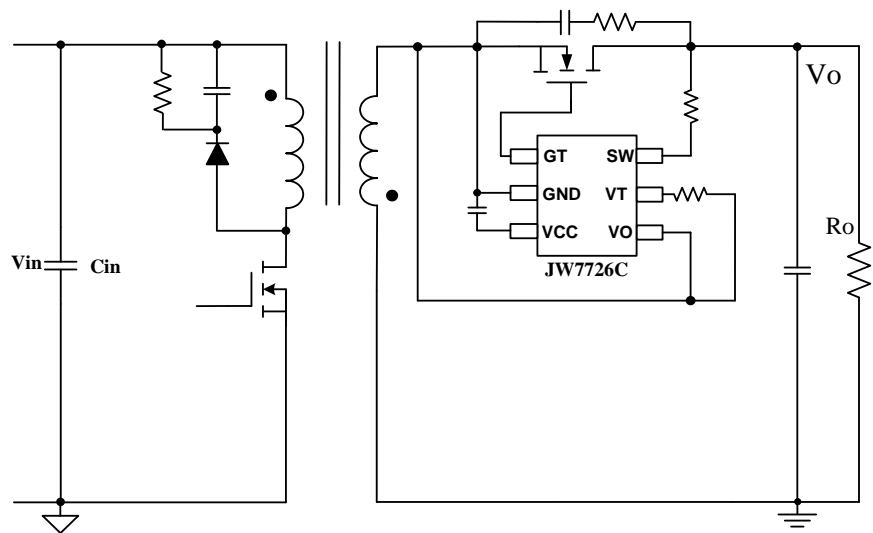
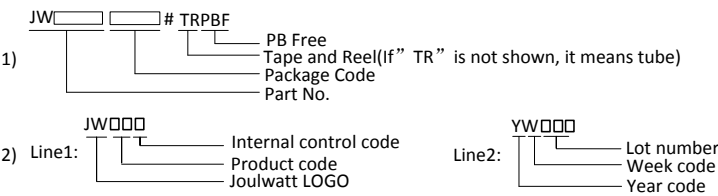


Figure B: JW7726C Typical Application for high-side.

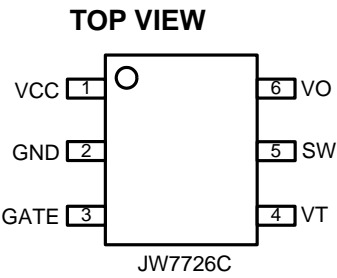
ORDER INFORMATION

DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
JW7726CSOTB#TRPBF	SOT23-6	JWFJ□ YW□□□

Notes:



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

SW PIN	-1 to 140V
VO PIN	-0.3 to 28V
VCC, GT PIN.....	-0.3 to 10V
VT PIN.....	-0.3 to 7V
Continuous Power Dissipation($T_A=+25^{\circ}\text{C}$) ²⁾ SOT23-6.....	0.6W
Junction Temperature ³⁾	150°C
Lead Temperature	260°C
Storage Temperature.....	-65°C to150°C
ESD Susceptibility (Human Body Model)	2kV

RECOMMENDED OPERATING CONDITIONS⁴⁾

SW Pin.....	4.7V to 120V
VO Pin.....	4.7V to 25V
VCC, GT PIN.....	4V to 8.5V
Operation Junction Temperature	-40°C to 125°C

THERMAL PERFORMANCE⁵⁾

θ_{JA} θ_{JC}

SOT23-6.....	200 ...130°C/W
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Note:

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$.
- 3) Continuous operation over the specified absolute maximum operating junction may damage the device.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, unless otherwise stated

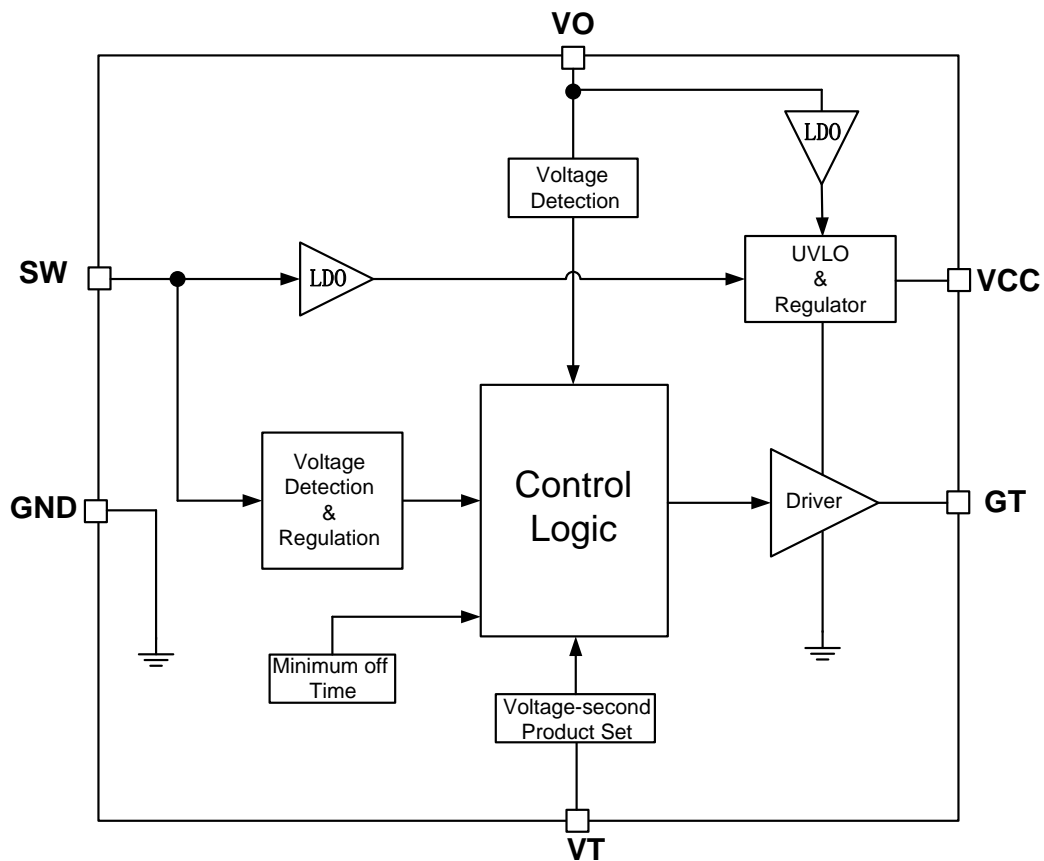
Item	Symbol	Condition	Min.	Typ.	Max.	Units
<i>VCC Section</i>						
VCC Voltage	VCC	SW=40V, VCC=2.2uF	7.5	8	8.5	V
VCC Startup voltage	V _{CC_Startup}		4.35	4.5	4.65	V
VCC UVLO	V _{CC_UVLO}		3.8	3.95	4.1	V
Operation Current (GT On)	I _{VCC}	GT=5nF, VCC=2.2uF		0.9		mA
Quiescent Current	I _q	VCC=6V, VCC=2.2uF		110		uA
<i>Gate Section</i>						
Gate Turn on Threshold	V _{MOS_ON}			-140		mV
Gate Turn off Threshold	V _{MOS_OFF}			-10		mV
Gate Turn off Threshold in MOT	V _{GTOFF_MOT}		0.95	1	1.05	V
Gate Turn on Voltage	V _{GT}	SW=32V, VCC=2.2uF	V _{CC} -1	V _{CC}		V
Maximum Gate Pull up current	I _{GU}	⁶⁾		0.6		A
Maximum Gate Pull down current	I _{GD}	⁶⁾		4		A
Gate Minimum on Time	T _{MIN_ON}			575		ns
Absolutely Minimum off Time	T _{MIN_OFF}			365		nS
Turn-on total delay	T _{DON}	C _{LOAD} =4.7nF ⁶⁾		50		nS
Turn-off total delay	T _{DOF}	C _{LOAD} =4.7nF ⁶⁾		20		nS
<i>SW and VO Section</i>						
VCC Charge Current	I _{SW_CHG}	SW=40V, VCC=6V	75	85		mA
SW Regulation Voltage	V _{MOS_REG}		-50	-40	-20	mV
SW Control Voltage MAX	V _{MOS_REG_MAX}		-185	-160	-145	mV
VO Enable Charge Voltage	V _{O_EN}	VCC=4V, SW=0V, rising	4.5	4.6	4.7	V
VO Disable Charge Voltage	V _{O_DIS}	VCC=4V, SW=0V, falling	4.4	4.5	4.6	V
VO Charge Current	I _{VO_CHG}	SW=0V, VCC=6V, VO=12V	33	40		mA

Note:⁶⁾ Guaranteed by design.

PIN DESCRIPTION

PIN	Name	Description
3	GT	Drive the External NMOSFET.
2	GND	Ground.
1	VCC	Power supply. Bypass a Capacitor Between VCC and GND.
4	VT	Set the voltage-second product.
6	VO	Output Voltage Sensing and Charging to VCC.
5	SW	External Power MOSFET Drain Voltage Sensing. Charging to VCC.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

JW7726C is a synchronous rectifier controller which combined with external MOSFET can replace the Schottky Barrier Diode. It supports all operations, such as DCM, CrCM, (Quasi-Resonant) and CCM when adopted in Active Clamp Flyback and Flyback converter.

Startup

During the startup period, when the VCC is charged up by the two internal LDOs connected to SW and VO pin respectively.

When VO is lower than 4.5V (falling), JW7726C can power itself through the internal LDO connected to SW pin during the SR turn-off period, which means primary the primary side MOSFET is turned on and SW presents a positive voltage. A capacitor between VCC and GND is required to store the energy and supply to IC during the SR turn-on period.

When VO is above 4.6V (rising), the VO pin charges VCC pin. .

Once the VCC voltage exceeds $V_{CC_Startup}$, the JW7726C exits the UVLO. If VCC is lower than V_{CC_UVLO} , the external MOSFET is turned off. The current flows though body diode before the VCC reaches to the startup voltage $V_{cc_startup}$.

Under-Voltage Lockout (UVLO)

When the VCC is below UVLO threshold, the external MOSFET is turned off and pulled low internally. Once the VCC exceeds the startup voltage $V_{cc_startup}$, the parts is activated again.

Turn On Phase

There are two conditions for the JW7726C to turn on the SR, i.e. V_{sw} , voltage-second value on SW pin when primary side switch is on, and the turn on phase is shown in Fig. 1.

1) V_{sw} : when the synchronous MOEFET is conducting, current flows through the body diode of MOSFET, which generates a negative voltage V_{SW} across it. When V_{SW} is lower than V_{MOS_ON} , the part will pull the gate high to turn on the synchronous MOSFET after turn on delay time T_{DON} if the other condition is met.

2) Volt-second of SW: in DCM and QR operation, there are parasitic oscillations. In some applications, the drain resonant voltage may fall below the SR turn on threshold, especially for the first couple rings. SR could be falsely turned on, which may cause shoot through issue and result in high power loss. The volt-second value of SW pin can be used to distinguish the parasitic ring from normal primary side switch on. The threshold can be set by the resistance at VT pin. The curve is shown in Fig. 2.

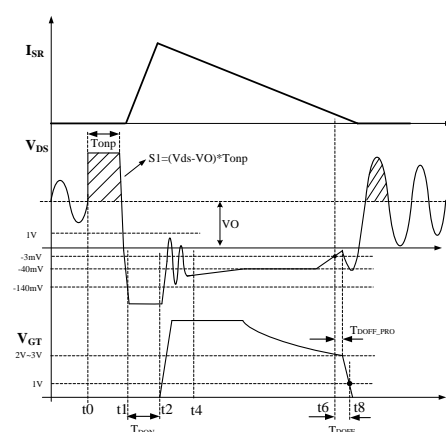


Figure-1 Turn on delay and turn off delay

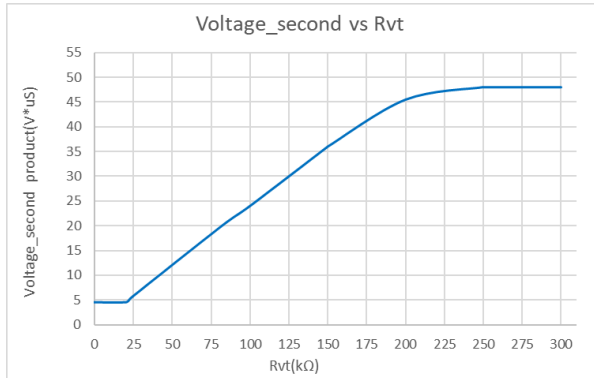


Fig. 2 Volt-second value vs. VT resistance

Minimum On Time (MOT)

When the synchronous MOSFET is turn on, there is a minimum on time for the SR. The V_{SW} voltage may have a parasitic ring when the synchronous MOSFET turns on. So, a minimum on time (MOT) is very important to avoid the MOSFET turn off threshold is false triggered. Minimum on time is 575ns for high frequency applications. During the minimum time, the gate can still be turned off if V_{SW} touches a positive threshold value, +1V.

Conducting Phase

When the synchronous MOSFET is turned on, the drain source voltage V_{SW} it is determined by its on resistance and the current through it. The part adjusts the gate voltage and regulates the V_{SW} to the internal threshold (typical -40mV) after the synchronous MOSFET turn on. When the V_{SW} is lower than -40mV, the gate keeps its maximum voltage. And the synchronous MOSFET is fully on.

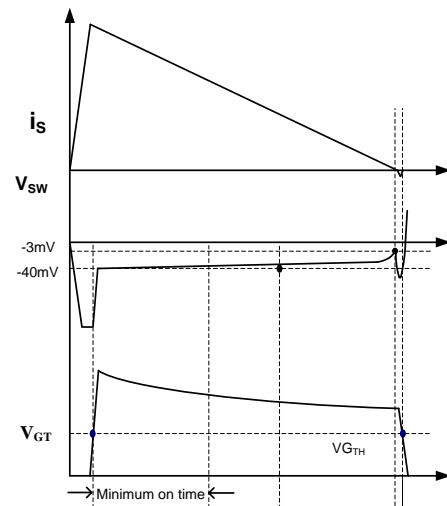


Figure. 3 Conducting phase for DCM mode

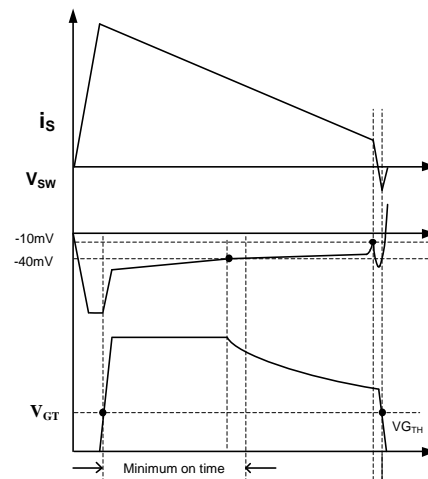


Figure. 4 Conducting phase for CCM mode

The V_{SW} rises when the current follow through the MOSFET decreases. The gate voltage will be decreased to increase its on resistance and regulate the V_{SW} around -40mV.

Figure. 3 and Figure. 4 show the theoretical waveforms when a conventional Flyback converter operated in DCM mode and CCM mode respectively.

For Active Clamp Flyback converter, the SR current is a kind of resonant current, like sinusoidal, as shown in Fig.5. The current at the beginning is small, and then it rises to its maximum value and then decreases to zero. It is similar to the LLC resonant converter. So, after the gate voltage is pulled up during the first 365ns, it will decrease to a small value because of small current, when the current increases, the gate voltage should increase too, which means the pull up current source should always be enabled during the whole SR conduction period. The pull up current can be reduced in normal operation. Due to limited regulation bandwidth, the gate voltage change may not be able to keep up with the current variation. The VSW may below -40mV regulation threshold. In this case, if the VSW reaches twice the regulation threshold (such as -80mV), the gate can be pulled up with small current source. For conventional Flyback converter, since the current always decreases, usually the pull up current source can be disabled after the firstly 365ns.

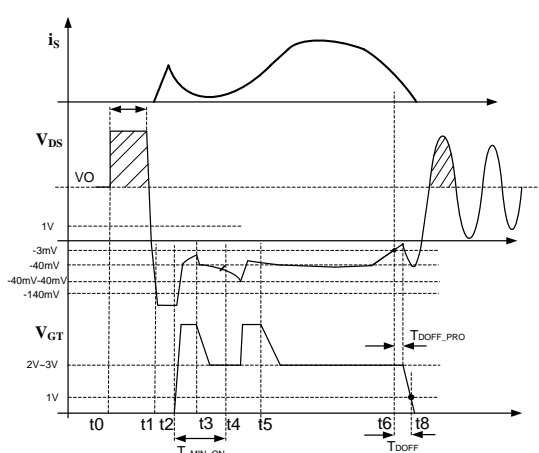


Figure.5 Conducting phase for ACF

It should be noted that the typical regulation threshold (-40mV) during MOSFET on time is not fixed, it can be internally changed to ensure the proper operation under CCM mode.

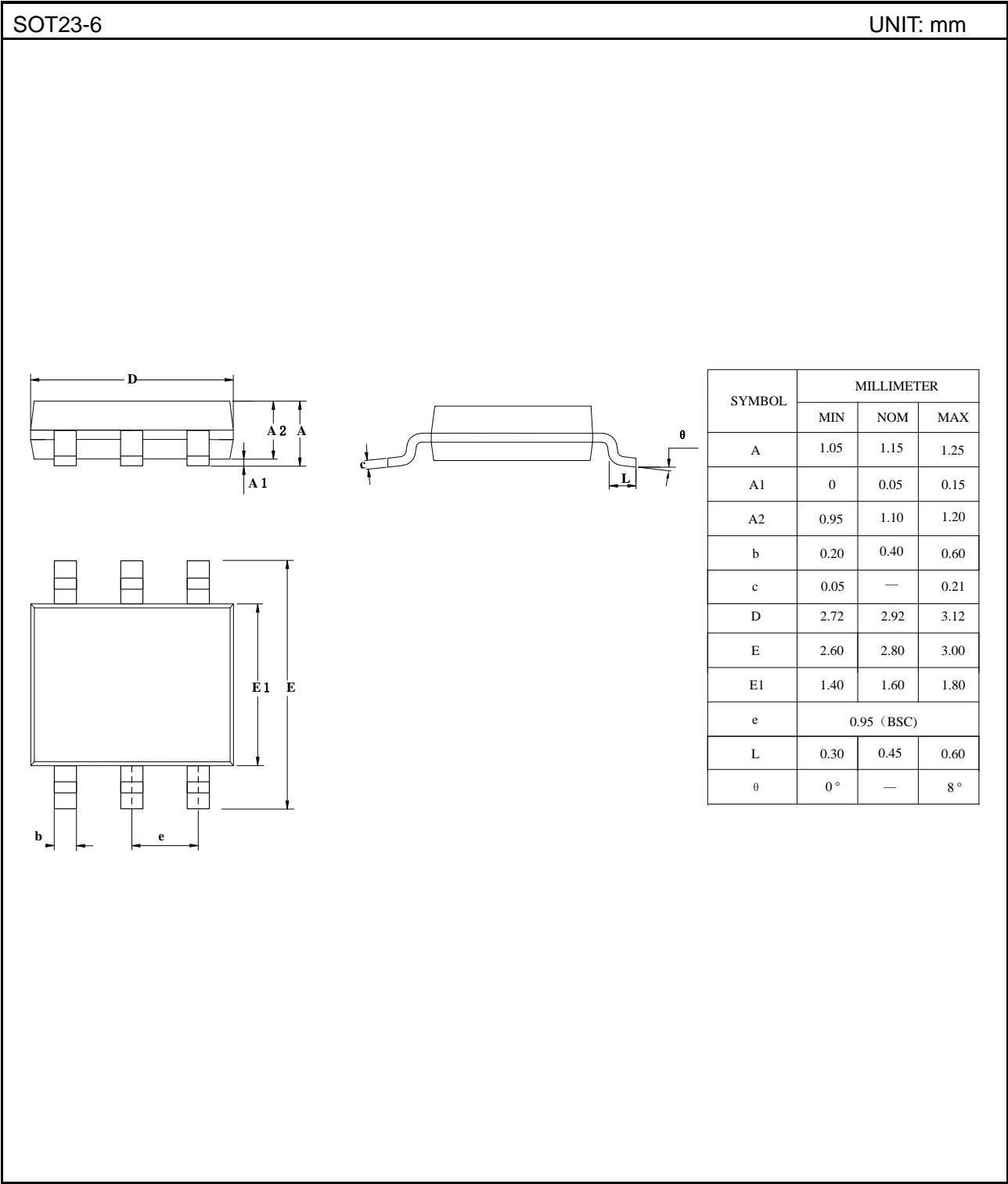
Turn Off Phase

After synchronous MOSFET conducting, once the voltage V_{SW} touches the MOSFET turn off threshold (-3mV), the gate is pulled to low after a turn off delay time T_{DOFF} . A 365nS blanking time is necessary to avoid error trigger. The blanking time is reset once V_{SW} rises above 2.5V.

Output Voltage Detection

The JW7726C has output voltage detection function via VO pin. VCC is charged from VO pin when VO is higher than 4.6V to save power loss caused by the LDO when charging from SW pin to VCC pin. When VO drops below 4.5V, the JW7726C is powered from SW pin.

PACKAGE OUTLINE



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