



# JW7951C

## 15W High Efficiency Full-Bridge Power Stage for Wireless Charger Transmitter

*Parameters Subject to Change Without Notice*

### DESCRIPTION

The JW<sup>®</sup>7951C is a high efficiency full-bridge power stage (integrated MOS plus driver) designed for wireless charger transmitter. With a transmitter controller, it can provide flexible wireless charger solutions compliant with WPC v1.2.3 Baseline Power Profile and Extended Power Profile.

The integrated low  $R_{DS(on)}$  power MOSFETs maximizes the system efficiency with better heat performance.

The JW7951C also provides input current sense function. The chip measures the input current with the current sampling resistor and reports it on the ISENSE pin, so that the total current can be read by the controller to realize the FOD (Foreign Object Detection) and in-band communication.

The JW7951C guarantees robustness with input over-current protection, thermal shutdown and under voltage lockout.

### FEATURES

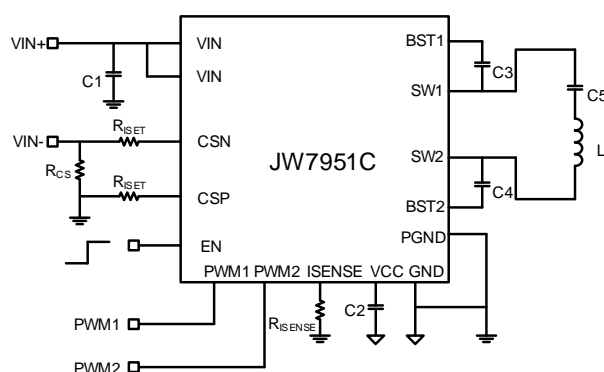
- 4.0V to 20V wide input voltage range.
- Output power: 15W
- Integrate low  $R_{DS(on)}$  switch power MOS.
- Independent two PWM control for flexible transmitter design.
- Integrate input current sense and programmable current sense ratio.
- Support all wireless charger switch frequency.
- High efficiency over full load range.
- Over-current protection
- Thermal shutdown.
- Package: QFN3x4-15 and ETSSOP20

### APPLICATIONS

- Wireless Charger Transmitter
- Motor Drivers

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### TYPICAL APPLICATION

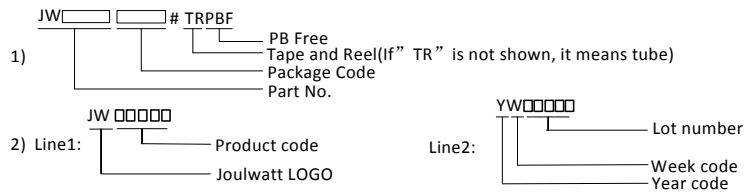


Typical application circuit

## ORDER INFORMATION

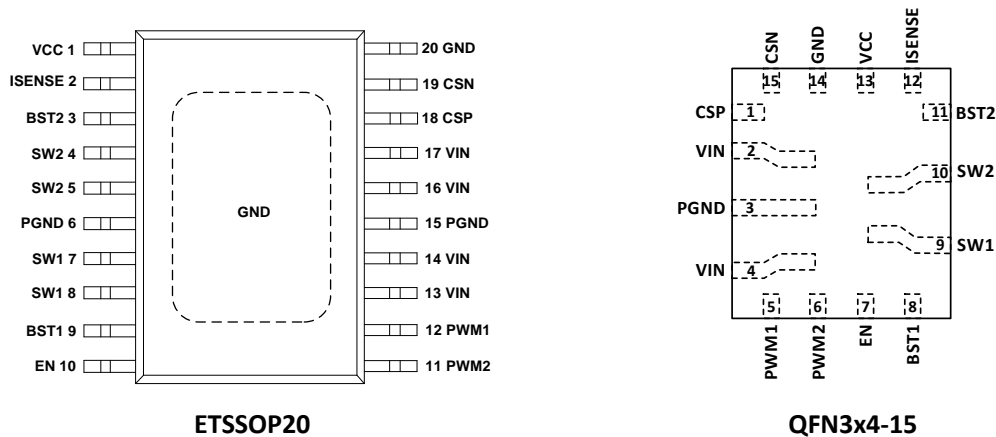
DEVICE <sup>1)</sup>	PACKAGE	TOP MARKING <sup>2)</sup>
JW7951CQFNE#TRPBF	QFN3×4-15	JW7951C YW□□□□
JW7951CETSSOP#TRPBF	ETSSOP20	JW7951C YW□□□□

## Notes:



## PIN CONFIGURATION

## TOP VIEW

ABSOLUTE MAXIMUM RATING<sup>1)</sup>

VIN, SW, EN .....	-0.3V to 29V
PWM1, PWM2.....	-0.3 to 9V
BST1-SW2, BST2-SW2 .....	-0.3V to 4V
All Other Pins .....	-0.3V to 4V
Junction Temperature <sup>2)3)</sup> .....	150°C
Lead Temperature .....	260°C
Storage Temperature .....	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

VIN .....	4.0V to 20V
PWM1, PWM2, EN .....	2.0V to 5V
Operation Junction Temp (T <sub>J</sub> ) .....	-40°C to +125°C

THERMAL PERFORMANCE<sup>4)</sup>

	$\theta_{JA}$	$\theta_{JC}$
QFN3X4-15.....	48...11°C/W	
ETSSOP20.....	34...20°C/W	

Note:

- 1) Exceeding these ratings may damage the device.
- 2) The JW7951C guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
- 3) The JW7951C includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

<i>V<sub>IN</sub>=5V, T<sub>A</sub>=25 °C, unless otherwise stated</i>						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
<b>Power Supply</b>						
V <sub>IN</sub> Voltage Range	V <sub>IN</sub>		4		20	V
V <sub>IN</sub> UVLO threshold	V <sub>IN_UVLO</sub>	V <sub>IN</sub> rising	3.55	3.7	3.85	V
		V <sub>IN</sub> falling	3.25	3.4	3.55	V
V <sub>CC</sub> output voltage	V <sub>CC</sub>	EN=3.3V 0mA load	3.1	3.3	3.4	V
		EN=3.3V 50mA load	3.0	3.2	3.35	V
V <sub>CC</sub> output current limit	I <sub>VCC</sub>	V <sub>IN</sub> =8V, V <sub>CC</sub> >2.7V		50		mA
Supply current in shut-down mode	I <sub>Q</sub>	V <sub>IN</sub> =5V, EN=0V		37	50	μA
<b>Interface</b>						
PWM1, PWM2 logic high threshold	V <sub>PWMH</sub>	Input rising			2.0	V
PWM1, PWM2 logic low threshold	V <sub>PWML</sub>	Input falling	0.8			V
EN logic high threshold	V <sub>ENH</sub>	V <sub>EN</sub> rising			2.0	V
EN logic low threshold	V <sub>ENL</sub>	V <sub>EN</sub> falling	0.8			V
<b>Current Sense</b>						
ISENSE current sense ratio	CS_gain	R <sub>CS</sub> =10mΩ, R <sub>ISET</sub> =2k, R <sub>ISENSE</sub> =10kΩ, I <sub>IN</sub> =1A,		24		uA/A
ISENSE current sense offset	CS_offset	R <sub>CS</sub> =10mΩ, R <sub>ISET</sub> =2k, R <sub>ISENSE</sub> =10kΩ, I <sub>IN</sub> =1A,	-2		2	uA
<b>Power MOS</b>						
<b>ETSSOP</b>						
Top switch on-resistance <sup>5)</sup>	R <sub>dsbkTG</sub>			40		mΩ
Bottom switch on-resistance <sup>5)</sup>	R <sub>dsbkBG</sub>			40		mΩ
<b>QFN</b>						
Top switch on-resistance <sup>5)</sup>	R <sub>dsbkTG</sub>			20		mΩ
Bottom switch on-resistance <sup>5)</sup>	R <sub>dsbkBG</sub>			20		mΩ
Switch minimum off time <sup>5)</sup>	T <sub>off_min</sub>			100		ns
Switch minimum on time <sup>5)</sup>	T <sub>on_min</sub>			100		ns
<b>Protection</b>						
Input over-current threshold <sup>5)</sup>	I <sub>OC</sub>			9		A
Thermal shutdown threshold <sup>5)</sup>	T <sub>SHUT</sub>			150		°C
Thermal recovery threshold <sup>5)</sup>	T <sub>REC</sub>			130		°C

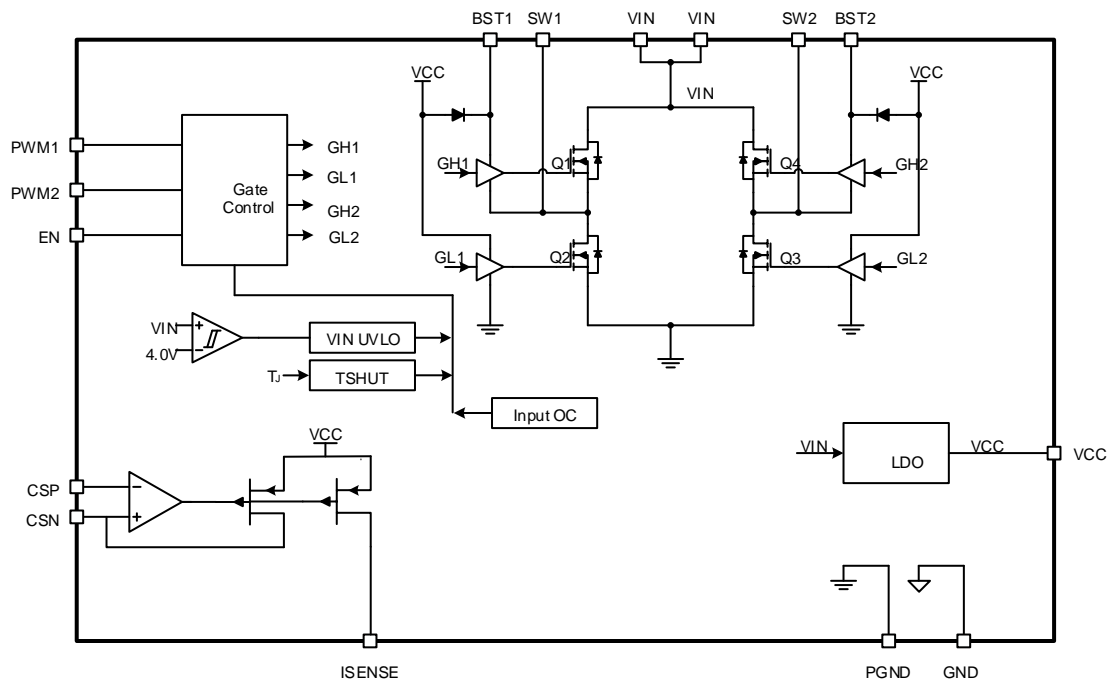
**Notes:**

5) Guaranteed by design.

## PIN DESCRIPTION

Pin No.	Name	Description
1	CSP	Positive terminal of input current sense.
2, 4	VIN	Power supply input.
3	PGND	Power Ground.
5	PWM1	PWM input for the control of the arm at SW1 side. When PWM1 is high, the top switch Q1 is turned on and the bottom switch Q2 is turned off. When PWM1 is low, the top switch Q1 is turned off and the bottom switch Q2 is turned on.
6	PWM2	PWM input for the control of the arm at SW2 side. When PWM2 is high, the top switch Q4 is turned on and the bottom switch Q3 is turned off. When PWM2 is low, the top switch Q4 is turned off and the bottom switch Q3 is turned on.
7	EN	Chip enable pin. Active High to enable the chip. When EN is low, the chip is disabled, and both SW1 and SW2 are High-Z.
8	BST1	Bootstrapped supplies to the high side floating driver of Q1. An 0.1 $\mu$ F ceramic capacitor is suggested to be connected between this pin and SW1 pin.
9	SW1	Power switching node 1.
10	SW2	Power switching node 2.
11	BST2	Bootstrapped supplies to the high side floating driver of Q4. An 0.1 $\mu$ F ceramic capacitor is suggested to be connected between this pin and SW2 pin.
12	ISENSE	Input current sense output pin. Connect a resistor from this pin to GND.
13	VCC	3.3V LDO for power driver and internal circuit. Must be bypassed to GND with a minimum of 4.7 $\mu$ F ceramic capacitor for stable operation.
14	GND	Signal GND.
15	CSN	Negative terminal of input current sense.

BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

JW7951C is a high-efficiency full-bridge power stage (integrated MOS plus driver) for wireless charger transmitter. With a transmitter controller, it can provide flexible wireless transmitter solutions, compliant with WPC v1.2.3 Baseline Power Profile and Extended Power Profile.

### Integrated Full-Bridge Stage

The JW7951C integrates a full-bridge power stage with low  $R_{DS(on)}$  N-channel MOSFETs and can work with wide input voltage ranging from 4.0V to 20V. All circuits needed to drive the full-bridge stage are integrated, such as gate drivers and bootstrap circuits. With the PWM control signals from the controller, it can be widely used in wireless transmitter applications.

### PWM Control

The JW7951C has two PWM input pins, PWM1 and PWM2. Each input signal can control one arm of the integrated full-bridge independently. The PWM1 input controls the arm of Q1 and Q2, and the PWM2 input controls the arm of Q3 and Q4.

When the input PWM signal is high, the top switch of the corresponding arm is turned on, and the bottom switch of this arm is turned off. When the input PWM signal is low, the bottom switch of the corresponding arm is turned on, and the top switch is turned off. For example, when PWM1 is high, the Q1 is turned on and Q2 is turned off. When PWM1 is low the Q1 is turned off and Q2 is turned on.

For a typical WPC transmitter, the PWM1 and PWM2 are complementary and the duty cycle is fixed in 50% with the frequency range from 100kHz to 205kHz. When the frequency reaches 205kHz, the output power can be limited furtherly by reducing the duty cycle of PWM1 and PWM2.

### Current Sense

The JW7951C provides input current sense function. The total input current is measured by the current sensing resistor and reported on ISENSE pin.

As seen in the figure 1, the current ISENSE pin outputs can be calculated by the formula below.

$$I_{ISENSE}(\mu A) = R_{CS}(m\Omega) / R_{ISET}(k\Omega) \times 5 \times I_{IN}(A)$$

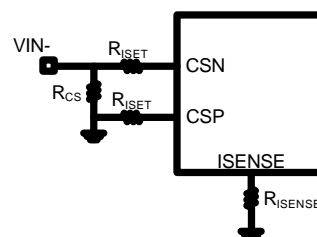


Figure 1. Current sensing configuration

Where  $R_{CS}$  and  $R_{ISET}$  are the resistors in figure 1,  $I_{IN}$  is the input current.

If the resistance from ISENSE pin to GND is  $R_{ISENSE}$ , the voltage on ISENSE pin can be achieved by the expression below.

$$V_{ISENSE}(mV) = I_{ISENSE}(\mu A) \times R_{ISENSE}(k\Omega)$$

### Protection

The JW7951C guarantees robustness with input over-current protection, thermal shutdown and under voltage lockout.

#### Input Over-Current Protection

The JW7951C measures the inductor peak current by top switches. And the over-current protection threshold is constant 9A.

When the inductor peak current exceeds the input over current threshold, the device turns off the top switches and turns on the bottom switches regardless of the status of PWM1 and PWM2 to protect the chip from damage. When the over current event happens 4 times, IC will

enter hiccup mode.

### Under-Voltage Lockout

When the input voltage falls below the  $V_{IN\_UVLO}$  falling threshold, the device stops switching. When the input voltage rises above the  $V_{IN\_UVLO}$  rising threshold, the device resumes working, if EN is still high.

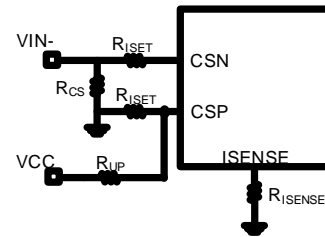
### Thermal Shutdown

When the junction temperature of the JW7951C rises above 150°C, the device enters shut down mode. When the temperature of JW7951C drops below 130°C, the JW7951C can be resumed.

### Current Sensing Offset Correction

For minimizing current sensing error, zero calibration can be made by external MCU as reference in figure 2. VIN- is the voltage of input power source negative pole. VCC is the voltage

on VCC pin of the JW7951C.



**Figure 2. Current sensing offset correction**

MCU's ADC reads  $V_{ISENSE0}$  when JW7951C works without loading. The value of  $R_{UP}$  and  $R_{ISET}$  are advised to satisfy the below expression.

$$\frac{R_{ISET}}{R_{UP} + R_{ISET}} \times VCC \geq 5mV$$



## PACKAGE OUTLINE

QFN3X4-15

UNIT: mm

TOP VIEW

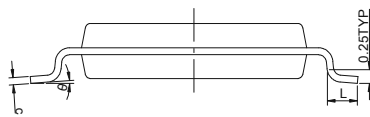
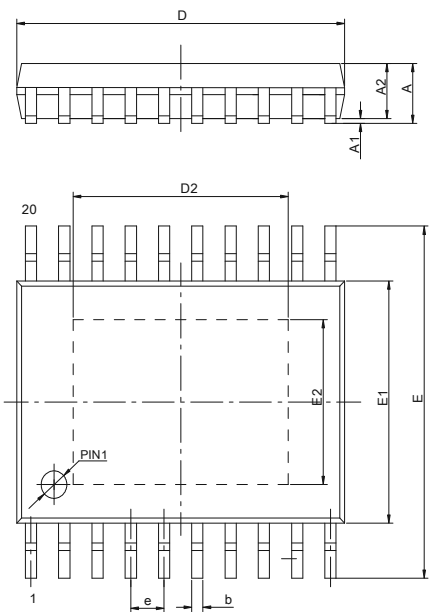
BOTTOM VIEW

SIDE VIEW

	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
c	0.15REF		
b	0.15	0.20	0.25
b1	0.09	0.14	0.19
b2	0.12	0.17	0.22
D	3.90	4.00	4.10
E	2.90	3.00	3.10
e	0.40	0.50	0.60
e1	0.90	1.00	1.10
H	0.10REF		
K	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	1.15	1.25	1.35
L2	1.12	1.22	1.32

ETSSOP-20

UNIT: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.02	—	0.15
A2	0.80	0.90	1.00
b	0.19	—	0.30
c	0.09	—	0.20
D	6.40	6.50	6.60
D2	4.10	4.20	4.30
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
E2	2.90	3.00	3.10
e	0.65(BSC)		
L	0.50	—	0.70
θ	0 °	—	8 °

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