JWH6344

High Efficiency
Synchronous Step-Down PWM Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®H6344 is a synchronous buck regulator controller. Operating with an input range of 5V~65V, the JWH6344 adopts voltage mode control and provides high efficiency, excellent transient response, and high DC output accuracy needed for low output voltage, high current, PC system power rail and similar POL power supply in digital consumer products. At light loads, the regulator operates in low frequency to maintain high efficiency.

The JWH6344 guarantees robustness with thermal protection, short-circuit protection, over current protection, output over-voltage protection, output under-voltage protection and input under voltage lockout.

The JWH6344 is available in QFN3.5X4.5-20 package, which provides a compact solution with minimal external components.

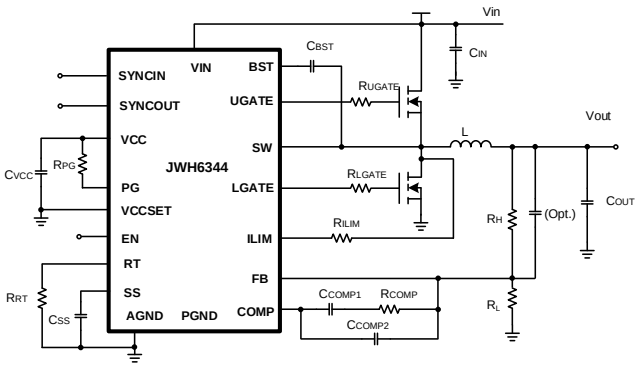
FEATURES

- 5V to 65V operating input range
- 0.8V to 65V output voltage range
- Built-in ±1% 0.8V reference voltage
- Switching frequency from 100kHz to 1MHz
  -SYNC In and SYNC Out capability
- 7.5V gate drivers for standard VTH MOSFETs
  -14ns dead time
  -2.3A source and 3.5A sink capability
  -Low-side soft-start for pre-bias start-up
- Programmable current limit by low side $R_{DS(ON)}$ sensing or shunt sensing
- Adjustable soft-start or optional voltage tracking
- Built-in OCP/UVP
- Power good indicator
- Thermal protection
- Available in QFN3.5X4.5-20 package

APPLICATIONS

- Networking and Computing Power
- Industrial Motor Drives

TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JWH6344QFNAC#TRPBF	QFN3.5X4.5-20	JWH6344 YW□□□□□

Notes:

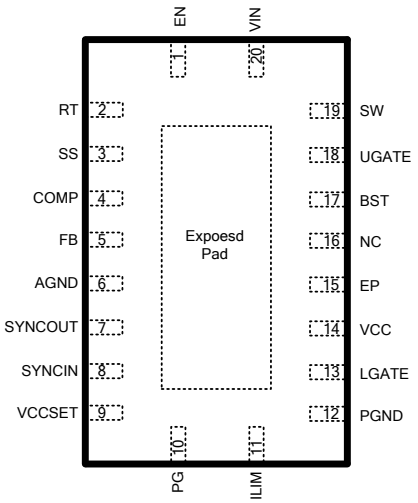
1) JW□□□# TRPBF
- PB Free
- Tape and Reel(If" TR" is not shown, it means tube)
- Package Code
- Part No.

2) Line1: JW□□□□□
- Product code
- Joulwatt LOGO

Line2: YW□□□□□
- Lot number
- Week code
- Year code

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, ILIM Pins ..... -0.3V to 80V
SW Pin ..... -0.3V(-5V for 20ns) to 80V
BST Pin ..... SW-0.3V to SW+14V
VCC, PG, SYNCIN, VCCSET Pins ..... -0.3V to 14V
FB, COMP, SS, RT Pins ..... -0.3V to 6V
UGATE to SW Pin ..... -0.3V to 14V
LGATE to GND Pin ..... -0.3V to 14V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN without External VCC .....6V to 65V
Input Voltage VIN with External VCC .....5V to 65V
External VCC .....8V to 13V
Output Voltage Vout.....0.8V to Dmax x VIN V
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
QFN3.5X4.5-20	37	2.1ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH6344 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{EN}=1.5V, R_{RT}=25kΩ, T_J = -40ºC~125ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
Shutdown Current	I_{SD}	V_{EN}=0V, V_{VCC}<1V，TA=25℃		10	15	μA
Standby Input Current	I_{Q_STBY}	V_{EN}=1V		600	800	uA
Operating Input Current, Not Switching	I_{Q_RUN}	V_{EN}=1.5V, V_{SS}=0V		600	800	uA
V_{CC} Under-voltage Lockout Threshold	V_{VCC_MIN}	V_{VCC} rising	4.8	5	5.2	V
V_{CC} Under-voltage Lockout Hysteresis	$V_{VCC\_MIN\_HYST}$	V_{VCC} falling		370		mV
V_{CC} Regulation Voltage	V_{VCC}	V_{SS}=0V, 9V≤V_{IN}≤65V, 0mA≤I_{VCC}≤20mA, V_{VGSET}=GND or floating	7.3	7.5	7.7	V
		V_{SS}=0V, 12V≤V_{IN}≤65V, 0mA≤I_{VCC}≤20mA, V_{VGSET}≥5V	9.7	10	10.3	V
VIN to VCC dropout voltage	V_{VCC_LDO}	V_{IN}=6V, V_{SS}=0V , I_{VCC}=20mA		0.35	0.63	V
VCC Short-circuit Current Limit	I_{SC_LDO}	V_{SS}=0V , V_{VCC}=0V,	40	60	90	mA
Minimum External Bias Supply Voltage	V_{VCC_EXT}	Voltage required to disable VCC regulator, V_{VGSET}=GND or floating	8			V
External VCC Input Current, Not Switching	I_{VCC}	V_{SS}=0V , V_{VCC}=13V,			2.1	mA
Feedback Voltage	V_{FB}		792	800	808	mV
FB Input Bias Current	I_{FB}	V_{FB}=0.8V	-0.1		0.1	μA
COMP Output High Voltage	V_{COMP_HO}	V_{FB}=0V, COMP souring 1mA		5		V
COMP Output Low Voltage	V_{COMP_LO}	COMP sinking 1mA		0.5		V
Error Amplifier DC Gain	Gain			110		dB
Enable Shutdown to Standby Threshold	V_{SDN}	V_{EN} rising		0.4		V
Enable Shutdown Threshold	V_{SDN_HYS}	V_{EN} falling		50		mV
Enable Standby to Operating Threshold	V_{EN}	V_{EN} rising	1.164	1.2	1.236	V

Enable Standby to Operating Hysteresis Current		V_{EN} =1.5V	9	10	11	μA
Minimum Controllable On Time	T_{ON_MIN}	V_{BST}-V_{SW}=7V, UGATE 50% to 50%		40	60	ns
Minimum Off Time	T_{OFF_MIN}	V_{BST}-V_{SW}=7V, UGATE 50% to 50%		140	200	ns
Maximum Duty cycle	D_{MAX}	Fsw=100kHz, 6V≤V_{IN}≤65V	98%	99%		
		Fsw=400kHz, 6V≤V_{IN}≤65V	89%	93%		
Ramp valley voltage (COMP at 0% duty cycle)	V_{RAMP_MIN}			500		mV
PWM Feed-forward Gain	k_{FF}	6V≤V_{IN}≤65V,		15		V/V
Internal Boot Strap Switch On resistance	R_{BST}				6	Ω
BST to SW Quiescent Current, Not Switching	I_{Q_BST}	V_{SS}=0V, V_{BST}=54V, V_{SW}=48V		35		μA
BST to SW Under-voltage Detection	V_{BST_UV}	V_{BST}-V_{SW} Falling		3.6		V
BST to SW Under-voltage Hysteresis	V_{BST_HYS}	V_{BST}-V_{SW} Rising		0.4		V
ILIM Source Current	I_{RS}	R_{SENSE} Mode	90	100	110	μA
	I_{RDSON}	R_{DSON} Mode	180	200	220	μA
ILIM Source Current TC	I_{RSTC}	R_{SENSE} Mode		0		ppm/ ºC
	$I_{RDSONTC}$	R_{DSON} Mode		4500		ppm/ ºC
ILIM comparator threshold at ILIM	V_{ILIM_TH}		-8	-2	3.5	mV
SCP Clamp Offset Voltage	V_{CLAMP_OS}	Clamp to COMP steady state offset voltage	0.2+ V_{IN}/75			V
Minimum Clamp Voltage	V_{CLAMP_MIN}	Clamp voltage with continuous current limiting	0.3+V_{IN}/150			V
Hiccup Mode Activation Delay	C_{HICC_DEL}			128		cycles
Hiccup Mode Off-time After Activation	C_{HICCUP}			8192		cycles
Zero-cross Detect Disable Threshold (CCM)	V_{ZCD_DIS}	ZCD threshold measured at SW pin 1000 clock after first UGATE pulse		200		mV
Zero-cross Detect Soft-start Ramp	V_{ZCD_SS}	ZCD threshold measured at SW pin 50 clock after first UGATE pulse		0		mV

Diode Emulation Zero-cross Threshold	$V_{DE,\_TH}$	Measured at SW with V_{SW} rising	-5	0	5	mV
SS Charge Current	I_{SS}	V_{SS}=0V	8.5	10	12	μA
SS Discharge FET Resistance	R_{SS_DIS}	V_{EN}= 0.8V, V_{SS}=0.1V		11		Ω
SS to FB Offset	V_{SS_FB}		-15		15	mV
SS Clamp Voltage	V_{SS_CLAMP}	V_{SS} - V_{FB}, V_{FB} = 0.8V		2		V
UGATE Drive Source	R_{UGATE_SR}	V_{BST}-V_{SW}=7V, I_{UGATE}=-100mA		1.5		Ω
UGATE Drive Sink	R_{UGATE_SK}	V_{BST}-V_{SW}=7V, I_{UGATE}=100mA		0.9		Ω
LGATE Drive Source	R_{LGATE_SR}	V_{VCC}=7V, I_{LGATE}=-100mA		1.5		Ω
LGATE Drive Sink	R_{LGATE_SK}	V_{VCC}=7V, I_{LGATE}=100mA		0.9		Ω
Dead Time	T_D	V_{BST}-V_{SW}=7V, LGATE off to UGATE on, 50% to 50%		14		ns
		V_{BST}-V_{SW}=7V, UGATE off to LGATE on, 50% to 50%		20		ns
UGATE, LGATE Rising Times	T_{TR}	V_{BST}-V_{SW}=7V, C_{LOAD}=1nF, 20% to 80%		7		ns
UGATE, LGATE Falling Times	T_{TF}	V_{BST}-V_{SW}=7V, C_{LOAD}=1nF, 80% to 20%		4		ns
Power Good Lower Threshold	PG_{LTH}	FB falling, hysteresis=2%	90%	92%	94%	
Power Good Upper Threshold	PG_{UTH}	FB rising, hysteresis=3%	106%	108%	110%	
Power Good Delay	PG_{DLY}	PG from low to high or low to high		25		us
Power Good Sink Current	I_{PG}	V_{FB}=0.9V, V_{PG}=0.4V	6			mA
Oscillator Frequency	F_{SW}	R_{RT}=100k		100		kHz
		R_{RT}=25k	380	400	420	kHz
		R_{RT}=12.5k		780		kHz
SYNCIN External Clock Frequency Range	F_{SYNC}	% of nominal frequency set by R_{RT}	-50%		50%	
Minimum SYNCIN Input Logic High	V_{SYNC_IH}		3			V
Minimum SYNCIN Input Logic Low	V_{SYNC_IL}				0.5	V
SYNCIN Input Resistance	R_{SYNCIN}	V_{SYNCIN}=3V		20		kΩ
SYNCIN Input Minimum Pulse Width	T_{SYNCIN_PW}	Minimum high state	50			ns
SYNCOUT High-state Output Voltage	$V_{SYNCOUT\_H}$	$I_{SYNCOUT}$=-1mA (souring)	3			V

SYNCOUT Low-state Output Voltage	$V_{SYNCOUT\_L}$	$I_{SYNCOUT}$=1mA (sinking)			0.4	V
Delay from UGATE Rising to SYNCOUT Leading Edge	$T_{SYNCOUT}$	V_{SYNCIN}=0V, T_S=1/F_{SW}, F_{SW} set by R_{RT}		T_S/2-130-		ns
Delay from SYNCIN Leading Edge to UGATE Rising	T_{SYNCIN}	50% to 50%		220		ns
VCCSET Logic High Input Voltage	V_{VCCSET_H}		5			V
VCCSET Logic Low Input Voltage	V_{VCCSET_L}				0.8	V
Thermal Shutdown[5)]	T_{TSD}	T_J rising		175		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYS}			20		°C

Note：

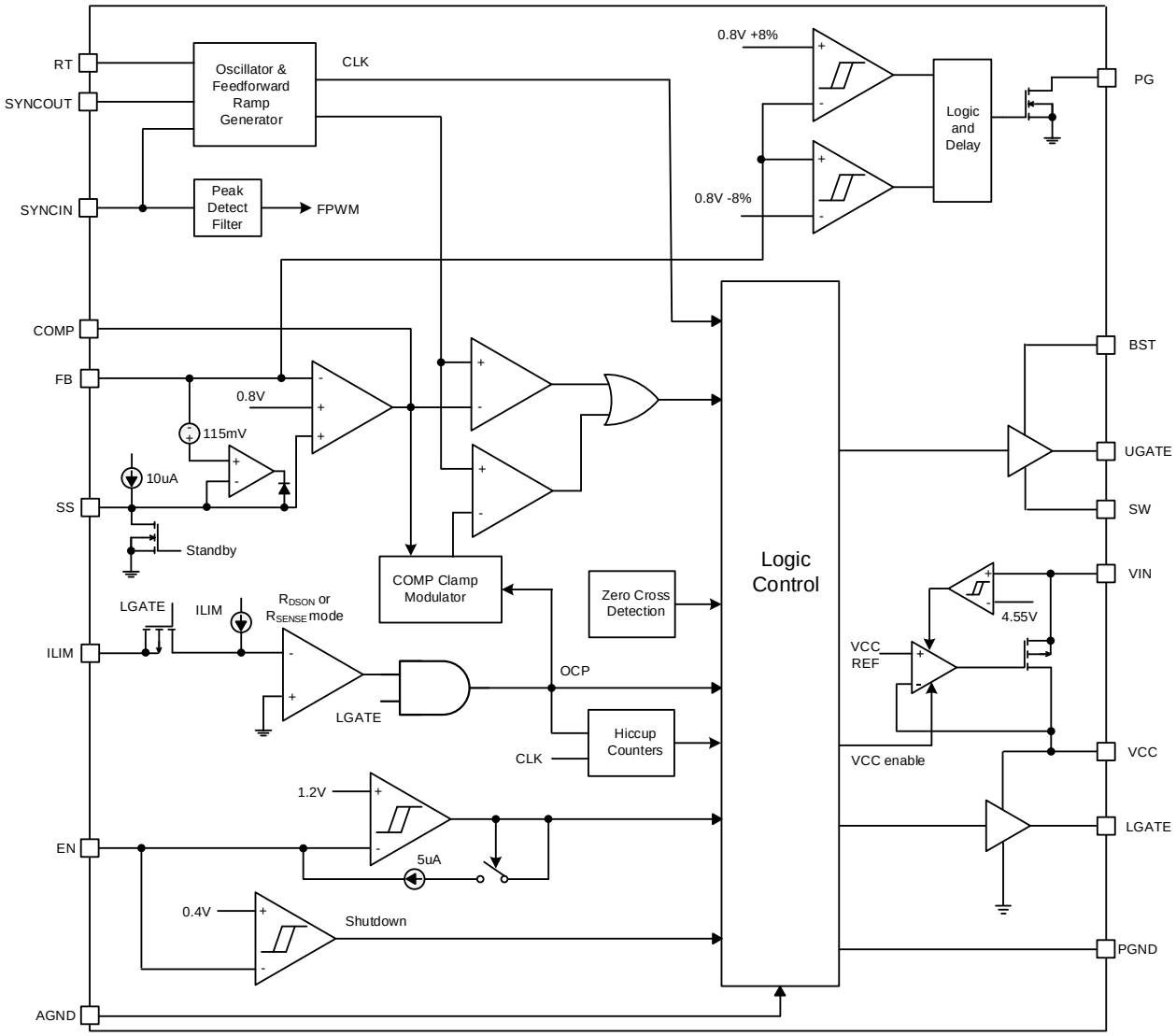
5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	EN	Enable input pin. If the EN voltage is lower than 0.4V, the device entry shutdown mode with all function disabled; if the EN voltage is higher than 0.4V and lower than 1.2V, the regulator is in standby mode which the VCC regulator operational, the SS pin grounded and no switching at the UGATE/LGATE outputs; if the EN voltage is higher than 1.2V, the device entry normal operation mode. Once the EN voltage rises above the 1.2V threshold, a 10uA current source is enabled and flows through the external UVLO resistor divider to generate a hysteresis. The hysteresis at EN pin can be adjusted by the resistance of the external divider.
2	RT	Oscillator frequency program input. Connect a resistor from this pin to AGND to program the internal oscillator frequency. An RT resistor is required even when using the SYNCIN pin to synchronize to an external clock.
3	SS	External soft-start pin. A minimum capacitance from SS to AGND of 2.2nF is required.
4	COMP	Low impedance output if the internal error amplifier. The loop compensation network should be connected between COMP pin and FB pin.
5	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 800mV. Connect a resistive divider at FB pin.
6	AGND	Analog ground.
7	SYNCOUT	Synchronization output.
8	SYNCIN	Synchronization input.
9	VCCSET	VCC regulation voltage setting pin. Pull the VCCSET pin higher than 3V, the VCC regulation voltage is 10V; Pull the VCCSET pin to ground or leave this pin floating, the VCC regulation voltage is 7.5V.
10	PG	Open drain output for power-good indicator. Usea10kΩ to 100kΩ pull-up resistor to logic rail or other DC voltage no higher than 13V.
11	ILIM	Current limit adjust and current sense comparator input. An external resistor connected to the ILIM pin is used to program the valley current limit and the opposite end of the resistor can be connected to either the drain of the low-side MOSFET for RDS(on) sensing or to a current sense resistor connected to the source of the low-side FET.
12	PGND	Power ground.
13	LGATE	Gate drive output for low side external MOSFET. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.
14	VCC	Output of the internal regulator output. Bypass to GND with a minimum 1uF ceramic capacitor.
15	EP	Pin internally connected to exposed pad of the package.
16	NC	No connection.
17	BST	Bootstrap pin for top switch. Connect through a capacitor to SW pin.

18	UGATE	Gate drive output for high side external MOSFET. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.
19	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
20	VIN	Supply voltage for the internal VCC regulator.
Exposed-pad		Exposed pad of the package. The exposed pad is recommended to be soldered to a large PCB and connected to GND for maximum power dissipation.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The JWH6344 is a synchronous step-down PWM controller. It adopts voltage mode control and regulates input voltages from 5V to 65V down to an output voltage as low as 0.8V.

Voltage-Mode Control

The JWH6344 utilizes a voltage-mode control with input voltage feed-forward to eliminate the input voltage dependence of the PWM modulator. A ramp is generated internally for the PWM modulation and the ramp voltage amplitude increases with input voltage increases to maintain constant modulator gain. The ramp is initialed at the falling edge of the internal clock and the high-side MOSFET is turned on at the same time. The output voltage is measured at the FB pin through a resistive voltage divider. The FB voltage is compared to the internal 0.8V reference voltage and the error is amplified by internal transconductance error amplifier. The output of the error amplifier (COMP) is compared with the ramp and once the ramp voltage rises above the COMP voltage, the high-side MOSFET is turned-off and the low-side MOSFET turns on until the falling edge of the clock comes.

PFM Mode

With SYNCIN pin pulled down to low, the JWH6344 operates in PFM mode at light load. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

FCC Mode

When the SYNCIN pin is tied high, the controller keeps continuous conduction mode in light load condition. In this mode, switch frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

Shut-Down Mode

The JWH6344 shuts down when voltage at EN pin is below 0.4V. The entire controller is off and the supply current consumed by the JWH6344 drops below 15uA.

Standby Mode

When voltage at EN pin rises above 0.4V and is below the precision enable threshold 1.2V(typ.), the JWH6344 enters standby mode. In the standby mode, the internal bias supply LDO is on and regulating but the switching action and output voltage regulation are disabled.

Active Mode

When voltage at EN pin rises above the precision enable threshold 1.2V(typ.) and the VCC voltage is above its rising UVLO threshold of 5V, the JWH6344 enters active mode. In active mode, all the functions are enabled.

Precision Enable and Adjustable UVLO Protection

The JWH6344 support adjustable input under-voltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements and a resistive divider connected between VIN and ground with the central tap

connected to EN can be used to adjust the input voltage UVLO. (Shown in Figure 1). Once the EN pin voltage exceeds 1.2 V, an additional 10μA of hysteresis is added. This additional current facilitates input voltage hysteresis. Use Equation 1 and Equation 2 to set the input startup voltage and external hysteresis for the input voltage.

$$R_{EN\_H} = \frac{V_{STR} - V_{STOP}}{I_{HYS}}$$

$$R_{EN\_L} = R_{EN\_H} \times \frac{V_{EN}}{V_{STR} - V_{EN}}$$

where R1 and R2 are in Ω, i_{HYS}=10uA, V_{EN} =1.2V

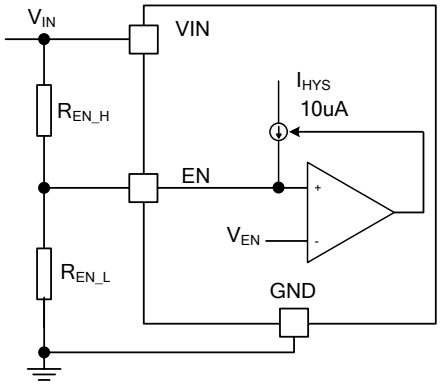


Figure 1. UVLO Setting

VCC Regulator

JWH6344 has an internal high-voltage VCC regulator that provides the power supply for the PWM controller and its gate driver for the external MOSFETs. The output of the VCC regulator can be set by the VCCSET pin. If the VCCSET pin pulled low or floating, the output of the VCC regulator is 7.5V in typical; and if the VCCSET pin pulled high, the output of VCC regulator is 10V in typical. When the input voltage drops below the VCC set-point level, the VCC output tracks VIN with a small voltage drop. Connect a ceramic decoupling capacitor between 1 μF and 5 μF from VCC to AGND for stability.

The VCC regulator has a current limit of 40mA (minimum) and under-voltage lockout protection. When the VCC voltage exceeds its rising UVLO threshold of 4.93 V, the output is enabled (if EN/UVLO is above 1.2 V) and the soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of 4.67 V (typical) or if EN/UVLO goes to a standby or shutdown state.

Internal power dissipation of the VCC regulator can be minimized by connecting the output voltage or an auxiliary bias supply rail (up to 13 V) to VCC using a diode D_{VCC}. A diode in series with the input prevents reverse current flow from VCC to VIN if the input voltage falls below the external VCC rail.

MOSFET Gate Driver

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 7.5V (or 10V) of bias voltage is delivered from VCC supply. The average drive current is also equal to the gate charge at V_{GS}=7.5V (or 10V) times switching frequency. The instantaneous drive current is supplied by the bootstrap capacitor between BST and SW pins. The drive capability is represented by its internal resistance, which are 1.5Ω for BST to UGATE and 0.9Ω for UGATE to SW.

The low-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The drive capability is represented by its internal resistance, which are 1.5Ω for VCC to LGATE and 0.9Ω for LGATE to GND. 7.5V (or 10V) bias voltage is delivered from VCC supply. The instantaneous drive current is supplied by an input capacitor connected between VCC and GND. The average drive current is equal to the

gate charge at V_{GS}=7.5V (or 10V) times switching frequency. This gate drive current as well as the high-side gate drive current times 7.5V (or 10V) makes the driving power which need to be dissipated from JWH6344 package. An adaptive dead time is designed to present shoot through between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

External Soft-start

Soft-start is designed in JWH6344 to prevent the converter output voltage from overshooting during startup and short-circuit recovery and the soft-start time can be adjusted by a capacitor connected between SS pin and AGND. When the chip starts, a 10uA current source charges the SS capacitor and the soft-start time can be calculated by the Equation 3.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}}$$

where C_{SS} is the SS capacitance between SS pin and AGND;
V_{REF} is the 0.8V internal reference voltage;
I_{SS} is the 10uA current sourced from SS pin.
When an overload event or short circuit event happens, the SS pin is internally clamped to V_{FB} +115mV to allow a soft-start recovery and the clamp circuit requires a soft-start capacitance greater than 2nF for stability.

Current Sense and Over-Current Protection

JWH6344 has a cycle-by-cycle overcurrent limiting control. A valley current limit is designed in the JWH6344 so that only when output current drops below the valley current limit can the high-side MOSFET be turned on. To provide both good accuracy and cost effective solution, the JWH6344 supports temperature compensated MOSFET $R_{DS(ON)}$ sensing mode and shunt resistor sensing mode, and it detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly. Figure 2 portrays the $R_{DS(ON)}$ sensing mode which resistor R_{ILIM} is tied to SW to use the R_{DSON} of the low-side MOSFET as a sensing element (termed R_{DSON} mode) and Figure 3 shows the shunt resistor sensing mode which R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET (termed R_{SENSE} mode).

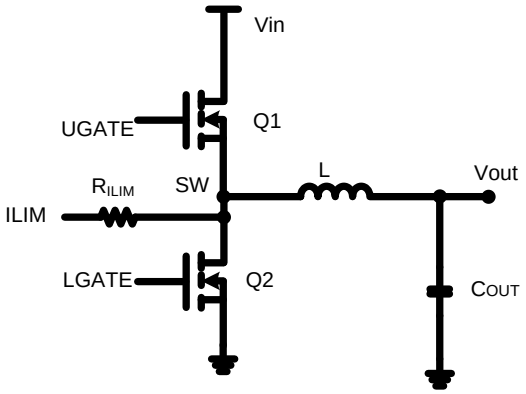


Figure 2

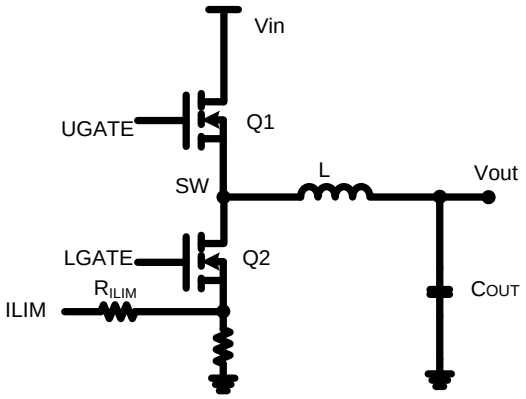


Figure 3

The ILIM pin of the JWH6344 sources a reference current that flows in an external resistor, designated R_{ILIM}, to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW

pulses if the ILIM pin voltage goes below GND. The ILIM current with R_{DSON} sensing is 200 µA at 25°C junction temperature and incorporates a TC of +4500 ppm/°C to generally track the R_{DSON} temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100 µA in R_{SENSE} mode. This controls the valley of the inductor current during a steady state overload at the output. Depending on the chosen mode, select the resistance of R_{ILIM} using Equation 4.

$$R_{ILIM} = \frac{I_{OUT} - \Delta I_L / 2}{I_{RDSON}} \times R_{DSON} \quad (R_{DSON} \text{ mode})$$

$$R_{ILIM} = \frac{I_{OUT} - \Delta I_L / 2}{I_{RS}} \times R_S \quad (R_{SENSE} \text{ mode})$$

where

R_{DSON} is the on-resistance of low-side MOSFET;

ΔI_L is the peak-to peak inductor ripple current;

I_{RDSON} is the ILIM pin current in R_{DSON} mode;

R_S is the resistance of current sensing shunt element;

I_{RS} is the ILIM pin current in R_{SENSE} mode.

In addition to valley current limiting, the JWH6344 uses a proprietary duty-cycle limiter circuit to reduce the PWM on-time during an overcurrent condition. As shown in Figure 4, an auxiliary PWM comparator along with a modulated CLAMP voltage limits how quickly the on-time increases in response to a large step in the COMP voltage that typically occurs with a voltage-mode control loop architecture. As depicted in Figure 4, the CLAMP voltage, VCLAMP, is normally regulated above the COMP voltage to provide adequate headroom during a response to a load-on transient. If the COMP voltage rises quickly during an overloaded or shorted output condition, the on-time pulse terminates thereby limiting the on-time and peak inductor current. Moreover, the CLAMP voltage is reduced if additional valley current limit events occur, further reducing the average output current.

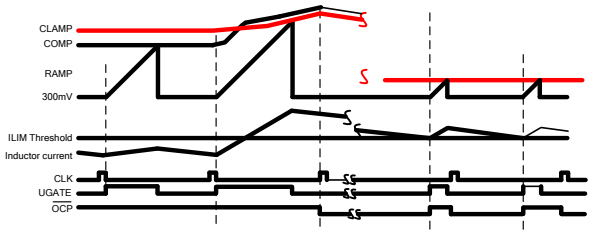


Figure 4

If the overcurrent condition exists for 128 continuous clock cycles, a hiccup event is triggered and SS is pulled low for 8192 clock cycles before a soft-start sequence is initiated.

Power Good

The JWH6344 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to a voltage source (such as Vout) through a resistor (10kΩ to 100kΩ). When the FB voltage exceeds 94% of the internal reference V_{REF}, internal comparators detect power good state and the power good signal becomes high with 25us deglitch delay time. If the feedback voltage goes under 92% of the target value, the power good signal becomes low with 25us deglitch delay time. Similarly, when the FB voltage exceeds 108% of the internal reference V_{REF}, the power good signal becomes low with 25us deglitch delay time. If the FB voltage subsequently falls below 105% of V_{REF}, the power good signal becomes high.

Switching Frequency

The switching frequency can be adjusted by the resistor connected between RT pin and AGND, or synchronizing the JWH6344 to an external clock signal through the SYNCIN pin.

The switching frequency range adjusted by the RT resistor is from 100 kHz to 1MHz, and the RT resistance can calculated by the Equation 5.

$$R_{RT}(k\Omega) = \frac{10^4}{f_{SW}(kHz)}$$

Clock Synchronization

The switching frequency in CCM state of JWH6344 can be synchronized to an external clock and the requirements for the external clock SNYC signal are:

Clock range: 100kHz to 1MHz

Clock frequency range: -50% to +50% of the free-running frequency set by R_{RT}

Clock maximum voltage amplitude: 13V

Clock minimum pulse width: 50ns

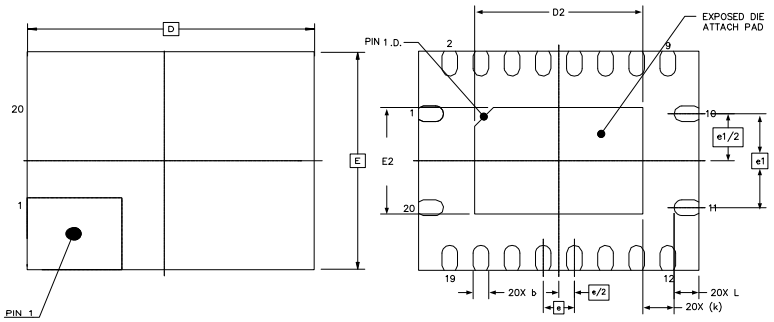
Thermal Protection

When the junction temperature of the JWH6344 rises above 175°C, it is forced into thermal shut-down which both the high-side and low-side MOSFETs are turned off and the SS and PG are pulled low.

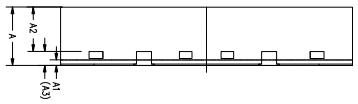
Only when the junction temperature drops below 155°C can the device restart again.

PACKAGE OUTLINE

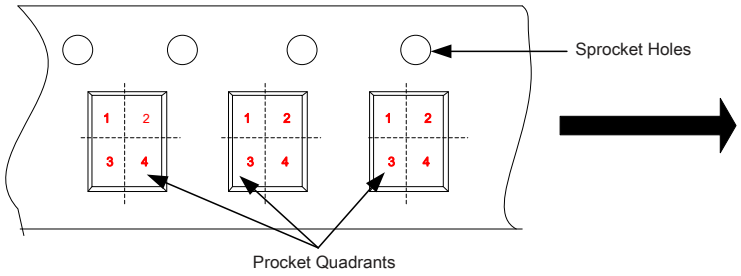
QFN3.5X4.5-20 UNIT: mm



SYMBOL	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	---	0.65	---
A3		0.203 REF	
b	0.2	0.25	0.3
D		4.5 BSC	
E		3.5 BSC	
e		0.5 BSC	
e1		1.5 BSC	
D2	2.6	2.7	2.8
E2	1.6	1.7	1.8
L	0.3	0.4	0.5
K		0.5 REF	



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN3.5X4.5-20	1

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