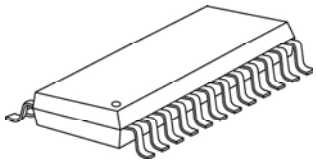
16-Channel Constant Current LED Sink Driver

Features

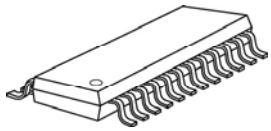
- 16 constant-current output channels
- Constant output current invariant to load voltage change:
  Constant output current range:
  3-45mA@V_{DD}=5V;
  3-30mA@V_{DD}=3.3V
- Excellent output current accuracy
  between channels: ±1.5% (typ.) and ±2.5% (max.)
  between ICs: ±1.5% (typ.) and ±3% (max.)
- Output current adjusted through an external resistor
- Fast response of output current, $\overline{OE}$ (min.): 70ns with good uniformity between output channels
- 25MHz clock frequency
- Schmitt trigger input
- 3.3V/ 5V supply voltage
- Package MSL Level : 3
- RoHS compliant package

Small Outline Package



GF: SOP24L-300-1.00

Shrink SOP



GP: SSOP24L-150-0.64

Product Description

With PrecisionDrive™ technology, JXI5020 is designed for LED displays which require to operate at low current and to match the luminous intensity of each channel. It provides supply voltage and accepts CMOS logic input at 3.3V and 5.0V to meet the trend of low power consumption. JXI5020 contains a serial buffer and data latches which convert serial input data into parallel output format. At JXI5020 output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations.

JXI5020 provides users with great flexibility and device performance while using JXI5020 in their system design for LED display applications, e.g. LED panels. It accepts an input voltage range from 3V to 5.5V and maintains a constant current up from 3mA to 45mA determined by an external resistor, R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. JXI5020 guarantees to endure maximum 17V at the output port. The high clock frequency, 25 MHz, also satisfies the system requirements of high volume data transmission.

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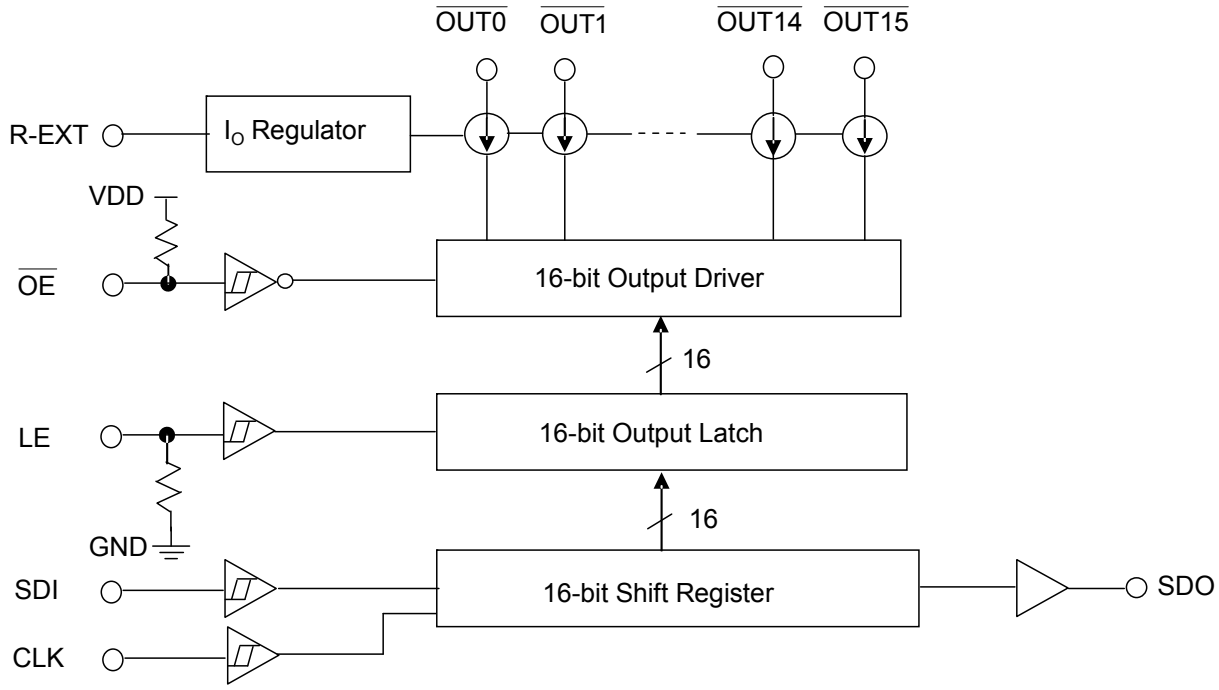
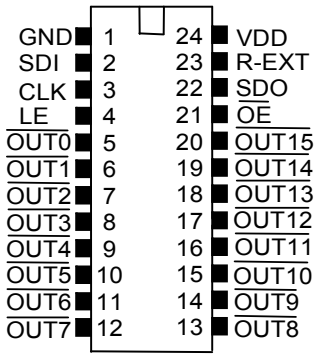
Block Diagram



Terminal Description

Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
CLK	Clock input terminal for data shift on rising edge
LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
$\overline{OE}$	Output enable terminal When $\overline{OE}$ (active) low $\overline{OUT0}$ ~ $\overline{OUT15}$ are enabled. When $\overline{OE}$ high $\overline{OUT0}$ ~ $\overline{OUT15}$ are turned OFF (blanked).
SDO	Serial-data output to the following SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

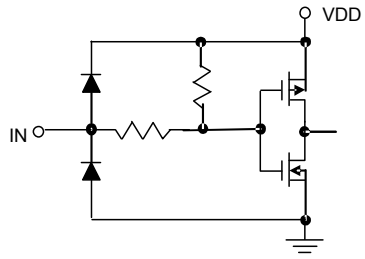
Pin Configuration



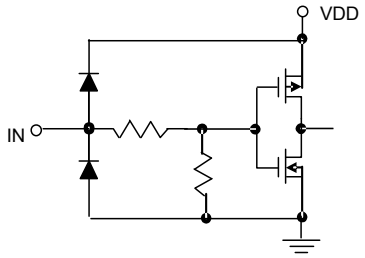
JXI5020GF/ GP

Equivalent Circuits of Inputs and Outputs

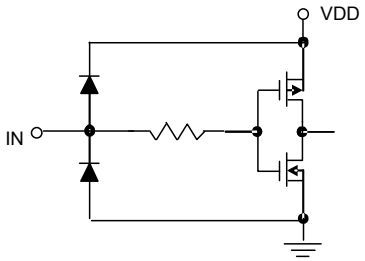
$\overline{OE}$ terminal



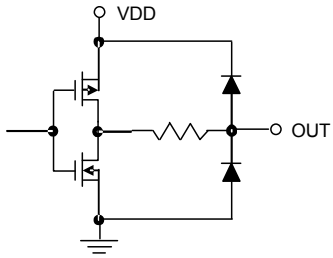
LE terminal



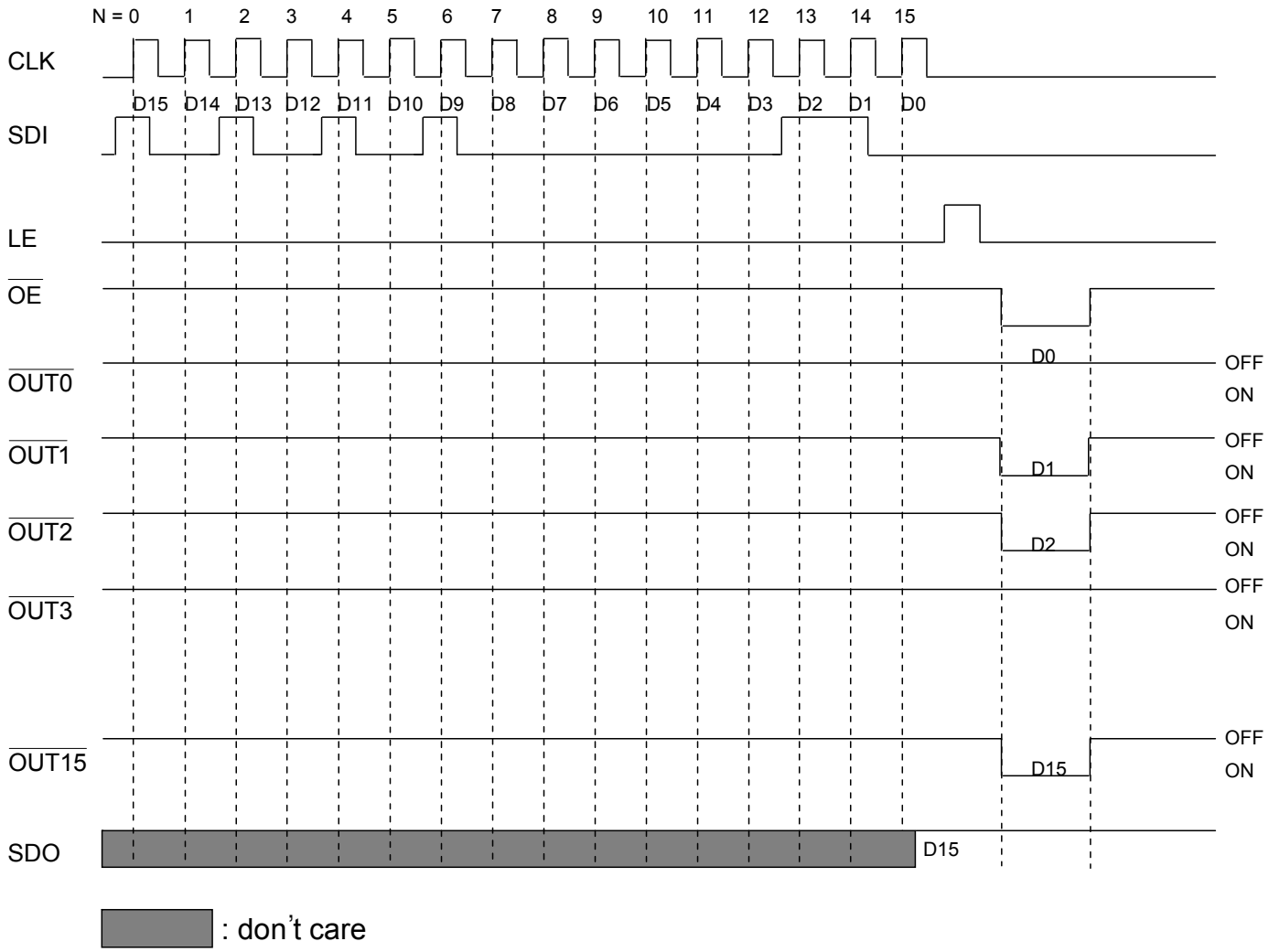
CLK, SDI terminal



SDO terminal



Timing Diagram



Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT7}$ … $\overline{OUT15}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ……. $\overline{D_{n-7}}$ ….. $\overline{D_{n-15}}$	D_{n-15}
↑	L	L	D_{n+1}	No Change	D_{n-14}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ ….. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …. $\overline{D_{n-5}}$ …. $\overline{D_{n-13}}$	D_{n-13}
↓	X	H	D_{n+3}	Off	D_{n-13}

Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7.0	V
Input Voltage		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+45	mA
Sustaining Voltage at OUT Port		V_{DS}	-0.5~+17.0	V
GND Terminal Current		I_{GND}	720	mA
Power Dissipation (On PCB, Ta= 25°C)*	GF-type	P_D	1.69	W
	GP-type		1.37	
Thermal Resistance (On PCB, Ta= 25°C)*	GF-type	$R_{th(j-a)}$	74	°C/ W
	GP-type		91	
Operating Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM (MIL-STD-883H Method 3015.8, Human Body Mode)	HBM	Class 2 (3.5KV)	-
	MM (ANSI/ ESD S5.2-2009, Machine Mode)	MM	Class M4 (400V)	-

* The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

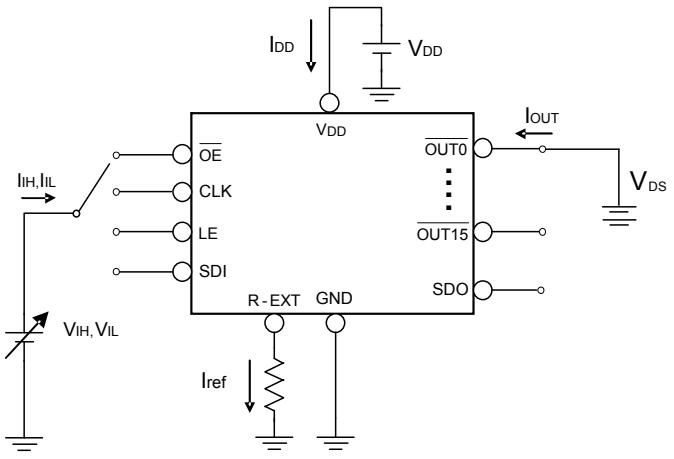
Electrical Characteristics (V_{DD}= 5.0V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17	V
Output Current		I_{OUT}	**Refer to „Test Circuit for Electrical Characteristics"**		3.0	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	„H" level	V_{IH}	Ta=-40~85ºC		0.7 x V_{DD}	-	V_{DD}	V
	„L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3 x V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	µA A
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Output Current 1		I_{OUT1}	V_{DS}=1.0V	R_{ext}=6000 Ω	-	3.1	-	mA
Current Skew		dI_{OUT1}	I_{OL}=3.1mA V_{DS}=1.0V	R_{ext}=6000 Ω	-	±1.5	±2.5	%
Output Current 2		I_{OUT2}	V_{DS}=1.0V	R_{ext}=720 Ω	-	25.8	-	mA
Current Skew		dI_{OUT2}	I_{OL}=25.8mA V_{DS}=1.0V	R_{ext}=720 Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V		-	-	±1.0	%/V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		125	350	490	KΩ
Pull-down Resistor		R_{IN}(down)	LE		125	350	490	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	3.0	3.8	mA
		I_{DD}(off) 2	R_{ext}=720Ω, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	8.0	9.0	
	"ON"	I_{DD}(on) 1	R_{ext}=720Ω, $\overline{OUT0}$~ $\overline{OUT15}$=On		-	8.0	9.0	

Electrical Characteristics (V_{DD}= 3.3V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17	V
Output Current		I_{OUT}	Refer to „Test Circuit for Electrical Characteristics"		3.0	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	„H" level	V_{IH}	Ta=-40~85ºC		0.7 x V_{DD}	-	V_{DD}	V
	„L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3 x V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA A
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
Output Current 1		I_{OUT1}	V_{DS}=1.0V	R_{ext}=6000Ω	-	3.1	-	mA
Current Skew		dI_{OUT1}	I_{OL}=3.1mA V_{DS}=1.0V	R_{ext}=6000Ω	-	±1.5	±2.5	%
Output Current 2		I_{OUT2}	V_{DS}=1.0V	R_{ext}=720Ω	-	25.8	-	mA
Current Skew		dI_{OUT2}	I_{OL}=25.8mA V_{DS}=1.0V	R_{ext}=720Ω	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.3	%/V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	-	±1.0	%/V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		125	350	490	KΩ
Pull-down Resistor		R_{IN}(down)	LE		125	350	490	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext}= Open , $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	2.5	3.3	mA
		I_{DD}(off) 2	R_{ext}=720Ω, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	7.5	8.5	
	"ON"	I_{DD}(on) 1	R_{ext}=720Ω, $\overline{OUT0}$~ $\overline{OUT15}$=On		-	7.5	8.5	

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}= 5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time („L" to „H")	CLK-$\overline{OUT2n}$ *	t_{pLH1}	V_{DD}=5.0V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=930Ω V_L=4.0V R_L=150Ω C_L=10pF	-	37	52	ns
	CLK-$\overline{OUT2n+1}$*			-	35	50	ns
	LE-$\overline{OUT2n}$	t_{pLH2}		-	37	52	ns
	LE-$\overline{OUT2n+1}$			-	35	50	ns
	$\overline{OE}$ -$\overline{OUT2n}$	t_{pLH3}		-	37	52	ns
	$\overline{OE}$ -$\overline{OUT2n+1}$			-	35	50	ns
	CLK-SDO	t_{pLH}		-	25	35	ns
Propagation Delay Time („H" to „L")	CLK-$\overline{OUT2n}$	t_{pHL1}		-	42	52	ns
	CLK-$\overline{OUT2n+1}$			-	40	50	ns
	LE-$\overline{OUT2n}$	t_{pHL2}		-	42	52	ns
	LE-$\overline{OUT2n+1}$			-	40	50	ns
	$\overline{OE}$ -$\overline{OUT2n}$	t_{pHL3}		-	42	52	ns
	$\overline{OE}$ -$\overline{OUT2n+1}$			-	40	50	ns
	CLK-SDO	t_{pHL}		-	25	35	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ **	$t_{w(OE)}$		70	100	-	ns
Hold Time for LE		$t_{h(L)}$		30	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
Maximum CLK Rise Time		t_r		-	-	500	ns
Maximum CLK Fall Time		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$T_{f,SDO}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}		-	40	50	ns
Output Fall Time of Output Ports		t_{of}		-	55	60	ns

*The staggered delay between odd channels, $\overline{OUT2n+1}$ (e.g. OUT1, OUT3, OUT5, etc.) and even channels $\overline{OUT2n}$ (e.g. OUT2, OUT4, OUT6, etc.) is 2ns. JXI5020 has a built-in staggered circuit to perform delay mechanism, by which the even and odd output ports will be turned on at a different time so that the instant current from the power line will be lowered.

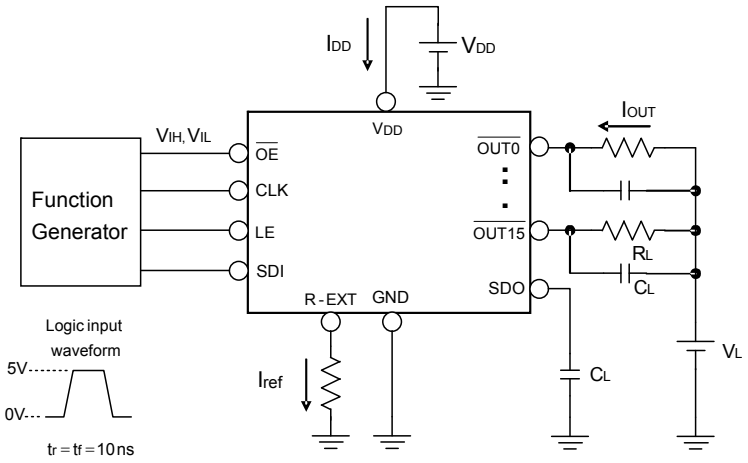
** With uniform output current.

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time („L" to „H")	CLK- $\overline{OUT2n}$ *	t_{pLH1}	V_{DD}=3.3V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=930Ω V_L=4.0V R_L=150Ω C_L=10 pF	-	52	72	ns
	CLK- $\overline{OUT2n+1}$*			-	50	70	ns
	LE- $\overline{OUT2n}$	t_{pLH2}		-	52	72	ns
	LE- $\overline{OUT2n+1}$			-	50	70	ns
	$\overline{OE}$ - $\overline{OUT2n}$	t_{pLH3}		-	52	72	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$			-	50	70	ns
	CLK-SDO	t_{pLH}		-	35	45	ns
Propagation Delay Time („H" to „L")	CLK- $\overline{OUT2n}$	t_{pHL1}		-	52	62	ns
	CLK- $\overline{OUT2n+1}$			-	50	60	ns
	LE- $\overline{OUT2n}$	t_{pHL2}		-	52	62	ns
	LE- $\overline{OUT2n+1}$			-	50	60	ns
	$\overline{OE}$ - $\overline{OUT2n}$	t_{pHL3}		-	52	62	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$			-	50	60	ns
	CLK-SDO	t_{pHL}		-	35	45	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ **	$t_{w(OE)}$		100	130	-	ns
Hold Time for LE		$t_{h(L)}$		30	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
Maximum CLK Rise Time		t_r		-	-	500	ns
Maximum CLK Fall Time		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$T_{f,SDO}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}		-	60	75	ns
Output Fall Time of Output Ports		t_{of}		-	60	75	ns

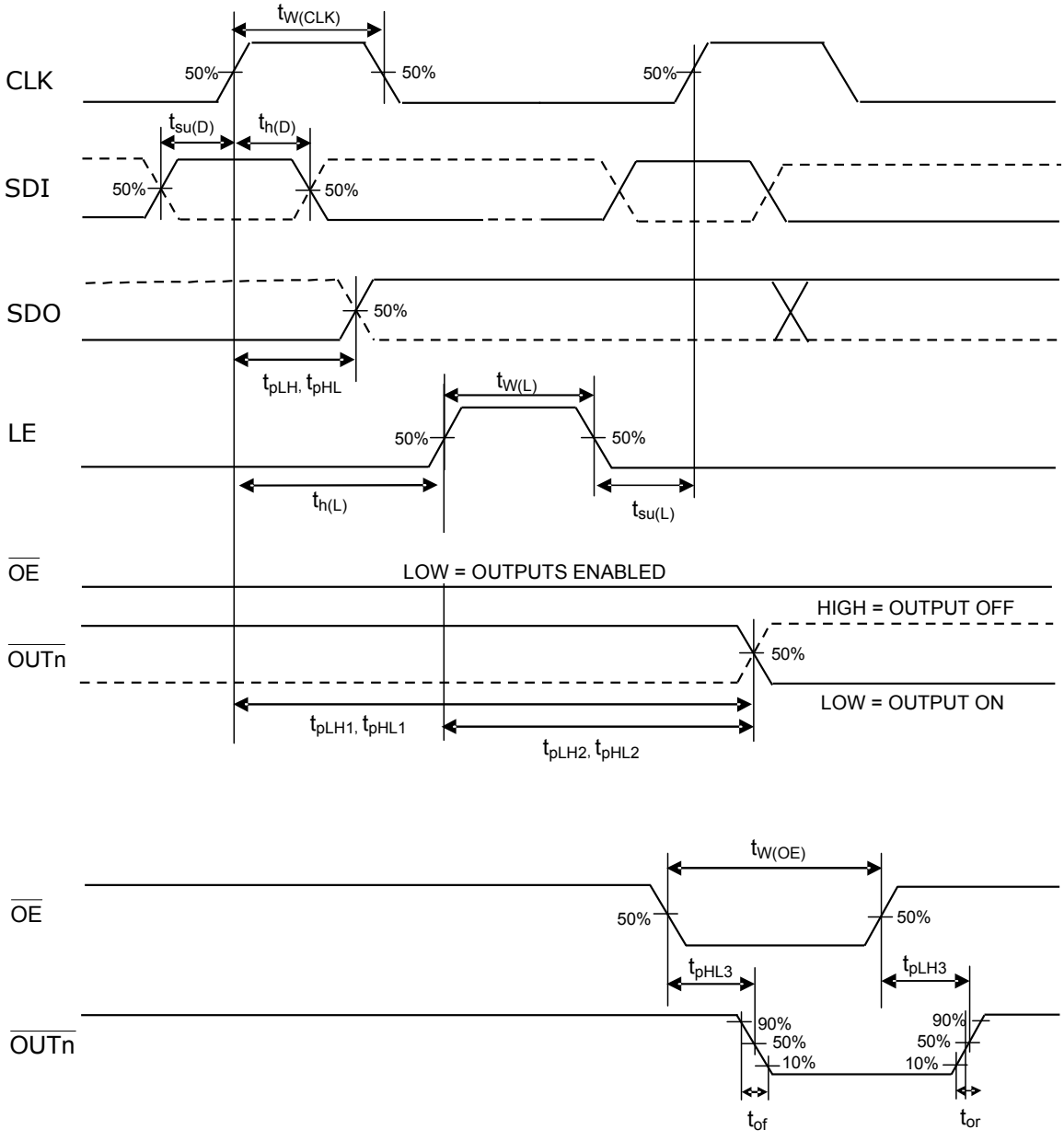
*The staggered delay between odd channels, $\overline{OUT2n+1}$ (e.g. OUT1, OUT3, OUT5, etc.) and even channels $\overline{OUT2n}$ (e.g. OUT2, OUT4, OUT6, etc.) is 2ns. JXI5020 has a built-in staggered circuit to perform delay mechanism, by which the even and odd output ports will be turned on at a different time so that the instant current from the power line will be lowered.

** With uniform output current.

Test Circuit for Switching Characteristics



Timing Waveform



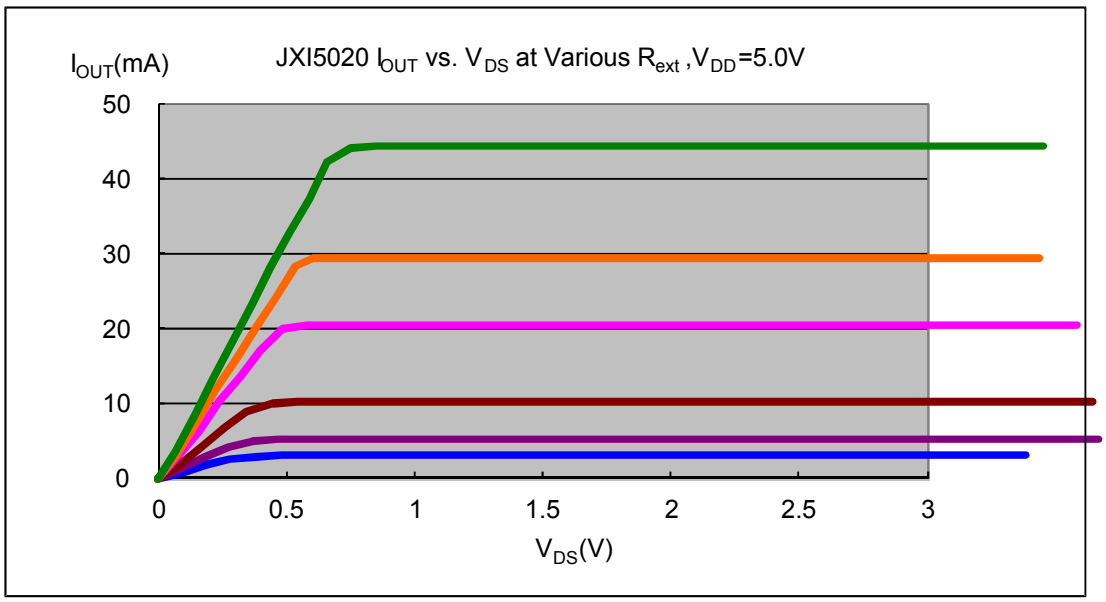
Application Information

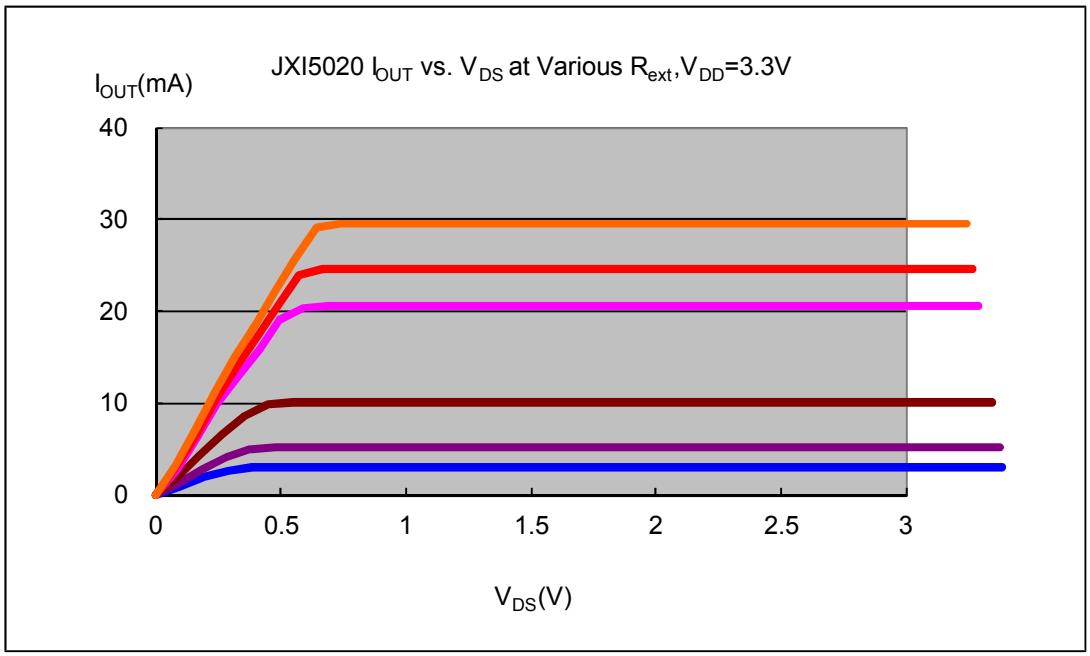
Constant Current

To design LED displays, JXI5020 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than ±2.5%, and that between ICs is less than ±3%.

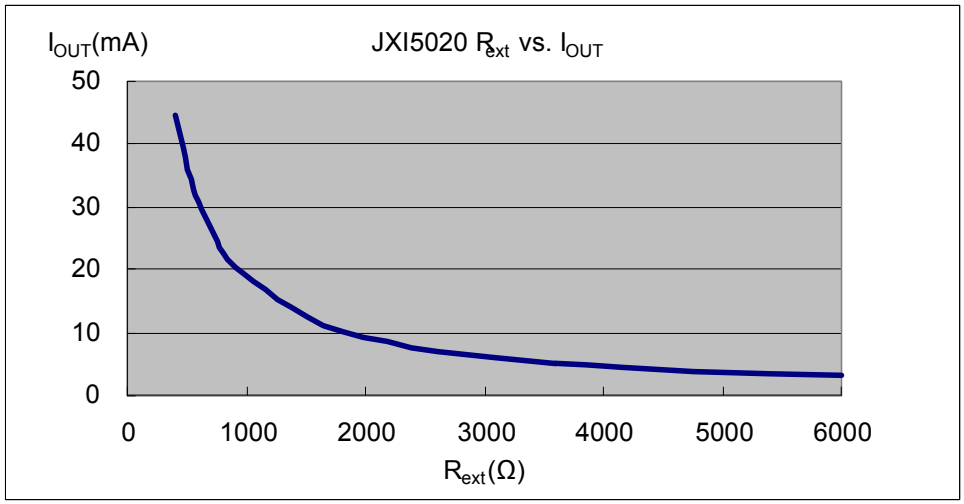
2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This performs as a perfection of load regulation.





Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.



Also, the output current can be calculated from the equation:

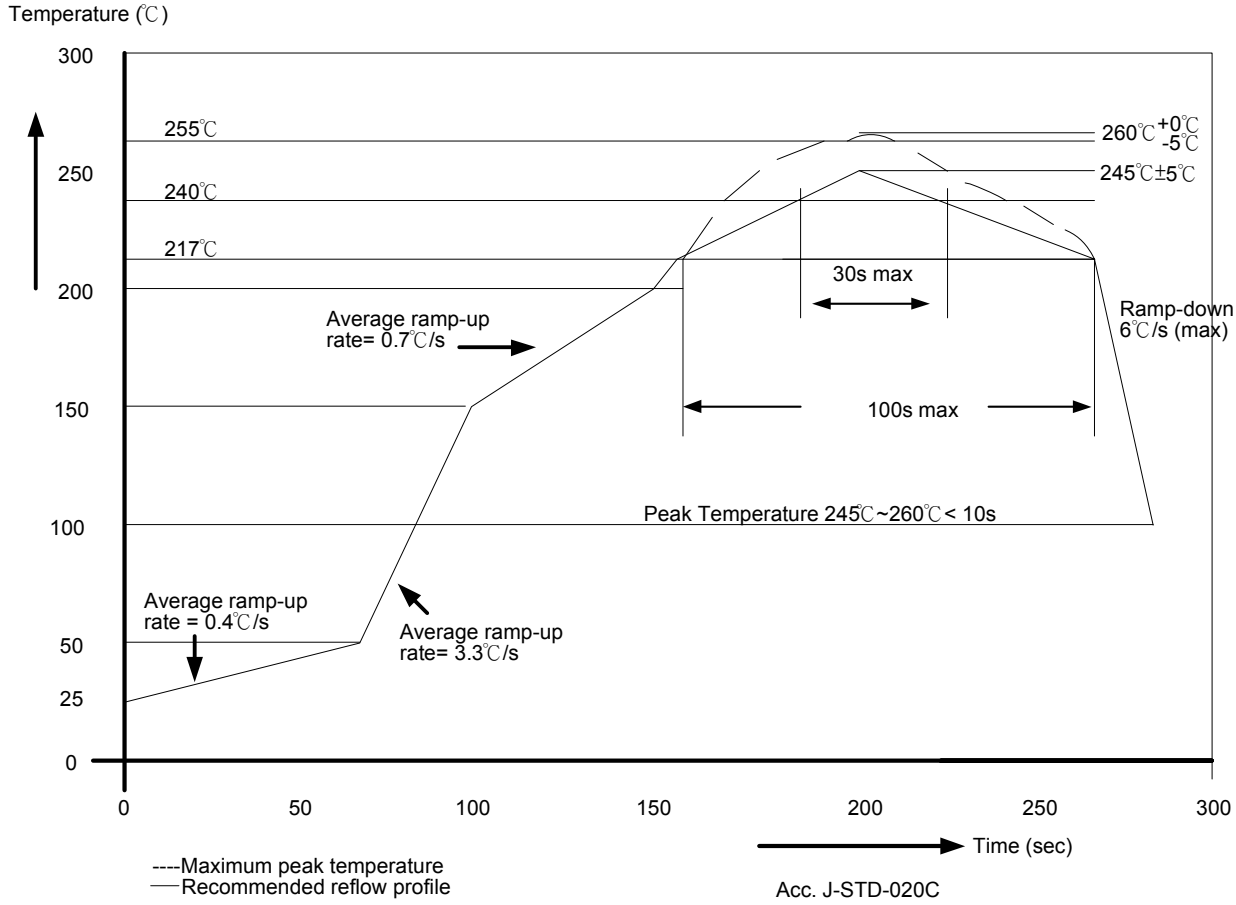
$V_{R\text{-}EXT}$=1.24V; $I_{OUT}=V_{R\text{-}EXT}$ *(1/Rext)x15; $R_{ext}=(V_{R\text{-}EXT}/I_{OUT})$x15

where R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is the voltage of R-EXT terminal. The magnitude of current (as a function of R_{ext}) is around 25mA at 744Ω and 10mA at 1860Ω.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245°C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.

For managing MSL3 Package, it should refer to JEDEC J-STD-0 20C about floor life management & refer to JEDEC J-STD-033C about re-bake condition while IC's floor life exceeds MSL3 limitation.



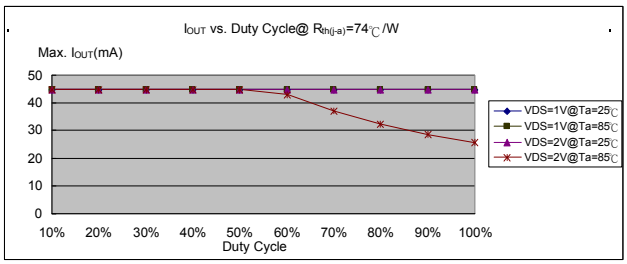
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

* For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

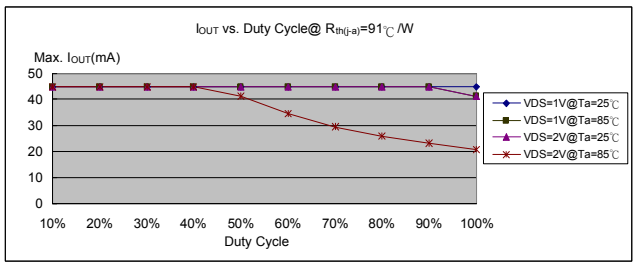
Package Power Dissipation (P_D)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.



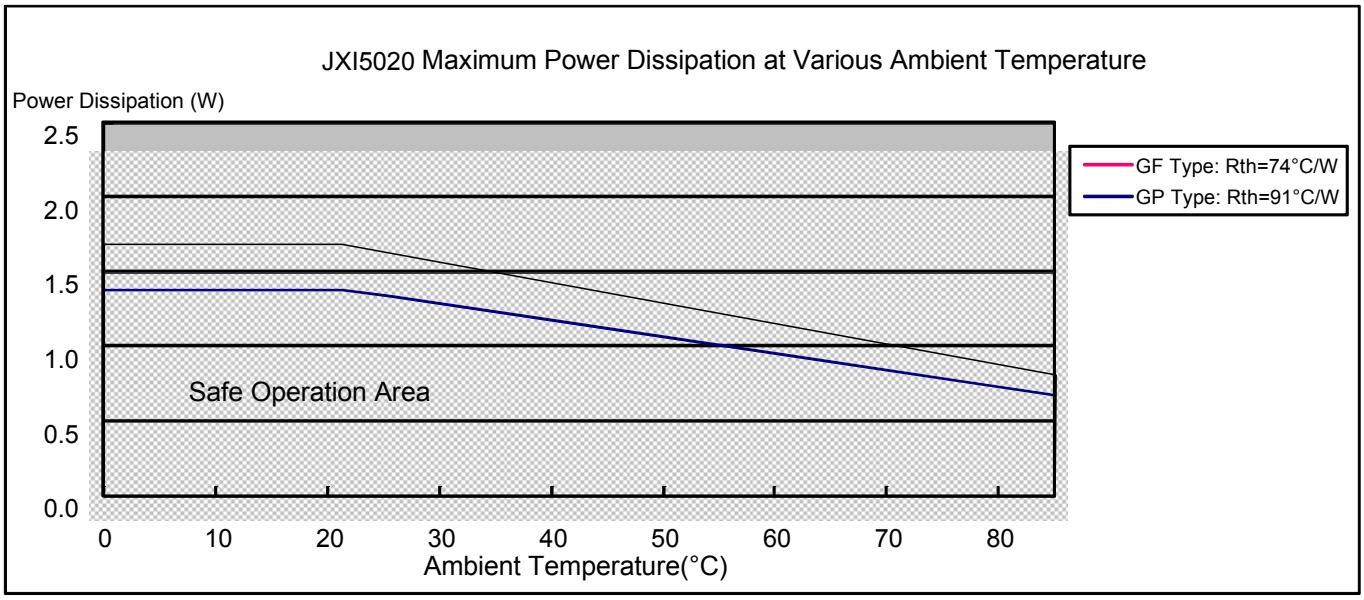
JXI5020GF



JXI5020GP

Condition: I_{OUT}=45mA 16 output channels active		
Package	$R_{th(j-a)}$ (°C/W)	P_D (W)
GF	74	1.69
GP	91	1.37

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.

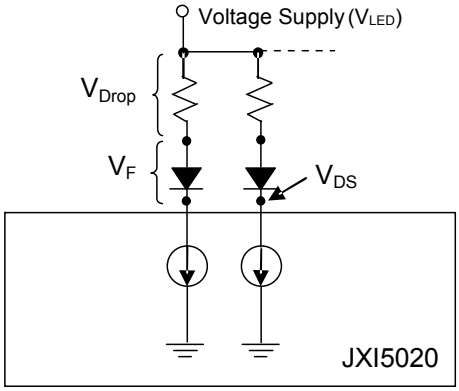


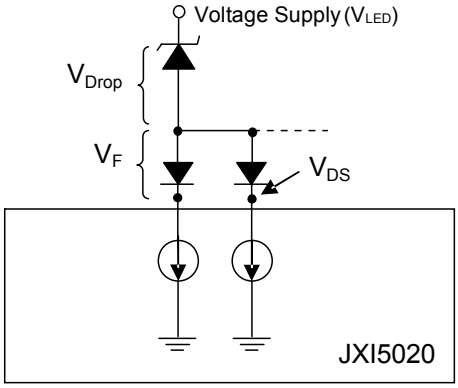
Load Supply Voltage (V_{LED})

JXI5020 are designed to operate with V_{DS} ranging from 0.4V to 0.8V (depending on I_{OUT}=3~45mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)} > P_{D(max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

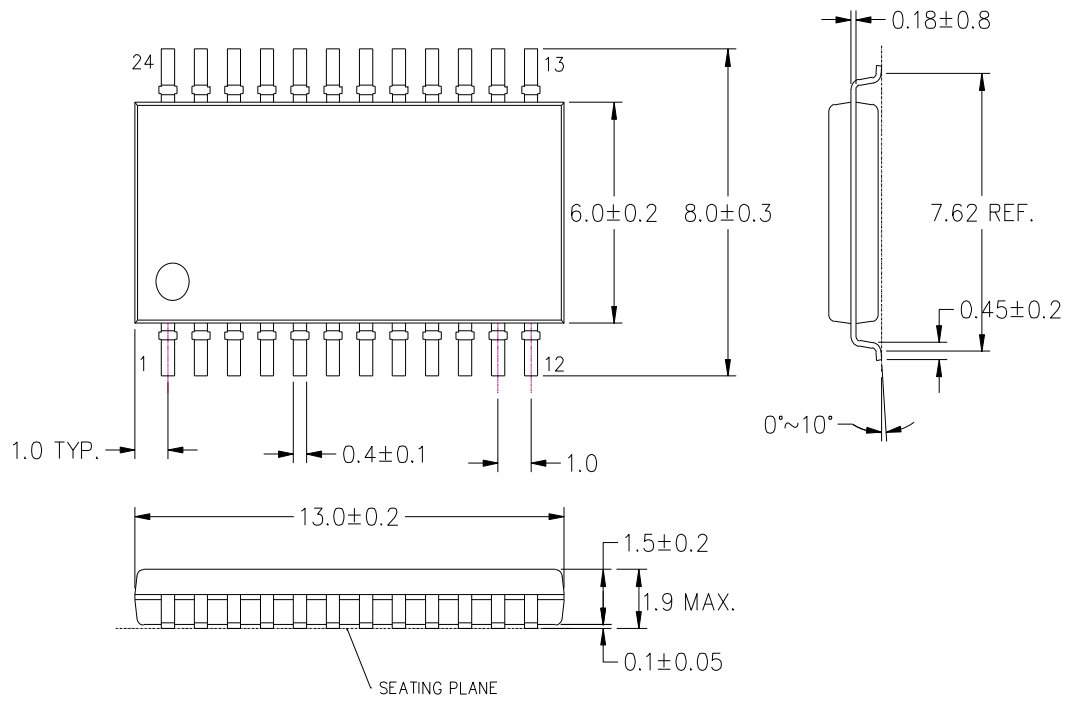
A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.



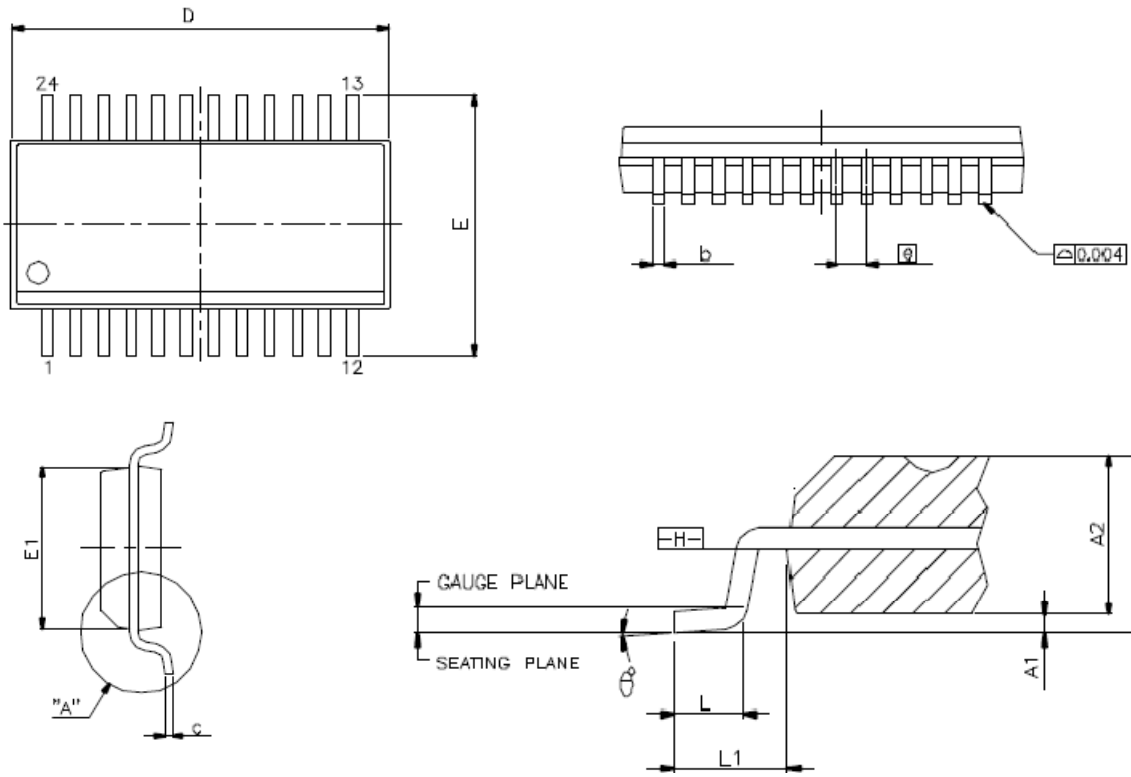


Package Outline



Unit: mm

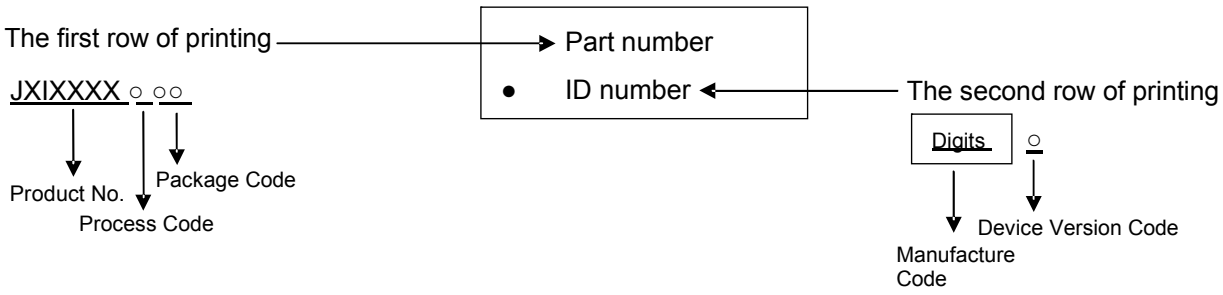
JXI5020GF Outline Drawing



SYMBOLS	Dimensions shown in inches			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ	0	—	8	0	—	8

JXI5020GP Outline Drawing

Product Top-mark Information



Product Revision History

Datasheet Version	Device Version Code
V1.00	A
V1.01	A
V1.02	A
V2.00	B
V2.01	B

Product Ordering Information

Part Number *	RoHS Package Type	Weight (g)
JXI5020GF-B	SOP24L-300-1.00	0.28
JXI5020GP-B	SSOP24L-150-0.64	0.11

*Please place your order with the „Part Number" information on your purchase order (PO).

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